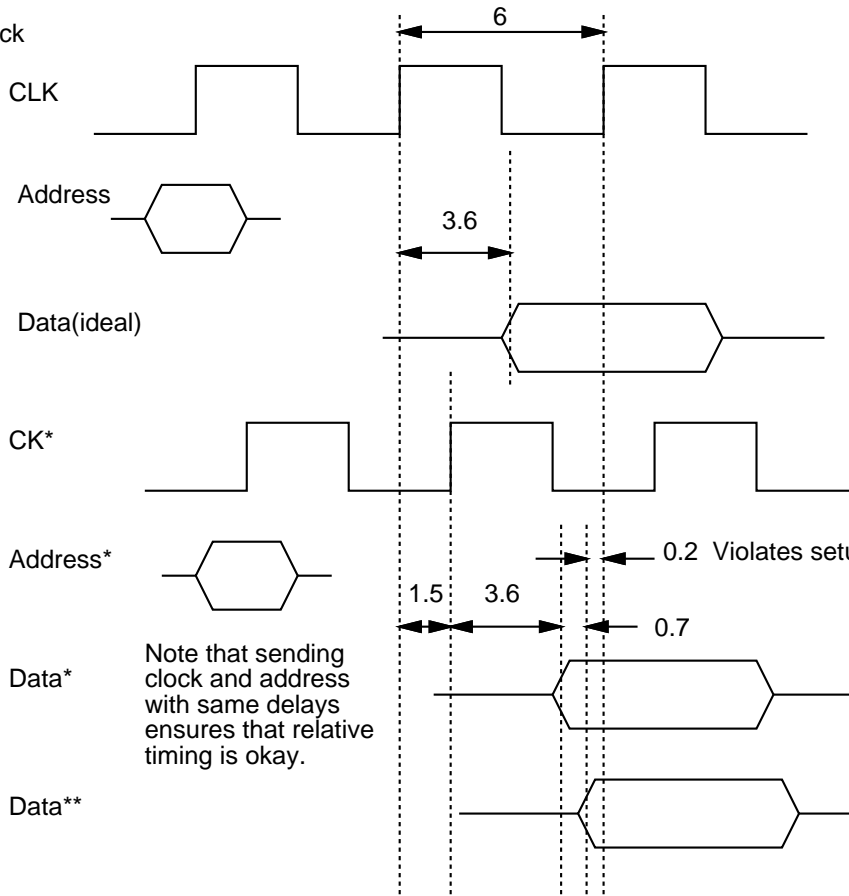


167MHz clock



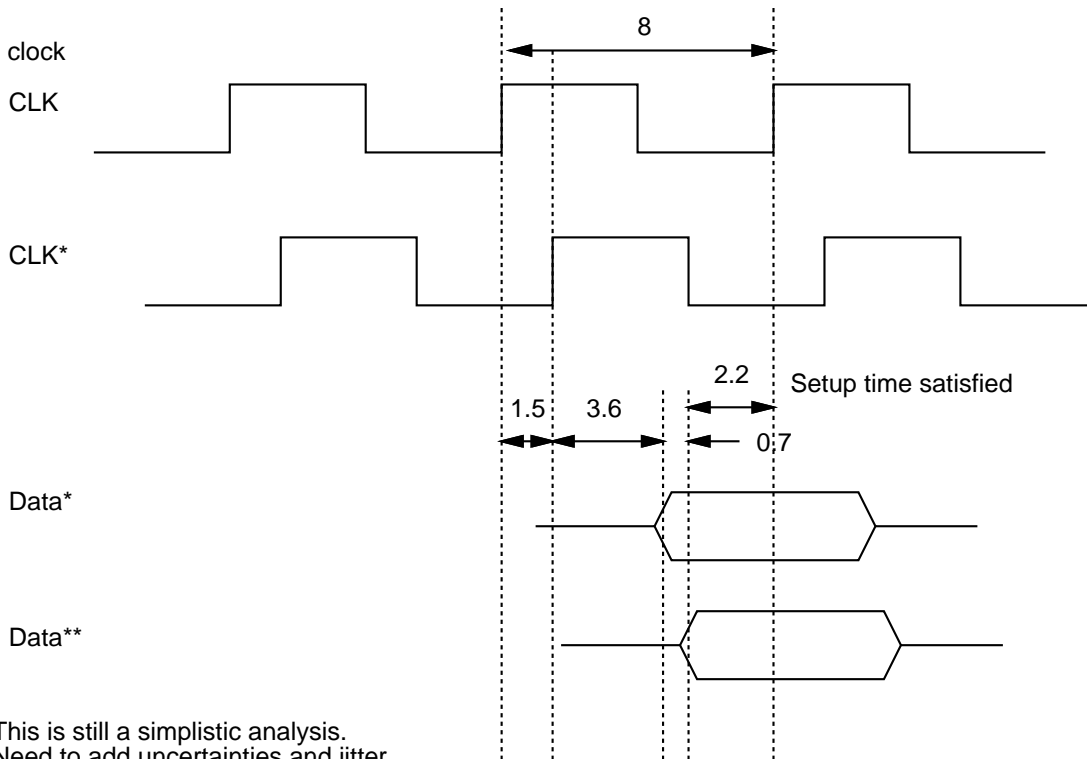
FPGA FF
 $t(\text{setup}) = 0.8$
 $t(\text{hold}) = -0.4$

Memory Clk high
to output valid = 3.6

Use DCM to align clocks
and get back 1.5ns, leaving
 $0.2 + 1.5 - 0.8 = 0.9\text{ns}$ margin

Note that sending
clock and address
with same delays
ensures that relative
timing is okay.

125 MHz clock



This is still a simplistic analysis.
Need to add uncertainties and jitter.