How to add an external port such as a pushbutton to a Verilog design.

1. Add the variable name to the VHDL file as follows;
   There are 3 different spots within the vhd file that the variable name must be added.

```
entity <module_name> is
    port (
        -- ADD USER PORTS BELOW THIS LINE ------
        --USER ports added here
            <variable name>
         -- ADD USER PORTS ABOVE THIS LINE -----
    end entity <module_name>

    component <user_logic> is
        port (
        -- ADD USER PORTS BELOW THIS LINE -------
        --USER ports added here
            <variable name>
        -- ADD USER PORTS ABOVE THIS LINE ------
    end component user_logic;

    ----------------------------------------
    -- instantiate User Logic
    ----------------------------------------
    USER_LOGIC_I : component user_logic

  port map
  (
    -- MAP USER PORTS BELOW THIS LINE ---------------
    --USER ports mapped here
        variable_name => variable_name,
    -- MAP USER PORTS ABOVE THIS LINE ---------------
  );
```

2. Add the variable name to the Verilog file

```
module user_logic
(
    // -- ADD USER PORTS BELOW THIS LINE ---------------
     // --USER ports added here
    variable_name,
    // -- ADD USER PORTS ABOVE THIS LINE ---------------
);
```

3. Re-import the peripheral in EDK.
    a. Go to the “Create and Import Peripheral” in “Hardware” dropdown menu in EDK and click next
    b. Check the box that says “Import Existing Peripheral”, click next
    c. Ensure “To an XPS project” is checked and the right project is listed, click next
    d. In the dropdown box click on the name of your module and click next
    e. Select “HDL source files”, click next
    f. Two steps
        i. In the drop down box “HDL language used to implement your peripheral:” ensure “Mixed” is selected
        ii. Select “Use an existing Peripheral Analysis Order file”, browse to the pao file of your project select it and click next
            Note: ensure that the contents pao file contains your Verilog module and well as the VHDL module
    g. Click next on the “HDL Analysis Information” page
    h. “Select the bus interfaces” that your design uses and click next
    i. Click next on the “MPLB + SPLB : Port” page
    j. Click next on the “SPLB : Parameter” page
    k. Uncheck “Select and configure interrupts” (if selected), click next, unless you want your variable to act as an interrupt signal
    l. Click next on the “Parameter Attributes” page
    m. Click next on the “Port Attributes” page
    n. Finally click Finish

4. Go to the “Ports” window of the “System Assembly View” in EDK, find your port name (should be in the expanded view of your module name) and make the port external.

5. Finally you must add the proper constraints to the UCF file of your design. Use the name given in the expanded view of “External Ports” section of the “Ports” window to do so.