Project Demos and Reports

ECE532S: Digital Systems Design

Spring 2011

1 Demo (20%) April 6, 2011

Please ensure that you have signed up for a demo slot. Contact your TA for a time if you do not have one yet.

The TAs and I will be going around as a group to see each project. You will first give an oral presentation describing your project. Each member of the group should make part of the presentation. Be prepared to answer many questions about what you did, the issues you had, how it works, etc.

Please be *Ready to Run* at the appointed time. Ready to run means that your circuit is downloaded and running. Time is tight and we do not want to be waiting for downloads to occur, so please try to have all displays up and running with what you want to show.

Your presentation must include the items in the following outline. Please make sure everything will fit in 20 minutes so think through the presentation and demonstration beforehand. A rehearsal or two would not be a bad idea. Preparing a few slides (Powerpoint or equivalent) will help you organize the presentation better.

- what your project is about
- what your initial goals were
- what you ended up with and why
  - what problems you had
  - what changes you had to make
  - good block diagrams will be helpful to show originally planned and resulting systems
- what code/blocks you created, what you grabbed from other places
- your design process – what did you do to ensure success?
- what you learned
- demo
  - something working
  - else interesting simulations

Individuals may receive different grades depending on how well each of you know the project.

2 Competition for Xilinx Prizes

A number of groups (approximately four) will be selected to proceed to another round of presentations that will be judged by people from Xilinx. The goal is to impress Xilinx with your projects! The winning group will be awarded Digilent Spartan 3E-Starter boards valued at US$149 each. The actual time will be arranged at a later date when everyone is available.

3 Group Report (17.5%) April 4, 2011

Late reports will be docked 3% out of the 17.5% for each day late.

The report should be the complete documentation of your project and strictly technical information. It should be a self-contained document that includes all references or pointers to all the information and documentation that you needed, such as data sheets, IP (hard or soft) that you got from elsewhere, other tools you used, etc. A test for completeness of the report is whether another person could take your report and figure out how to make your design work, modify it or maintain it. I will also be looking at your own code for style and, especially, comments!

Well-documented and functioning projects will be placed online as example designs.

If you have a working pcore we could make available, that would be welcome. Please put it in the appropriate directory structure and send me a zip/tar file.

Please follow the follwoing structure in your report:

Overview A high-level description of the project: motivation for doing the project, goals, block diagram, brief description of IP used, modified, created, or where it came from.

For the block diagram, please see the example posted under *Project Proposal* on the course web page, and the comments I've made about it. You will need a diagram that looks like that one.

Outcome Results. How well it works (or not). How could you improve the system that you built? What would you do differently if you could start over? If someone were to take over your project, what would you recommend as the next steps?

Description of the Blocks More detailed description of each of the IP blocks that you have used. This can be as simple as saying you used the XYZ Ver. x block from the library. It could also be a link to the origin of the code that you found online somewhere. You must also describe what changes you might have made. Ideally, you should have a source code control directory (like CVS) that contains the original version. Please document any other things you might have done to use this IP, such as additional constraints needed for compilation or synthesis, testing procedure, testbenches, test vectors.

Description of Your Design Tree As part of your submission, please send me a zip file or gzip tar file of your design directory. Include your group report in a *doc* directory but **NOT** your individual reports in the archive. If you make presentation slides, it would be good to include those. You may send me the archive after the presentations so that I receive the latest version of your slides.

Please do not send non-zip archive formats, such as rar, because zip files are easier for people to extract when I make them available on the web.

If the file is larger than 1MB, please do not send it as an attachment. You can use a service such as `www.yousendit.com` to exchange the file.

In addition, please send me electronic versions of your reports. I will make the group report and design tree available online and will archive all the reports electronically. Do not include your individual reports in the design tree because I will not be making those available online.

In this section, document what has been sent in the file. You should also include this information as a README file at the top level of your design tree directory.

Tips and Tricks I have a page online with Project Tips. If you anything to add that will benefit future students, please list them here.

Video This is not required, but it helps to promote what this course is about. For example, it is nice to send videos to Xilinx so that they can see what we are up to. A video also helps future students see what these projects are about. If you have time and are so inclined, please send me a video file or a youtube link and I will post it.

4 Individual Report (17.5%) April 4, 2011

Late reports will be docked 3% out of the 17.5% for each day late.

Here you have the opportunity to describe your contribution to the project and to give some additional feedback. This is where you can talk about the pain and anguish you went through in terms of what you tried, what worked, what did not, and how you eventually made things work.

This is a significant component of your grade and I need to see significant evidence of the work you did on the project.

Again, please follow the structure outlined below:

Introduction Feel free to borrow from the group report. You should also reference the group report for the full documentation.

What you did Include discussions of items like:

- How was the project partitioned?
  - What did you do on the project?
  - How did you ensure that your part would work with the parts done by other members of your team?
- What hurdles did you have to overcome?
- What other things did you learn about the various tools?
- What other tools did you try to use?
- What did you do to ensure success, or at least improve the likelihood of success?
  - what was your design flow?
  - what kind of source code control did you use?
  - what kind of simulations and/or testing did you do on your code?
- What modules did you write? How did you test them?
- What did you learn?
- Anything else you spent your time on (related to the project :-)

Community Contribution Please indicate your community contributions. I will observe who has been giving help on the bboard but indicate in this section what kinds of help you provided to make sure I account for it.

Also, if you figured out how to do something that isn't easy to find or documented well, or if you just came up with a simple example of how to do something that you wished you had available at the start, please write it up so that we can make it available to future users. Include it as a section in your report, but also send me a zip/tar file of the example and the document as well so that I can post it.

Feedback to Xilinx Xilinx is very interested in obtaining feedback about the tools. If there are features you liked, didn't like, or wish you had, please document them here. This could include things like "menu X should do this", to "it should be much easier to do Y."

Course feedback Any comments or suggestions you would like to make about the course for the future.

- Did the project timeline work, i.e., demos, deadlines? Could the project be started earlier?
- Does the grading structure work? Suggestions?
- Did you like the "open" lab concept, i.e., do these modules by this time and do these tasks at the end? i.e., instead of trying to grade something each week.
- I know the lectures need to be organized better still. Any other constructive comments on content and organization?