XUPV2P DDR SDRAM Memory Instructions

Objective

This document contains instructions on how to add the Multi-Port Memory Controller (MPMC) peripheral to an XPS system to use the DDR SDRAM on the XUPV2P board.

What You Need

- XUPV2P Board Kit
- Kingston KVR266X64C25/256 DIMM (256 MB) installed on XUPV2P
- Xilinx 10.1.02 ISE/EDK

Steps

1. Create a new XPS project and run the Base System Builder as in the m01 lab with the following exception. Choose the **Processor-Bus Clock Frequency** to be *100 MHz*.
2. Double click *clock_generator_0* to bring up its dialog box.
3. Choose *CLKOUT1* on the left, then…
    a. **Connected to =** *sys_clk_s_90*
    b. **Required frequency (Hz) =** *100,000,000*
    c. **Required phase shift =** *90*
    d. **Grouping information =** *DCM0*
    e. **Buferred =** *TRUE*
4. Choose *CLKOUT0,* change **Grouping information** to *DCM0.*
5. Choose *CLKOUT2* on the left, then…
    a. **Connected to =** *MPMC_Clk_Mem*
    b. **Required frequency (Hz) =** *100,000,000*
    c. **Required phase shift =** *20*
    d. **Grouping information =** *NONE*
    e. **Buferred =** *TRUE*
6. Click OK to exit the dialog box.
7. Add the MPMC to the system, instance name should be mpmc_0. (**IP Catalog -> Memory and Memory Controller -> Multi-Port Memory Controller(DDR/DDR2/SDRAM) v4.02a**). It is recommended you take a look at the MPMC datasheet here.
8. Connect the MPMC's two Slave PLB connections to the PLB.
9. Go to the addresses tab and set the following
    a. C_MPMC_BASEADDR : Size = 256M, Base Address = 0x10000000
    b. C_MPMC_CTRL_BASEADDR : Size = 64K, Base Address = 0x0FFF0000
10. Double Click the MPMC to bring up its dialog box (may take a few seconds). Set the following:

a. **Base Configuration Tab**
    i. Do nothing.
b. **Memory Interface Tab**
    i. On the top row (**Memory Part Selector**) select the following
        1. **Type** = *DDR*
        2. **Manufacturer** = *Wintec*
        3. **Style** = *DIMM*
        4. **Density** = *x256mbyte*
        5. **Width** = *x64*
        6. **Part No.** = *W4F232726HA-5Q*
    ii. Now change the Part No. to **Custom.**
    iii. Look at the **Configuration** section in the middle of the screen. Click the **X** button next to **Clock Width**. Choose *3* from the drop down list.
    iv. Uncheck the CHECKBOX (not the **X** button) for Registered Memory.
    v. Click the **Memory Part Settings** tab (midscreen) within the **Memory Interface** tab
    vi. Set the following in the **Memory timing Settings**
        1. CAS Latency A Fmax = 100MHz
        2. CAS Latency A = 2.5 (3)
        3. tRAS (ps) = 60000
        4. tRASMAX (ps) = 120000000
        5. tRC (ps) = 90000
        6. tWR (ps) = 20000
        7. tRRD (ps) = 20000
        8. tRCD (ps) = 30000
        9. tREFI (ps) = 7800000
        10. tRFC (ps) = 100000
        11. tRP (ps) = 30000
c. **Port Configuration Tab**
    i. Do Nothing
d. **Advanced Tab**
    i. In the **ECC/PM/PHY** tab
        1. Check the **Enable Static PHY** box
        2. **Sets Power-on/reset Value of RDDATA_CLK_SEL Register** = *0*
        3. **Sets Power-on/reset Value of RDDATA_SWAP_RISE Register** = *0*
        4. **Sets Power-on/reset Value of RDENDELAY Register** = *6*
e. **Click OK to exit the dialog box.**

11. In the System Assembly View Ports Tab, look at the mpmc_0 ports. Make all the ports that start with *DDR* external.
12. Assign the following mpmc ports as…
    a. **MPMC_Clk_Mem** = *MPMC_Clk_Mem*
    b. **MPMC_Rst** = *sys_periph_reset*

    c. **MPMC_Clk90** = *sys_clk_s_90*
    d. **MPMC_Clk0 =** *sys_clk_s*
    e. All others leave unconnected.
13. Copy the constraints found in *ddr_mem.ucf* into your UCF file.
14. Build your bitstream. You may get warnings about "logical net 'NXXX' has no driver" and "Dangling Pins on block …..". These warnings do not seem to affect operation.
15. Create a new software project. Set *No Optimizations* in the **Compiler Options**.
16. Add the *ddr_test.c* source file to the project and build the software.
17. Download to the XUPV2P. Connect the serial cable and open up Hyperterminal. It may be beneficial for you to set Hyperterminal to capture text via **Transfer -> Capture Text**.
18. Each test in *ddr_test.c* will report the number total operations, successes, and failures. If all your tests run without any failures, your DDR SDRAM is (probably) configured properly. This will take several minutes to run.
19. There are many other techniques for testing memory. The ones included in *ddr_test.c* are fairly basic and are not comprehensive (e.g. no walking 1's or walking 0's tests, etc). Passing the tests does not guarantee proper DDR operation in all use cases. If you are ever in doubt, use XMD mwr and mrd to check the memories operation.
20. The MicroBlaze does not seem to support bursting over the PLB. If you want bursting or don't want to use the PLB/MicroBlaze, look at the different MPMC interfaces in its datasheet.