

University of Toronto
Faculty of Applied Science and Engineering

Test 2 – April 2004

ECE532S – Digital Hardware

Examiner – Paul Chow

1. There are 5 questions and **10** pages. Do **all** questions. The total number of marks is 50. The duration of the test is 50 minutes.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. **No calculators or other computing devices allowed.**
4. Closed book. No aids permitted.

1 [10]	
2 [10]	
3 [10]	
4 [10]	
5 [10]	
Total [50]	

1. Starting with some short answer questions:

[2 marks]

(a) Define setup and hold time for a flip flop.

[2 marks]

(b) What happens when a flip flop goes metastable and how long will it stay in that state?

[2 marks]

(c) What is a clock domain?

[2 marks]

(d) Why is flip chip bonding preferred for high-speed packaging?

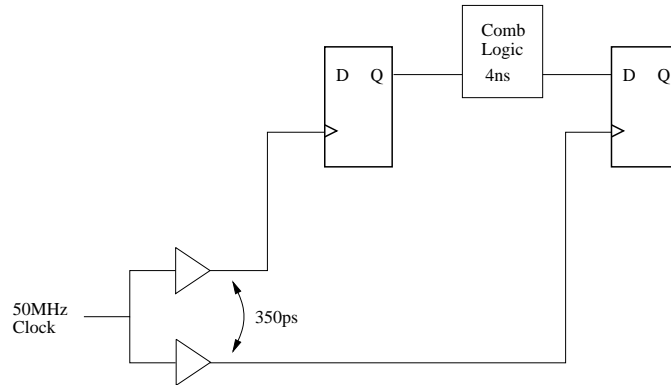
[2 marks]

(e) What is jitter in the context of timing analysis?

[10 marks] 2. Using a figure, describe how a basic MicroBlaze system is implemented. For each of the following components or functions you must show where (in FPGA, on board, in PC, etc.) and how they are implemented (FPGA logic, external chip, etc.). Also show how all the pieces are connected.

- MicroBlaze processor
- UART
- Ethernet physical layer interface (PHY)
- instruction and data memory using on-chip memory
- Ethernet controller
- instruction and data memory using off-chip memory
- serial port (RS232) physical drivers
- FPGA download functions
- XMD stub
- gcc

3. Consider the circuit shown below:



From the data sheets you have also gathered the following information about the flip flops:

$$\begin{aligned}t_{\text{setup}} &= 0.8ns \\t_{\text{hold}} &= 0.4ns \\t_{\text{ClockToQ}} &= 0.5ns\end{aligned}$$

The clock tree has a maximum skew of $350ps$, i.e., the phase of any one branch could be ahead or behind the other by $350ps$.

The clock source is a 50 MHz clock, or $20ns$ period with a jitter of $400ps$.

[5 marks]

- (a) There is a delay of $4ns$ accounting for the combinational logic and the wire delay for the data travelling between the two flip flops.

Being a very conservative designer, you also like to add $500ps$ of timing margin to all of your calculations.

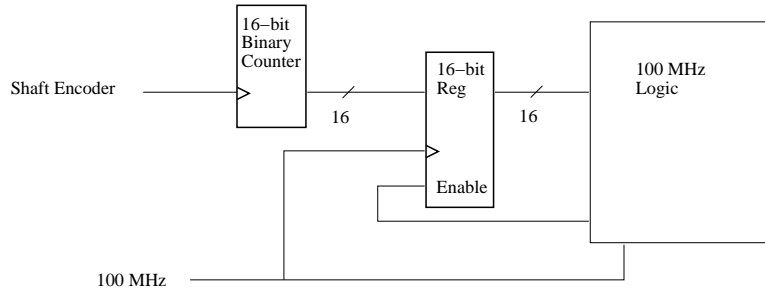
Determine whether the circuit will operate correctly (assuming that you include your own timing margin) by checking the *setup* and *hold* times for the receiving flip flop in the above circuit.

Question 3(a) continued...

[5 marks]

- (b) You also know of a similar circuit in another part of your design, except that it does not have the combinational logic. The output of the first flip flop connects directly to the input of the second flip flop. Assuming that the routing delay is $100ps$, determine whether this circuit meets timing.

4. You have inherited the anti-lock braking system module for a car as the next task in your job. There have been numerous reports of the system not working properly. The circuit capturing the data from the shaft encoder to calculate the speed is shown below.



The shaft encoder generates 1000 pulses per revolution. The pulses are counted in the 16-bit binary counter. The value of the counter is periodically sampled in the 100MHz domain when the Enable signal goes high. The sampling period is frequent enough that the 16-bit counter has adequate range.

[5 marks]

- (a) Why is this circuit unreliable? Give an example of how it could fail.

Question 4 continued...

[5 marks]

- (b) How would you fix this circuit? You are free to start over with a new design, except that the same shaft encoder is to be used and the core logic should run at 100MHz.

5. You have just joined a new company as the team leader of the ASIC verification group. After a number of weeks of hiring, you are now meeting your team of young recruits who are fresh out of school.

[3 marks]

(a) What will you tell your team about the importance of simulation in the overall ASIC design flow?

[3 marks]

(b) Your team has just grown to add some people that will be responsible for verifying a large FPGA. What will you tell them about the differences between designing ASICs and FPGAs?

[4 marks]

(c) One of the new recruits says that simulation is a waste of time for FPGAs. What is your response?