Print:

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Student Number:. . . . .

University of Toronto
Faculty of Applied Science and Engineering

Test II – April 2005
Wallberg 119

ECE532S – Digital Hardware

Examiner – Paul Chow

1. There are 4 questions and **9** pages. Do **all** questions. The total number of marks is 40. The duration of the test is 50 minutes.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. **No calculators or other computing devices allowed.**
4. Closed book. No aids permitted.

1 [10]	
2 [10]	
3 [10]	
4 [10]	
Total [50]	

1. Starting with some short answer questions:

[2 marks] (a) Under what conditions will a flip flop safely, or properly capture data at its input?

[2 marks] (b) What is the potential impact if the above conditions are violated?

[2 marks] (c) What is static timing analysis?

[2 marks] (d) Why is 8B10B coding used in high-speed serial data links?

[2 marks] (e) Why do the latest high-speed interfaces use serial transmission?

2. You need to transmit data between two FPGAs at the rate of 400 MBytes/s. Your board designers say that they can provide you with a 32-bit bus plus a few other lines if you need them. They are recommending a source synchronous interface.

[2 marks] (a) To maximize the timing margins, the clock needs to be phase shifted at the receiving end. What are two acceptable ways to phase shift the clock?

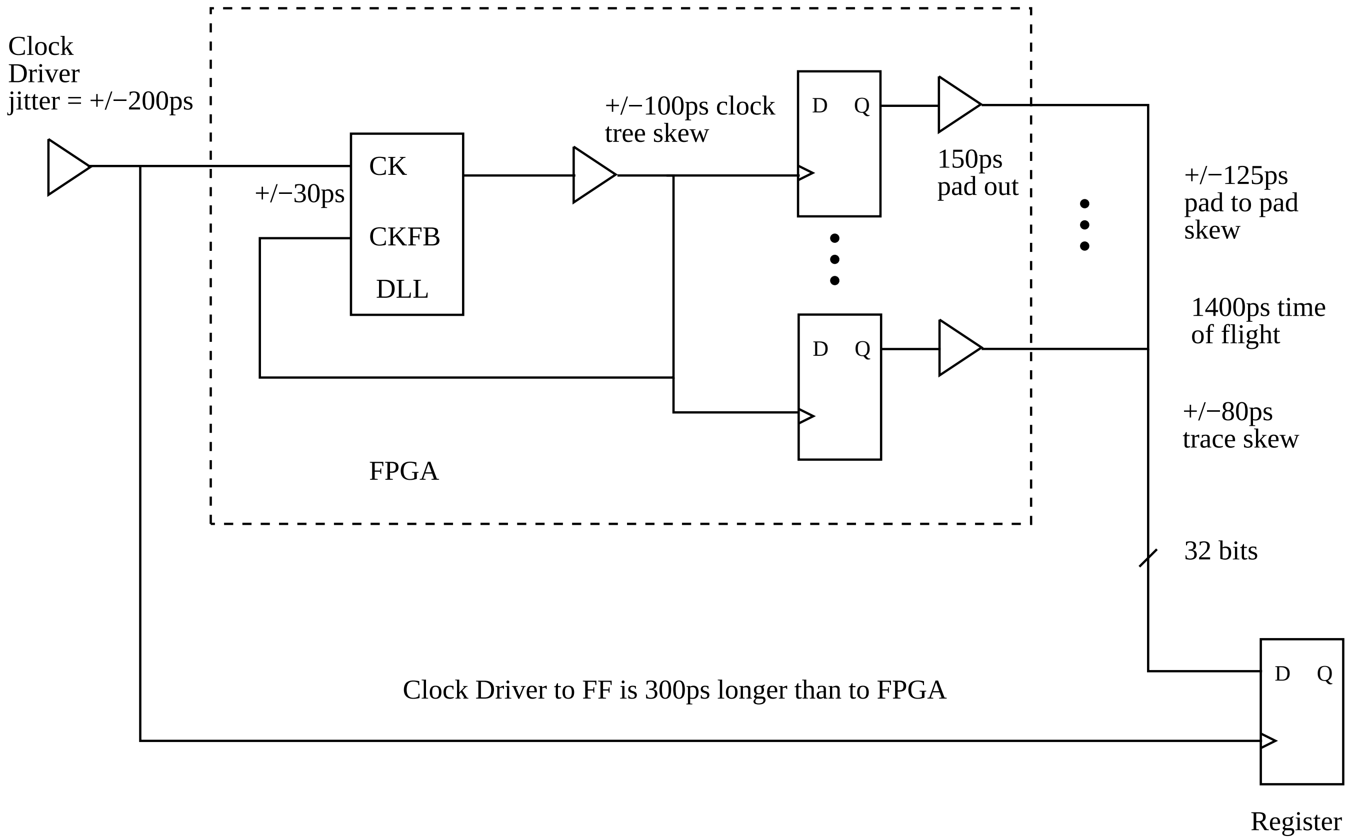
[2 marks] (b) Draw timing diagrams to show the timing relationships between the clock and data for an SDR interface and a DDR interface using a source synchronous clocking approach.

[2 marks] (c) What are the advantages/disadvantages of these two interface approaches?

Question 2 continued…

[4 marks] (d) Draw the circuit configurations for an SDR source synchronous interface showing the components, connections of the components and signals that you would need in and between the transmitting and receiving chips. Assume that the data is to be transmitted from flip flops in the transmitting chip to flip flops in the receiving chip.

3. Consider the circuit shown below:



From the data sheets you have also gathered the following information about the flip flops:

$$\begin{aligned} t_{\text{setup}} &= 0.8ns \\ t_{\text{hold}} &= 0.6ns \\ t_{\text{ClockToQ}} &= 0.2ns \end{aligned}$$

[5 marks] (a) What is the minimum clock period for this configuration? Assume that hold time is okay for now. First state the condition(s) you must satisfy in words, so I can understand what you are trying to do, before working out the numbers. State any assumptions you are making.

Question 3(a) continued. . .

[5 marks] (b) The difference in flight time from the clock driver to the FPGA and from the clock driver to the flip flop is shown as 300ps. At what value of this flight time would the flip flop hold time begin to be violated? Again, state the condition(s) you must satisfy in words first, and state any assumptions you are making.

4. You are tasked to develop a network intrusion detection ASIC that takes packets from an input gigabit data link, filters the packets for nasty things and outputs the filtered packets to an output gigabit data link. The input interface has a SERDES that takes the input serial data stream and converts it to a 32-bit parallel data stream and a data clock, which runs at 31.25 MHz ($32 \times 31.25 = 1000$). The data clock can be used to directly capture the data in flip flops. The output interface is a 32-bit parallel data port that must be clocked at 31.25 MHz.

[7 marks] (a) Show the design for your chip assuming the core logic of your chip runs at 100MHz.

You do not have to design the core logic at this time except for possibly the interfaces to the I/O logic. Assume the intrusion detection logic is a black box. You will have to show how you reliably move data from the input to the core, and from the core to the output by showing the necessary circuits.

Assume that you have a library of standard synchronous and combinational logic elements, memories, shift registers, FIFOs, adders, and multipliers.

Question 4 continued. . .

[3 marks] (b) You are considering running your core logic also at 31.25 MHz but using a local oscillator, i.e., not the data clock provided from the input interface What issues would you run into? How could you avoid them?