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Student Number:

University of Toronto
Faculty of Applied Science and Engineering

Test II – April 2007
BA 2155

ECE532S – Digital Systems Design

Examiner – Paul Chow

1. There are 5 questions and **9** pages. Do **all** questions. The total number of marks is 45. The duration of the test is 50 minutes.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. **No calculators or other computing devices allowed.**
4. Closed book. No aids permitted.

1 [10]	
2 [10]	
3 [10]	
4 [10]	
5 [5]	
Total [45]	

1. Starting with some short answer questions:

[2 marks] (a) Define *jitter* in the context of timing analysis for digital signals.

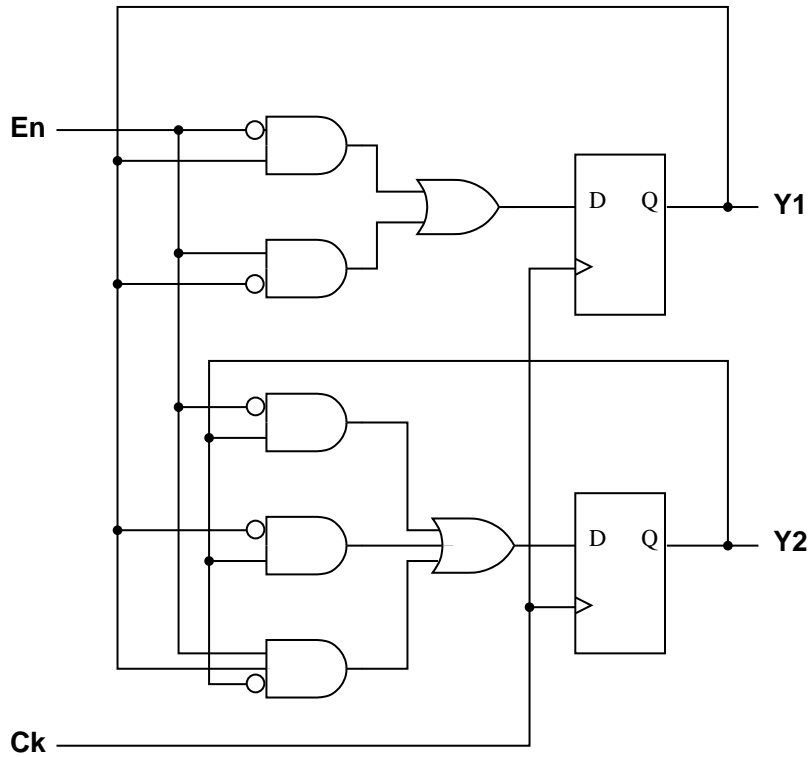
[2 marks] (b) What is the main advantage of embedding the clock signal into a serial data stream?

[2 marks] (c) What happens during the *place and route* phase of an FPGA CAD flow?

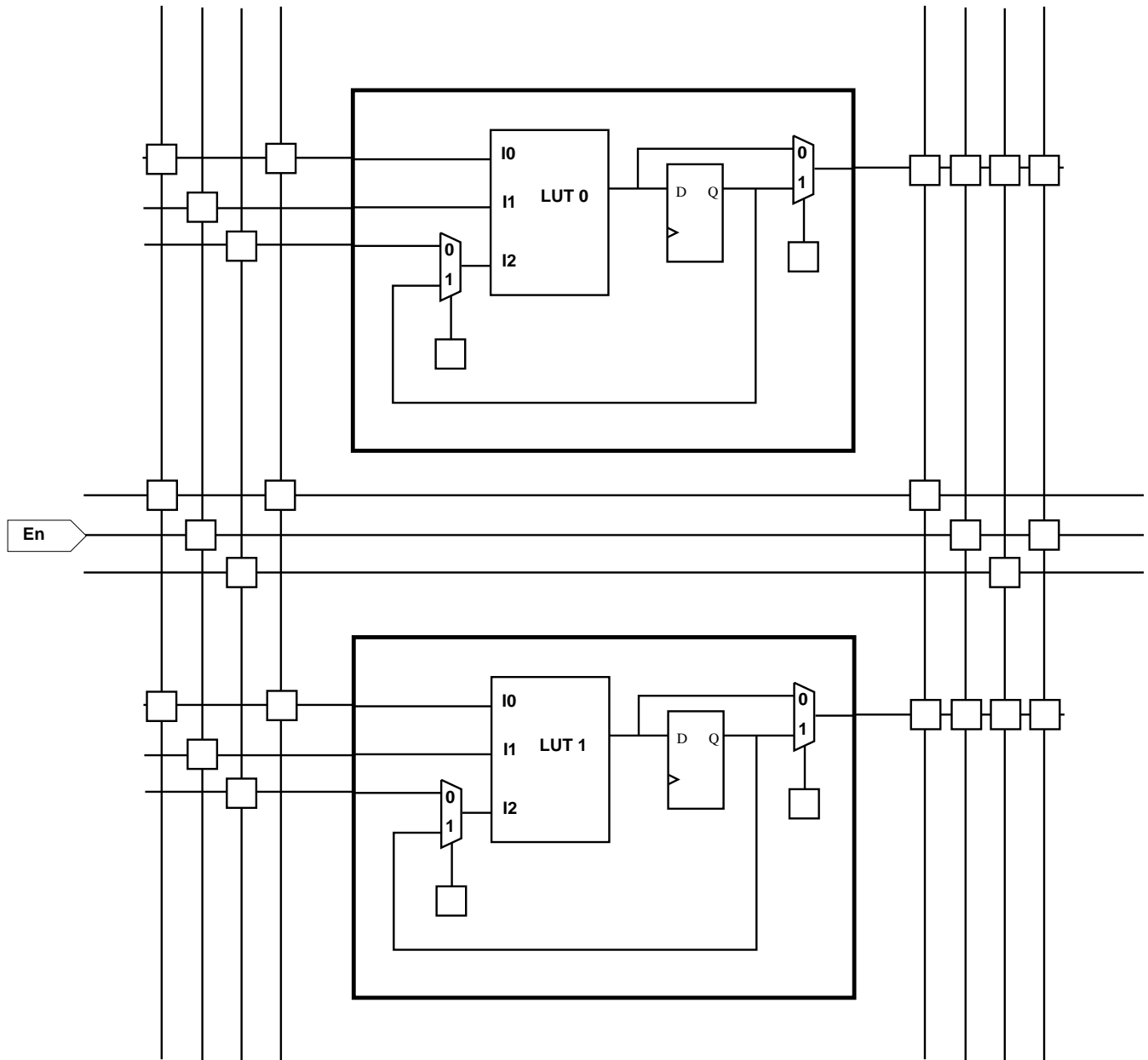
[2 marks] (d) Describe a BGA chip package.

[2 marks] (e) What is 8B10B coding used for?

- [10 marks] 2. Map the circuit shown below onto the FPGA blocks shown on Page 4. The small boxes in the FPGA diagram represent programming cells. For the multiplexers, enter a **0** or **1** in the box to select the respective input. For the boxes at wire intersections, enter an **X** to indicate a connection. The input **En** for the circuit is available on the labeled horizontal wire. The contents of the lookup tables are to be entered in the table on Page 5. You do not have to route the clock signal or route the outputs to any specific place.



Question 2 continued...

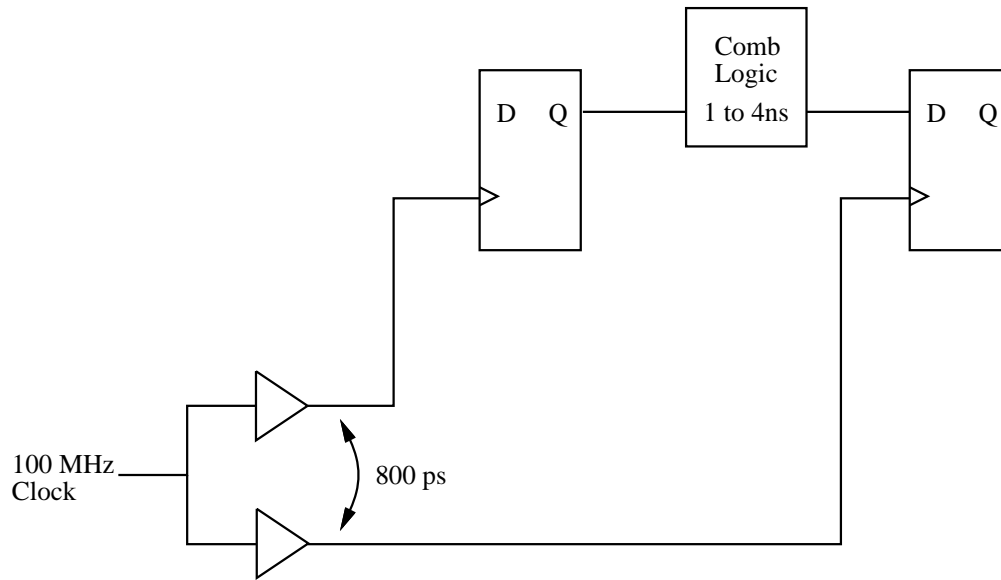


Question 2 continued...

Enter the contents to be loaded into the LUTs (lookup tables) of the FPGAs in the following table. The table has two blank columns corresponding to **LUT 0** and **LUT 1**.

I2	I1	I0	LUT 0	LUT 1
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[10 marks] 3. Consider the circuit shown below:



From the data sheets you have also gathered the following information about the flip flops:

$$\begin{aligned}t_{\text{setup}} &= 0.9ns \\t_{\text{hold}} &= 0.3ns \\t_{\text{ClockToQ}} &= 0.4ns\end{aligned}$$

The clock tree has a maximum skew of $800ps$, i.e., the phase of any one branch could be ahead or behind the other by $800ps$.

The clock source is a 100 MHz clock, or $10ns$ period with a jitter of $300ps$.

There is a delay of 1 to $4ns$ accounting for the combinational logic and the wire delay for the data travelling between the two flip flops. The range of delay means that the value could change as fast as $1ns$ or as slow as $4ns$.

Being a very conservative designer, you also like to add $500ps$ of timing margin to all of your calculations.

Determine whether the circuit will operate correctly (assuming that you include the timing margin) by checking the *setup* and *hold* times for the receiving flip flop in the above circuit.

Question 3 continued...

[5 marks] 4. (a) What is the advantage of using a *source synchronous* interface over a conventional *synchronous* interface?

[5 marks] (b) Show the basic model for a *source synchronous* interface. In particular, on the receiver side, be sure to show how the received data is clocked and clearly indicate all clock domains.

- [5 marks] 5. It is a good idea at the end of a project to do a postmortem where you reflect on what went right and what went wrong. The outcome should be a list of *lessons learned* for the next project. I would like to compile a list of these and post them (anonymously) on the course web page for future classes to read. Full marks will require responses that demonstrate an understanding of good design practice.

What are the three most important pieces of advice you would give to someone starting a project next year that would help them to be successful?