

Print:

First Name: Last Name:

Student Number:

University of Toronto
Faculty of Applied Science and Engineering

Test II – April 2008
BA 2139

ECE532S – Digital Systems Design

Examiner – Paul Chow

1. There are 4 questions and **9** pages. Do **all** questions. The total number of marks is 40. The duration of the test is 50 minutes.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. **Faculty approved calculators are permitted.**
4. Closed book. No aids permitted.

1 [10]	
2 [10]	
3 [10]	
4 [10]	
Total [40]	

1. Starting with some short answer questions:

[2 marks]

(a) Define *skew* in the context of timing analysis for digital signals.

[2 marks]

(b) What is the function of a CDR circuit in a high-speed serial transmission link?

[2 marks]

(c) What happens during the *technology mapping* phase of an FPGA CAD flow?

[2 marks]

(d) A DLL will not propagate input jitter to the output. Explain why this is true or false.

[2 marks]

(e) In 8B10B coding, why do some symbols have two different representations and how do the representations differ?

[10 marks] 2. Map the circuit shown below onto the FPGA blocks shown on Page 4.

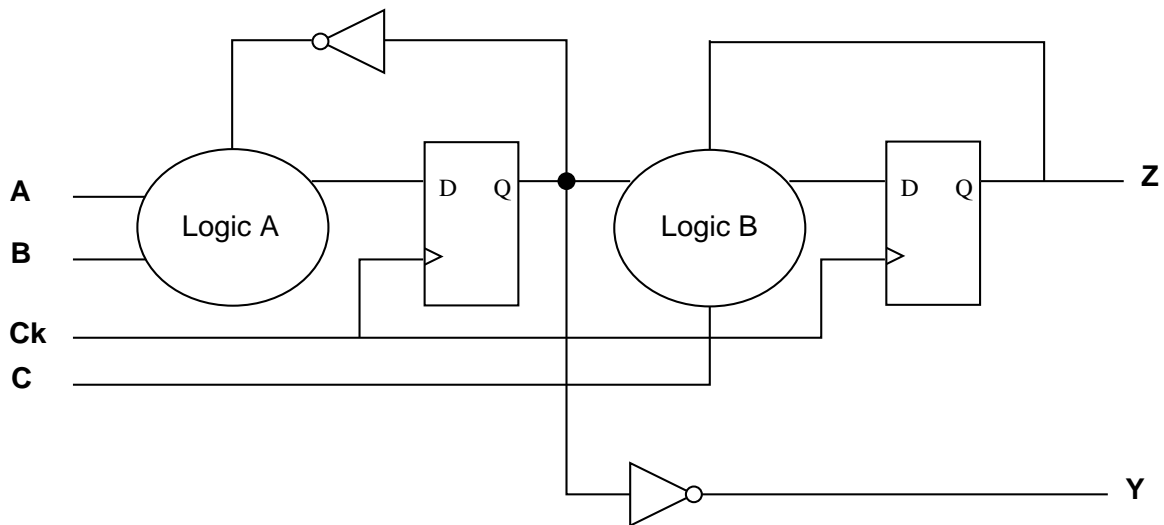
The small boxes in the FPGA diagram represent programming cells. For the multiplexers, enter a **0** or **1** in the box to select the respective input. For the boxes at wire intersections, enter an **X** to indicate a connection between the horizontal and vertical wires. Without a connection, the wires simply cross, but do not connect.

The inputs **A**, **B** and **C** for the circuit are available on the labeled horizontal wires.

The outputs, **Y** and **Z** only need to be connected to one of the routing tracks.

The contents of the lookup tables are to be entered in the table on Page 5.

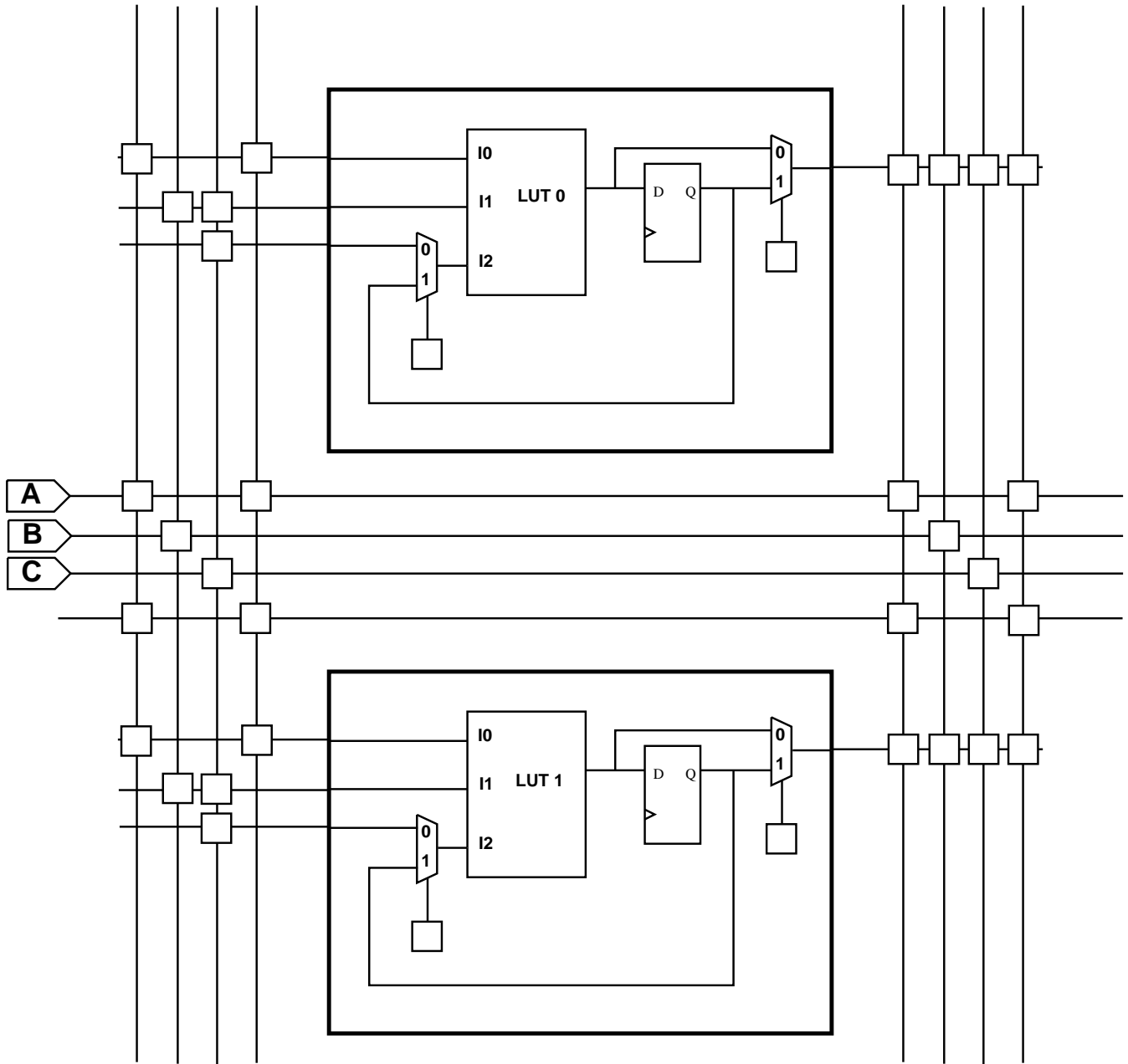
You do not have to route the clock signal.



Logic A implements the function: $A\bar{B}Y + AB + \bar{Y}\bar{A}B$

Logic B implements the function: $CY\bar{Z} + \bar{C}Z$

Question 2 continued...



Question 2 continued. . .

Enter the contents to be loaded into the LUTs (lookup tables) of the FPGAs in the following table. The table has two blank columns corresponding to **LUT 0** and **LUT 1**.

I2	I1	I0	LUT 0	LUT 1
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

3. Your task is to build a source synchronous 32-bit bus interface.

[5 marks]

(a) Draw a model of this interface. Explain how it works.

Question 3 continued. . .

[5 marks]

- (b) List all of the parameters you require to analyse the timing of the interface and show how you would use them to determine the maximum speed of your interface.

Being a very conservative designer, you also like to add $500ps$ of timing margin to all of your calculations.

State any assumptions, if you need to make any.

- [5 marks] 4. (a) Explain the difference between a *single data rate (SDR)* interface and a *double data rate (DDR)* interface? Include timing diagrams.

[5 marks]

- (b) Show the basic model for a *DDR* interface as described in class using *DDR* flops. In particular, on the receiver side, be sure to show how the received data is clocked and clearly indicate all clock domains.