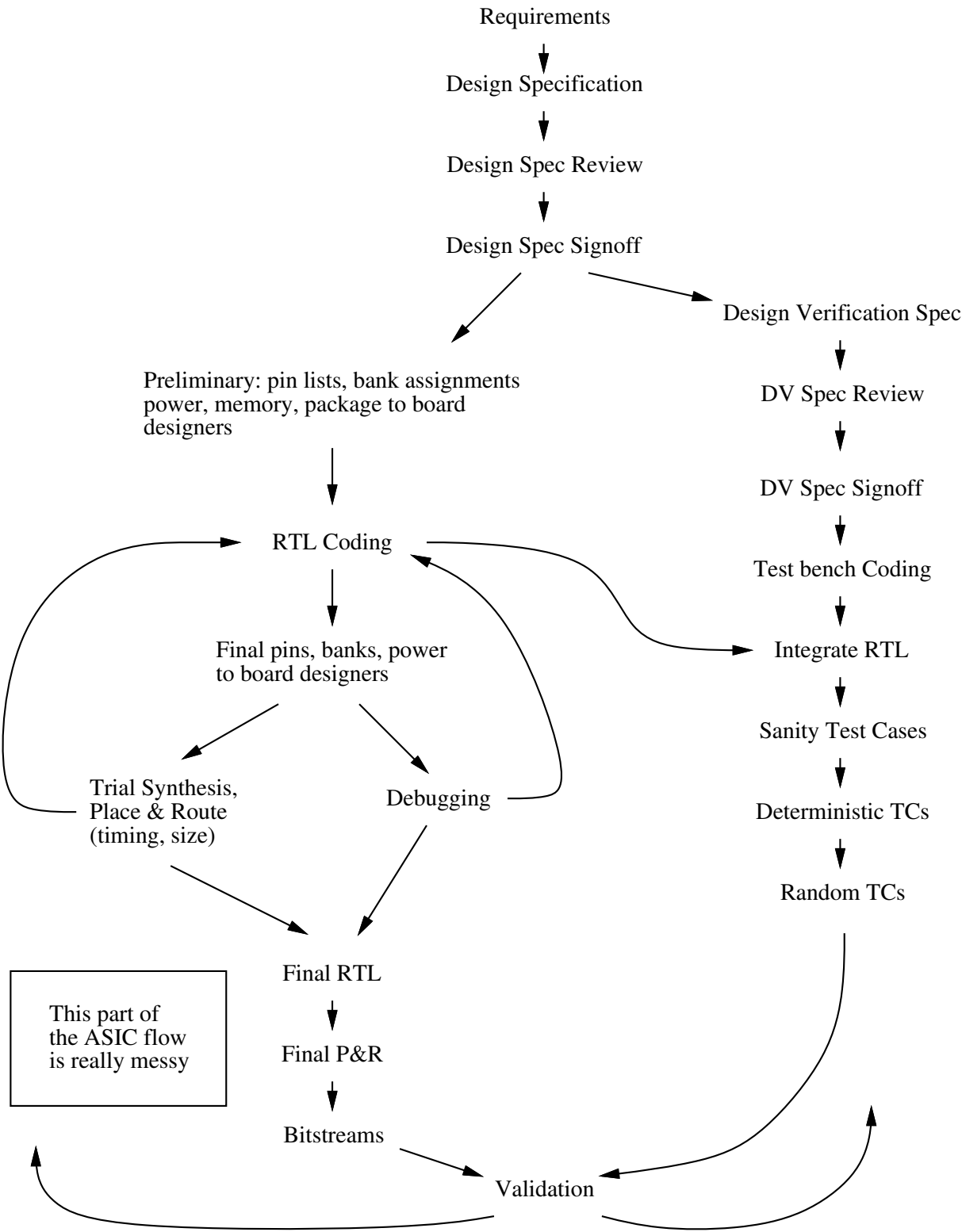FPGA Design and Verification Flow (High Level View)