A Field-Programmable
Mixed-Analog-Digital Array

by

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A Thesis submitted in conformity with the requirements
for the degree of Master of Applied Science in the
Department of Electrical Engineering,
University of T oronto

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Master of Applied Science, 1994

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Abstract

The trend in VLSI towards single-chip systems leads to the integration of analog and digital functions on a single chip. Field-programmable devices are likely to follow the same trend. Currently, there are many digital field-programmable devices in existence, and more recently analog arrays have been developed; however, there are no field-programmable mixed-analog-digital devices. This thesis describes the design and implementation of a Field-Programmable Mixed-Analog-Digital Array. The design contains a field-programmable analog array, a field-programmable gate array, and a mixed-signal interface that includes analog-to-digital and digital-to-analog converters.

The novel concept of reconfigurable data converters is introduced for use in a field-programmable system. The resource and architectural requirements for the Field-Programmable Mixed-Analog-Digital Array is determined by analyzing a set of mixed-signal circuits. Furthermore, the practical issues involved in the design of mixed-signal integrated circuits are addressed.

Acknowledgments

I would like to take this opportunity to thank my thesis supervisors, Professors Paul Chow and Glenn Gulak, for their guidance, advice, support, and encouragement throughout the course of my studies.

I am also indebted to Edward Lee for his patience in answering all my questions about his chip, and sharing his analog design experience.

As well, I would like to thank all of my friends who have made graduate school enjoyable. I especially thank David Karchmer, Ramin Khoini-Poorfard, Lysander Lim, Tony Ngai, Ali Sheikholeslami, Qiang Wang, David Yeh for their friendship, encouragement, and technical advice.

I would also like to thank Bryn Owen and Jaro Pristupa for their technical support.

I wish to express my sincerest gratitude to my parents who have always supported my studies.

Finally, and most importantly, I would like to thank Carol for her unwavering love and support.

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Chapter **1**

Introduction

1.1 Thesis Motivation

The trend in VLSI towards single-chip systems leads to the integration of analog and digital functions on a single chip. The reduction in the number of chips leads to reductions in board space, interconnections, and most importantly, cost. Field-programmable devices are likely to follow the same trend due to the rapidly expanding market for mixed-analog-digital devices [B&B89]. Currently, there are many commercial Field-Programmable Gate Arrays (FPGAs) available to implement digital circuits [Agar94] [Brit93] [Brow92] [Hsie90]. More recently, there has been research into the area of Field-Programmable Analog Arrays (FPAAs) [Lee91] [Lee92]. However, there has been no attempt to combine these two technologies to produce a single mixed-signal chip.

This thesis describes the design and implementation of a field-programmable mixed-analog-digital array by combining existing analog and digital arrays designed at the University of Toronto, and providing an interface to connect them.

1.2 Mixed-Signal Systems

Although large systems today consist mostly of digital logic, they must still interface with a largely analog world. To build a single-chip system, these interfaces must be included on chip.

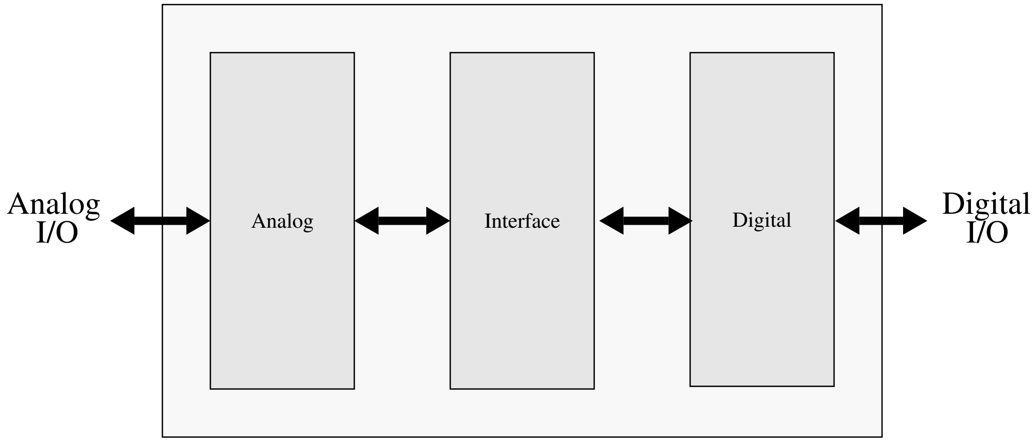

Figure 1-1: Block diagram of a mixed-signal chip.

Mixed-signal systems can be found in a wide variety of applications such as instrumentation, control, telecommunications, etc. Figure 1-1 shows a block diagram of a mixed-signal chip that consists of an analog block, a digital block, and a mixed-signal interface that contains circuits to perform data conversion between them.

There has been considerable research devoted to mixed-signal chips to benefit from the cost savings that accompanies a higher level of integration. This savings is a direct result of the reduction in the component count, which in turn leads to added savings in board space and interconnections. A beneficial side effect of these reductions is an increase in the reliability of the overall system. There are several other advantages that accompany the incorporation of both analog and digital functions on the same substrate. Since the interconnections between the two functions do not leave the chip, significant improvement in speed and reduction in power consumption can be achieved. This power savings can be attributed directly to the reduction in the number of pins. These advantages are particularly important in mobile applications where power and size are major concerns. As a result, the market for mixed-signal devices is growing at a faster rate than the market for either analog or digital devices [B&B89].

Performance improvements obtained by using technologies such as BiCMOS (which can use bipolar devices where speed, low noise, and current drive are required, and CMOS devices where high density and low power are required) will help drive the market for mixed-signal chips [Cope91].

1.3 Reconfigurability in a Mixed-Signal System

One reason for the proliferation of field-programmable devices is the fast prototyping capability that they provide. This is particularly important in analog circuits where traditionally prototypes were built using discrete components on breadboards and then transferred to silicon. However, this prototyping method introduces parasitic capacitances and inductances that are several orders of magnitude larger than those on silicon. These parasitics lead to sources of error that can be intolerable, especially at higher speeds.

An added feature of a reconfigurable mixed-signal system is that it can serve as a design tool to determine the best partitioning of analog and digital functions. This is particularly important in large systems where the signal processing task is divided between the analog and digital domain, and the boundary is placed at the most appropriate position according to the complexity of the processing required along the processing chain [Malo91a].

1.4 Thesis Objectives

Two conceptual views of a field-programmable mixed-analog-digital architecture are shown in Figure 1-2. The first view, shown in Figure 1-2(a), contains an analog array and a digital array with some interconnect. Any signal conversion that is required can be built from the resources available in the two arrays. An alternative view, shown in Figure 1-2(b), provides dedicated converters to perform signal conversions. The former view offers greater flexibility at the expense of a reduction in speed and an increase in area. To investigate field-programmable mixed-analog-digital architectures, a chip called MADAR[1], which includes dedicated converters will be designed and implemented. Since there have been no implementations of this kind to date, the best design is yet unknown. This implementation will help explore the system requirements, and design issues involved in field-programmable mixed-analog-digital arrays.

The design of MADAR is constrained by the existing analog and digital array designs. In this thesis, we will concentrate on building an interface to interconnect the two arrays. The speed and resolution of the data converters in this interface must be designed to be compatible with the analog and digital arrays. Furthermore, MADAR must be constrained to a reasonable size for

1. **M**ixed-**A**nalog-**D**igital **A**rray that's **R**econfigurable. The word MADAR in Persian means circuit.

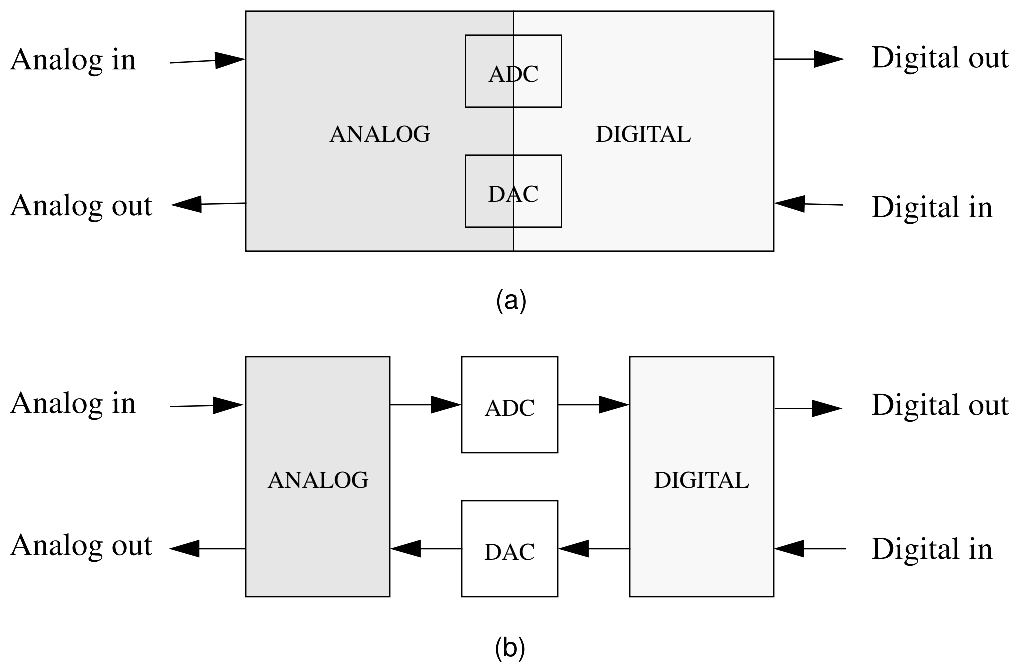

Figure 1-2: Conceptual views of mixed-signal architectures: (a) array architecture with field-programmable resources capable of constructing data converter as required; (b) array architecture with dedicated data converters.

implementation while still have enough functionality to demonstrate the feasibility of such a device.

1.5 Thesis Organization

This thesis consists of seven chapters. Chapter 2 provides a summary of previous work on field-programmable analog and digital arrays at the University of Toronto. Chapter 3 describes the demonstration circuits used to determine the architecture of MADAR. Also, the mixed-signal interface will be described along with the design issues involved in mixed-signal systems. Chapter 4 details the design and implementation of the reconfigurable digital-to-analog converter. Chapter 5 describes the design and implementation of the reconfigurable analog-to-digital converter. Chapter 6 presents the overall specifications for the MADAR chip, and an example of how a circuit can be embedded into it. Finally, Chapter 7 concludes this thesis and presents some suggestions for future work.

Chapter 2

Background

2.1 Introduction

The following two sections will describe previous work, done at the University of Toronto, on a field-programmable digital array and a field-programmable analog array. The layouts of these arrays will be used as building blocks in the construction of MADAR to reduce the layout effort required. These existing designs will influence the overall design and implementation of MADAR, particularly the mixed-signal interface. Discussion of this interface will be deferred until the next chapter.

2.2 Digital Array

A 1.2 µm CMOS FPGA, called LEGO, was designed and implemented to better understand the issues related to the design and architecture of digital FPGAs [Chow93]. The general architecture of LEGO is shown in Figure 2-1. The logic block (L) contains lookup tables that are used to implement the functionality of the circuit. The connection block (C) provides the connectivity between the logic blocks and the adjacent channels while the switch block (S) provides connectivity between the horizontal and vertical channels. A single tile, which contains one logic block, two connection blocks, and a switch block is constructed by combining smaller building blocks called mini-tiles using a novel layout technique. This layout method not only reduced the

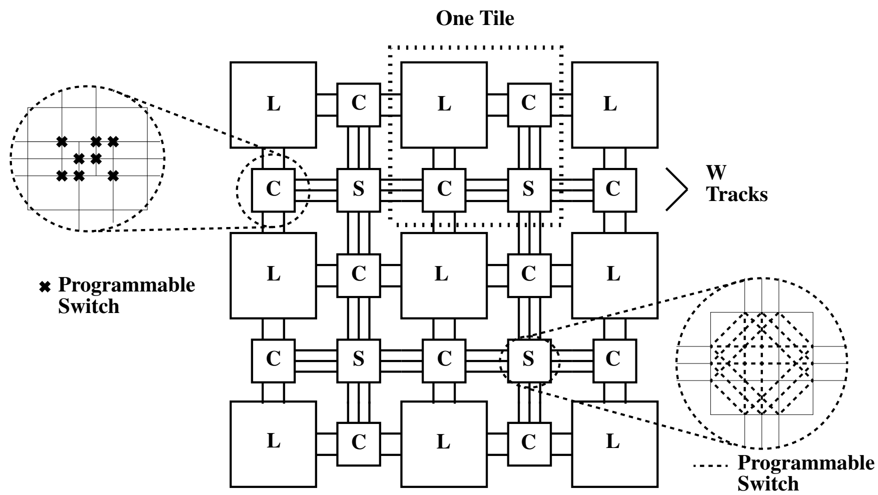

Figure 2-1: General architecture of LEGO.

time spent on custom layout, but also provides another level of customization through the addition of vias to create hardwired links in the logic block, and segmented routing in the channels.

Each tile in LEGO consists of four 4-input lookup tables, four D flip-flops, and connection resources for sixteen tracks in both the horizontal and vertical directions. The tracks are bidirectional and have variable segment lengths. Segmented routing is used to reduce the effect of routing delay due to the programmable switches by having routing tracks of different length. The track segmentation distribution in LEGO is as follows: nine of sixteen are 1-segments, four are 2-segments, and three are 3-segments. The four lookup tables in the logic block contain hardwired links (indicated by the solid lines) with the topology shown in Figure 2-2. Hardwired links replace the programmable switches used to connect lookup tables by a metal wire, thus reducing the delay associated with programmable interconnect. In LEGO, the interconnect consists of n-channel pass transistors.

SRAM cells are used to store the programming information that determines the logic function, and controls the switches that perform the routing and connection functions. The SRAM cells form a rectangular array that can be programmed in a serial-parallel fashion using a horizontal and a vertical shift register. The programming word is serially shifted into the horizontal shift register. The word is then loaded into the row selected by a vertical shift register. An additional

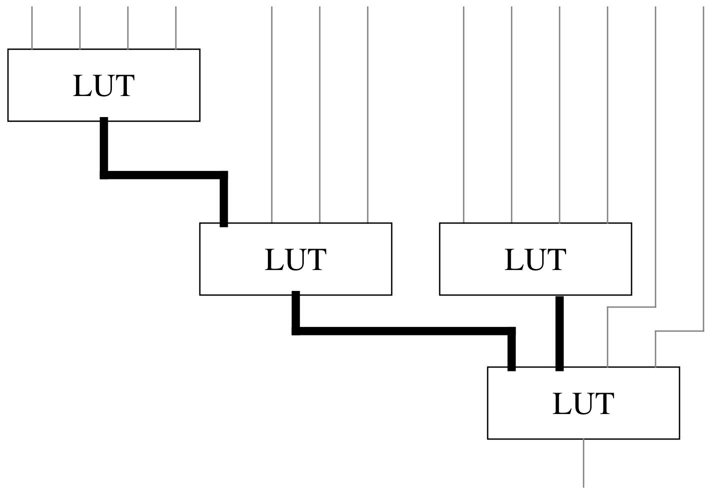

Figure 2-2: Lookup table topology used in LEGO.

shift register is used to program the multiplexers that connect the tracks to the external pins. It should be noted that all the LUT outputs that drive the tracks are disabled during programming.

2.3 Analog Array

An analog array must contain all the major components required to realize analog circuits. These include opamps, resistors, capacitors, and diodes, and a means to interconnect them. A field-programmable analog array (FPAA) was designed and implemented in a 1.2 µm CMOS process [Lee94]. Its architecture is shown in Figure 2-3, and contains all the necessary building blocks mentioned above. The opamps are located on the left side of the figure while the resistors, diodes, and capacitors are located along the bottom. A crossbar interconnect structure is used to connect these circuit elements with switches that are controlled by the contents of a shift register.

The configurable analog block (CAB), shown in Figure 2-4, contains a fully-differential opamp plus two sets of feedback capacitors that can be used to increase the tuning range of the RC time constants. One set contains 15 pF capacitors, and the other set contains 2.5 pF capacitors. Furthermore, the compensation capacitor in the opamp can be disabled to realize a fast comparator. The measured performance of the opamp is summarized in Table 2-1.

The resistors and the interconnection network are realized using MOSFET transconductors to create an area-efficient and parasitic-insensitive design. A four-transistor transconductor, shown in Figure 2-5(a), provides a way of realizing linear parasitic insensitive circuits through transistor

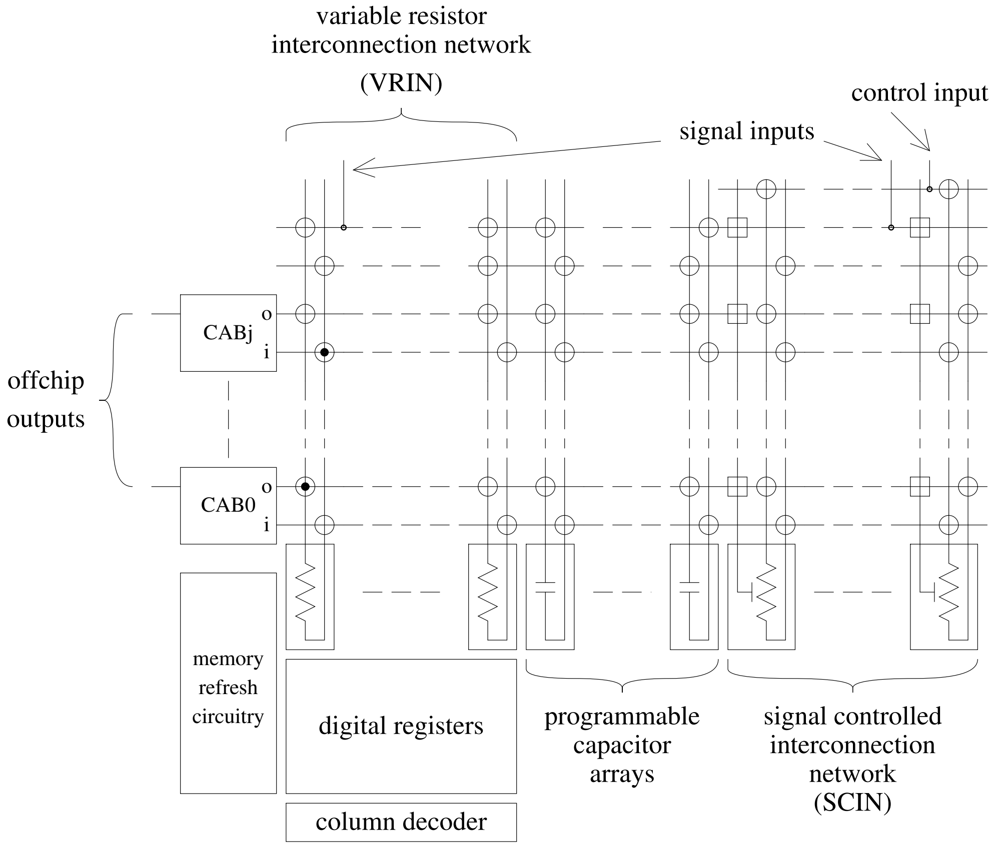

Figure 2-3: FPAA architecture.

matching and differential signalling [Dupu90]. The small-signal transconductance, G, when all the transistors are operating in the linear region, is given by

$$G = \mu C_{ox}\frac{W}{L}(V_{g1} - V_{g2}) \tag{2-1}$$

$$\text{for } v_1, v_2 \geq max\,[V_{g1} - V_T, V_{g2} - V_T]$$

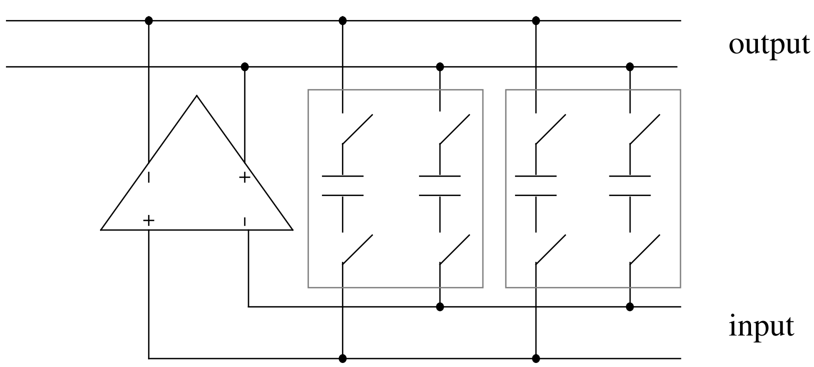

Figure 2-4: Configurable analog block used in FPAA.

Item	Value
Unity Gain Frequency	3 MHz
Slew Rate	7.5 V/µs
Open loop gain	> 60 dB
Power Dissipation	12 mW

Table 2-1: Experimental results of the opamp with 1 MΩ and 38 pF loading.

The transconductor can be used to implement either a switch element or a resistive element in an analog array; however, a design that uses transconductors as switches in the interconnection network would be area-inefficient due to the W/L ratios required and the circuitry needed to generate V_{g1} and V_{g2}. Figure 2-5(b) shows a modified transconductor consisting of a central part and two terminations with harmonic distortion and frequency response that is comparable to the original four-transistor transconductor. The central part, located at the bottom of the column in the variable-resistor interconnection network (VRIN), consists of long-channel transistors to realize large resistance values. The termination parts, used as connection switches in the crossbar

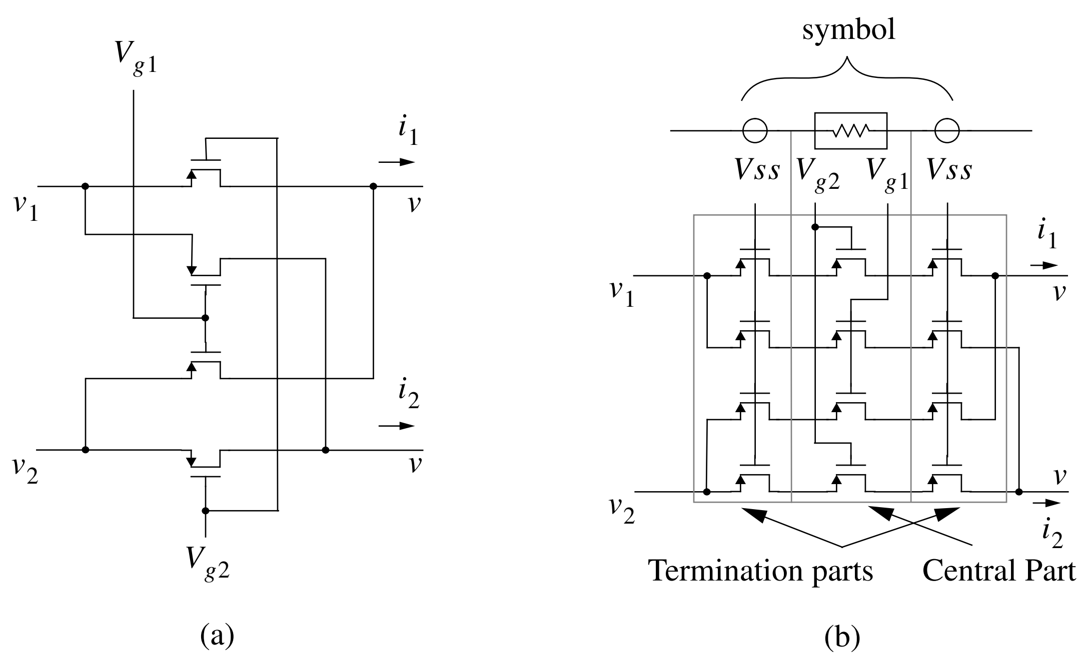

Figure 2-5: (a) Four-transistor transconductor (b) modified transconductor.

interconnect, consists of area-efficient short-channel transistors. Furthermore, the central part contains two sets of transconductors to realize both small and large resistors. Each column realizes a single transconductor, hence the number of resistors is determined by the number of columns in the network. A precise sample-and-hold (S/H) circuit is used to implement a multiple-value memory, which stores the analog voltage that programs the resistance values in the central part of the transconductor. The resistance values of the transconductors are stored in ten-bit registers; they are converted to analog values by multiplexing to an on-chip D/A. The analog value is then used to refresh the S/H circuit every 0.5 ms.

The signal-controlled interconnection network (SCIN) consists of the same modified transconductor used in the VRIN, but can be controlled by either the CAB outputs or by external inputs. As will be shown later, the SCIN is a crucial interconnect element in an analog-digital interface. A level shifter is also provided in the central part of the SCIN that shifts the voltages into the range required for the transconductors to maintain linear operation.

The FPAA also provides connection columns that contain passive elements such as diodes and capacitors. The capacitance values in the programmable capacitor array (PCA) is determined by a six-bit register.

A single tile of the analog array consists of the following elements: eight columns in the VRIN, six columns in the SCIN, three columns in the PCA, and four CABs. Two differential inputs are provided to both the SCIN and VRIN networks, and the differential outputs from all four CABs are accessible.

2.4 Summary

In this chapter, previous work on field-programmable digital and analog arrays that will be used to build MADAR have been discussed. The next chapter will describe the demonstration circuits used to determine the requirements for a field-programmable mixed-analog-digital array. Also, the architecture and the design issues involved in the implementation of MADAR will be discussed.

Chapter 3

Architecture

3.1 Introduction

This chapter describes the architecture of MADAR, which is arrived at through the analysis of a small set of mixed-signal circuits described in Section 3.2. The results from this analysis are used to determine the MADAR architecture, and the mixed-signal interface described in Section 3.3 and Section 3.4, respectively.

3.2 Mixed-Signal Circuits

To determine the architecture of a field-programmable mixed-analog-digital array, it is important to understand the requirements. Examples of mixed-signal circuits found in the literature are useful, but are too large and complex to be mapped into a prototype chip. This section contains a collection of smaller mixed-signal circuits, which offer insight into the resources that are needed in a mixed-signal system. A brief description of each circuit will be provided, and a summary of the resources and interconnections required will be tabulated at the end of this section.

The size of the circuits are constrained by the existing field-programmable designs described in the previous chapter. The main constraints to consider are the number of opamps in the analog array and the number of lookup tables in the digital array. A single analog tile contains four opamps while a single digital tile contains four lookup tables. For demonstration purposes, we have chosen to implement a chip that contains one analog tile and four digital tiles; thus, a total of four opamps and sixteen lookup tables will be available. Also, we will provide four data converters (two A/D converters and two D/A converters) for signal conversion between the analog and digital arrays. With these resources, we will be able to implement a variety of mixed-signal circuits and thus prove the feasibility of MADAR.

Simulation of these circuits was performed using Saber, a mixed-signal simulator that supports electrical-level, gate-level, and behavioral-level simulations [Anal92]. To reduce the simulation time, the digital circuitry was verified by either gate-level or behavioral-level simulation. The analog circuits, on the other hand, were simulated at either the behavioral level or the electrical level to provide greater detail and accuracy. The interface between the analog and digital simulations is handled by SABER 'hypermodels', which perform the necessary conversion between logical and electrical signals. A simulation example is provided in Chapter 6.

3.2.1 Sigma-Delta Analog-to-Digital Converter

Sigma-delta analog-to-digital converters (ADC) sample an analog input at a high speed, then digitally average and filter the data to produce a high-resolution digital output at a much lower frequency [Horo80]. Figure 3-1 shows a functional diagram of a simple first-order sigma-delta ADC. The converter consists of an analog modulator and a primitive digital filter. The analog modulator is basically a negative feedback loop that consists of the following components: a summer, an integrator, a comparator, and a 1-bit digital-to-analog converter (DAC). It tries to maintain a zero average voltage at the integrator output by balancing the input voltage with the average voltage from the 1-bit DAC. The resulting output is a stream of binary digits generated by the comparator; a binary one is generated when the integrator output is positive, and a binary zero is generated when it is negative. In this example, the digital filter consists of a counter that records the number of binary ones, which represents the average analog input signal during one complete cycle of the other counter. However, more complex digital circuitry is required to recover the analog signal with high resolution.

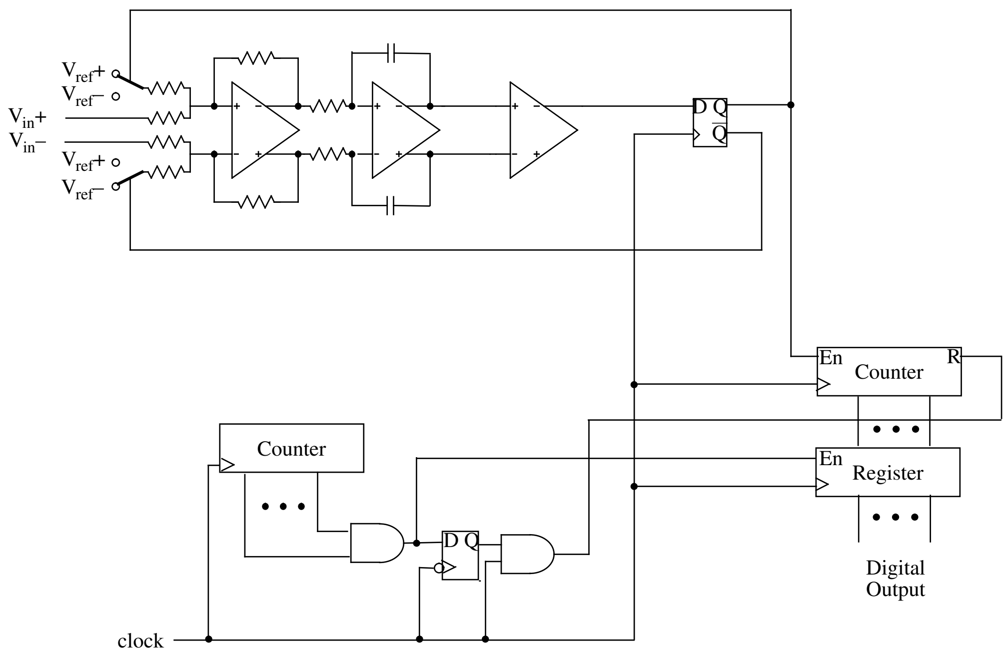

Figure 3-1: Sigma-delta analog-to-digital converter.

There are two connections between the analog and digital functions. The comparator in the analog part connects to the input of a flip-flop in the digital section, which is then fed back to the analog modulator to control the switches in the 1-bit DAC.

3.2.2 Dual-Slope Analog-to-Digital Converter

A dual-slope analog-to-digital converter, shown in Figure 3-2, is an example of an integrating converter that provides high resolution and accuracy but at low speeds [Greb84]. The circuit operation begins by closing switch S_r to reset the integrator. Then, the analog input V_{in} charges the integrating capacitor for a fixed time interval determined by the counter, and the voltage of the integrator proceeds to ramp up with a slope proportional to the input voltage. Next, the capacitor is discharged by a reference source V_{ref} of opposite polarity, and ramps down at a constant rate proportional to the reference source. When the integrator output reaches zero, the counter contains the digital equivalent of the analog signal, and is transferred to the register.

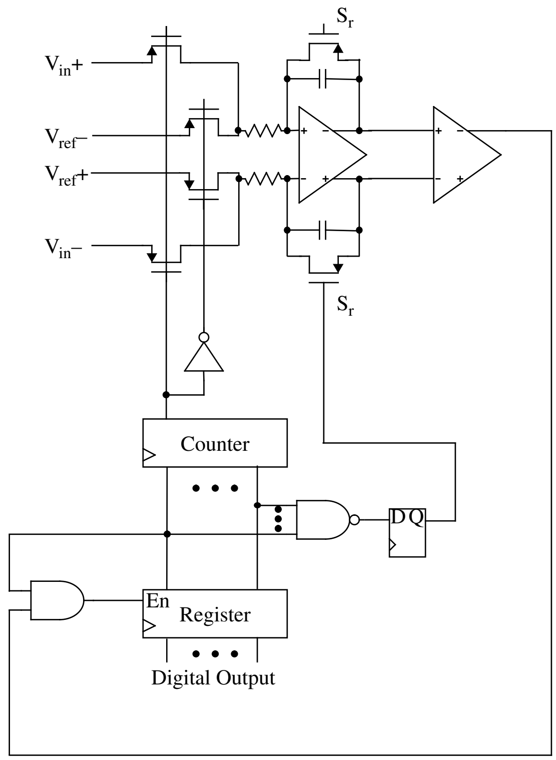

Figure 3-2: Dual-slope analog-to-digital converter.

The dual-slope ADC requires four connections between the analog and digital functions. A digital signal is used reset the integrator, and two others are used to control the switches that select the voltage to be integrated. The comparator in the analog part is used to enable the register.

3.2.3 Pulse-Width-Modulation Digital-to-Analog Converter

Pulse-width-modulation (PWM) techniques can be applied to realize oversampling digital-to-analog converters [Malo91b]. A functional diagram of a PWM DAC is shown in Figure 3-3. In the figure, a digital input is compared against the output of a counter running at a fixed frequency. The comparator generates a pulse whenever the digital input is greater than the value in the counter. In this way, the duty cycle of the resulting pulse width is equal to $n/2^m$, where n is the value of the digital input, and m is the number of bits in the counter. The output of the comparator is passed through a low-pass filter to obtain the average voltage of the pulse stream with m-bit accuracy. Several other methods can be used to obtain different distributions of the pulses, which can ease the filtering requirements. For example, the counter can be replaced by a

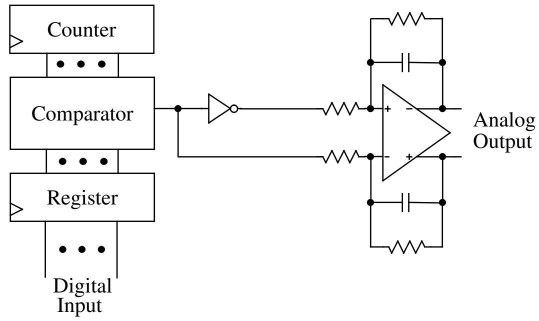

Figure 3-3: Pulse-width-modulation digital-to-analog converter.

pseudo-random number generator which results in a whiter output spectrum that can be filtered more easily.

This circuit requires a single connection from the digital to the analog section. The comparator output is fed directly to the low-pass filter in the analog portion. The rail-to-rail voltage of the comparator output, however, must be limited to keep the analog circuitry in the linear region of operation.

3.2.4 Noise Generator

The circuit shown in Figure 3-4 is used to generate band-limited white Gaussian noise. In analog systems, noise immunity can be determined by injecting white noise into the circuit and performing a set of measurements. Digitally-generated noise sources are particularly attractive since they can generate noise of known spectrum and amplitude without experiencing the interference and pickup problems associated with analog noise generators that use diodes or resistors [Horo80].

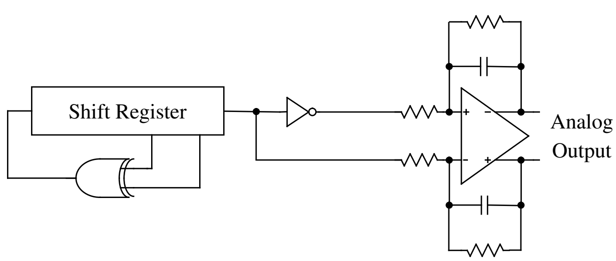

Figure 3-4: Noise generator.

The circuit consists of a linear feedback shift register (LFSR) and a low-pass filter. An LFSR can generate a pseudo-random sequence that repeats only after 2^m clock cycles, where m is the number of bits in the shift register. One bit from the LFSR can then be fed into a low-pass filter with a cutoff frequency that is several orders of magnitude less than the digital clock frequency. The resulting output of the low-pass filter is a noise voltage with a flat power spectrum in the pass band of the filter.

This circuit requires a single connection from the digital to the analog array. Again, this voltage must be reduced so that the analog circuitry remains in the linear region of operation.

3.2.5 Phase-Locked Loop

The phase-locked loop (PLL) is a very useful building block that can be used to perform many functions in a variety of applications (e.g. FM detection, tone decoding, frequency synthesis, synchronization) [Greb84]. Figure 3-5 shows a PLL that consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator (VCO). The phase detector in this circuit is simply a digital exclusive-OR gate, although more complex phase detection techniques exist. When the input frequency, f_{in}, and the VCO frequency, f_{vco}, are out of phase, the phase detector generates an error voltage that is proportional to their phase difference. This voltage is then fed into a low-pass filter, and the resulting signal is used to control the frequency of oscillation of the VCO.

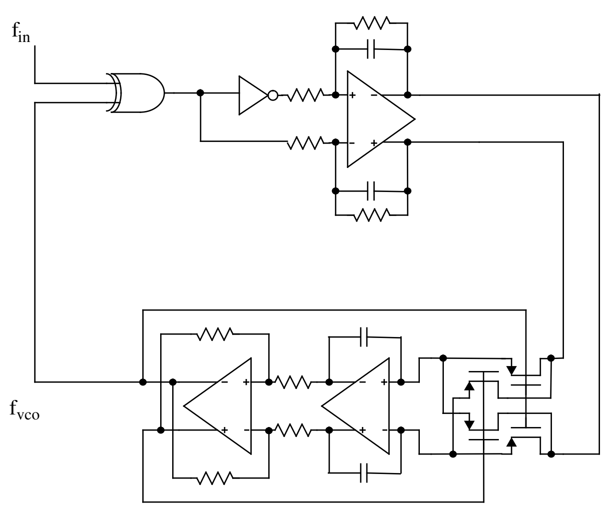

Figure 3-5: Phase-locked loop.

The post-filtered error voltage will tend to move the VCO frequency in the direction of the input frequency, if the two frequencies are sufficiently close. When f_{vco} becomes synchronized to f_{in} due to the feedback nature of the PLL, the PLL is locked onto the input signal frequency.

This circuit requires two connections between the digital and analog array. The output of the phase detector is fed directly into the low-pass filter, and the output of the VCO is fed into one of the phase detector's input terminals.

3.2.6 Automatic Gain Control

A number of applications contain automatic gain control (AGC) circuits that are used to maintain a stable output level despite variations in the input level. For example, AGC circuits are required on receiver chips used in digital transmission systems where the input level can vary by as much as 40 dB [Soin91]. A second example can be found in [Ohta90] where the concept is

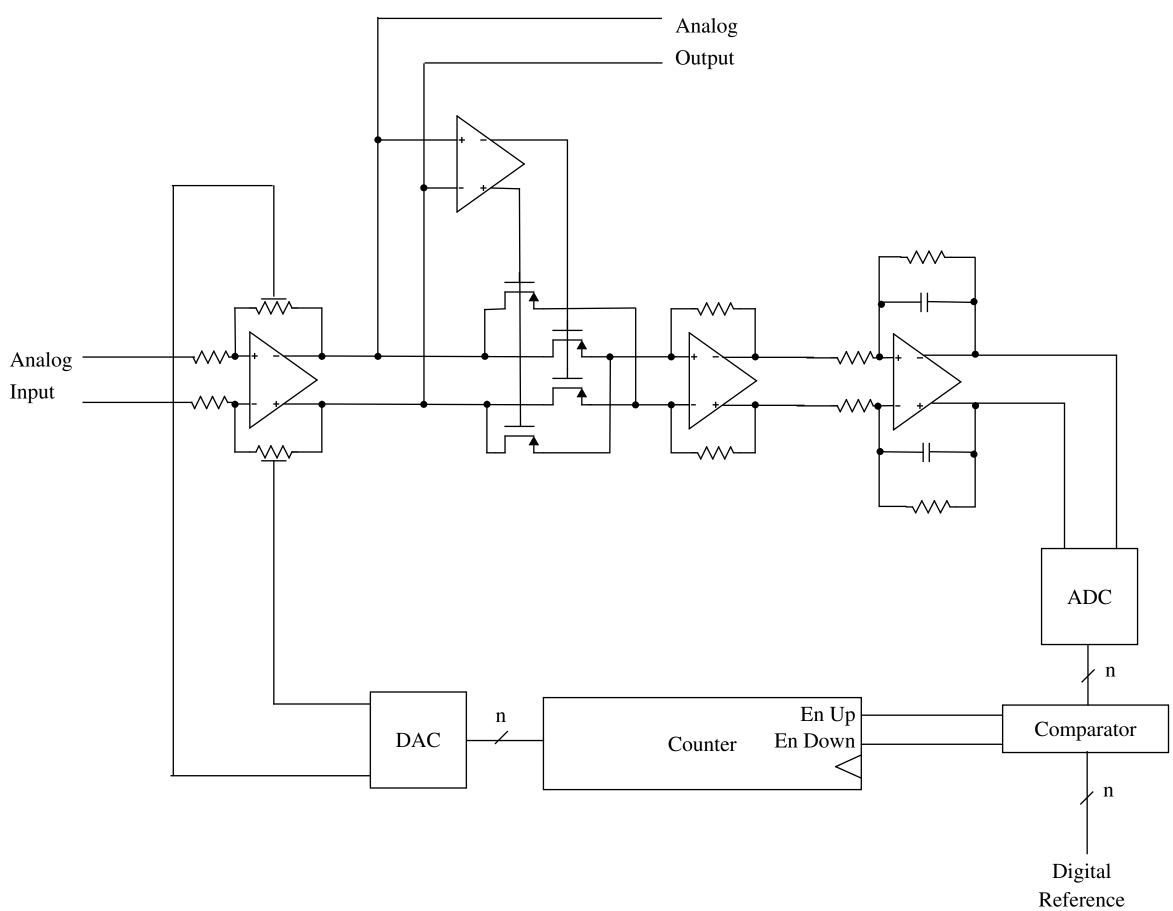

Figure 3-6: Automatic gain control circuit.

applied to an automatic color control (ACC) circuit that eliminates color flicker in digital television systems.

The analog path of the automatic gain control circuit, shown in Figure 3-6, consists of an opamp with a variable gain followed by a full-wave rectifier and an integrator. The output from the integrator is a measure of the output level. It is converted into a digital signal by the ADC, and compared against a digital reference. If the output level exceeds the reference, the digital control circuitry either increments or decrements the counter to bring the output level back to the reference. The DAC converts the digital counter value into an analog signal that controls the variable resistors and thereby adjusts the gain.

This circuit contains no direct connections between the analog and digital functions, instead, the connections are made through the two data converters.

3.2.7 Data Acquisition System

An important area in the field of instrumentation is the acquisition of data where measured data is usually acquired in analog form and then converted to digital form for display, storage, or transmission [Wolf83]. Often it is necessary for the analog signal to undergo some form of signal conditioning, such as amplification and filtering, before the final conversion to digital information. Figure 3-7 shows an example of a four-channel data acquisition system. Two channels are used to convert the measured analog signals to digital data following some signal conditioning. The other two channels operate in the reverse direction, and perform digital-to-analog conversion for display on analog meters. Multi-channel systems often include analog multiplexers to reduce the amount of circuitry for signal conditioning and data conversion. Digital multiplexers can be placed at the output to build single bus systems.

The data acquisition system shown connects the analog and digital sections via the data converters, hence there are no direct connections between the analog and digital functions.

3.2.8 Signal Processor

Signal processing in a mixed-signal environment proceeds along the path shown in Figure 3-8. Some initial pre-processing to remove the high frequency components is required to prevent aliasing of these components by the sampling that occurs during analog-to-digital conversion.

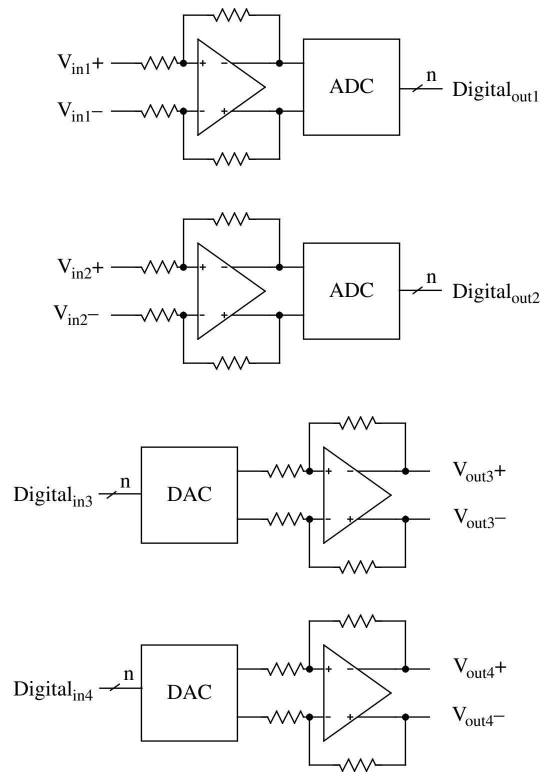

Figure 3-7: Data acquisition system.

Once the signal is converted to digital form, digital filtering can be performed. The digital-to-analog converter restores the data to analog form. Some final post-processing to smooth out the waveform from the DAC, and reject high frequency noise is required [Tsiv94].

The example shown in Figure 3-9 contains each of these processing stages. The analog input is fed into an anti-aliasing filter to remove the high frequency components. The output from the filter is converted into a digital signal by the ADC. The digital signal processing function is accomplished by averaging two consecutive samples of the digital signal to realize a simple low-pass filter. Next the signal is converted back to analog form by the DAC, and then passed through a smoothing filter to produce the final output.

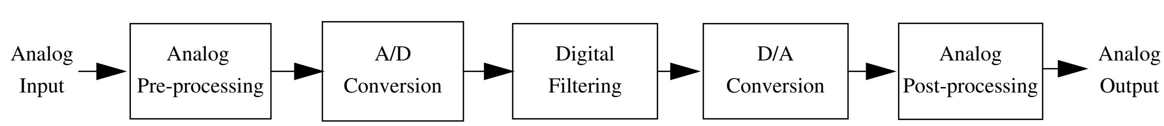

Figure 3-8: Signal processing in mixed-signal environment.

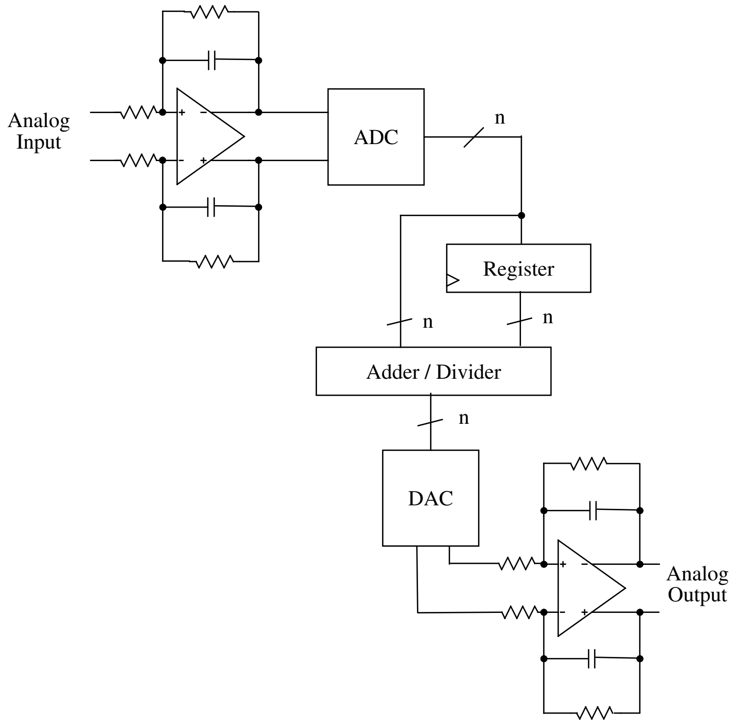

Figure 3-9: Signal processor.

3.2.9 Resource Requirements

The mixed-signal circuits described in the previous sections serve as a guide in determining the architecture of MADAR. The resources required to implement each of the demonstration circuits is extracted and tabulated in Table 3-1 . The key information extracted includes the number of opamps, lookup tables, data converters, and interconnections required to implement each circuit. Note that the number of analog-to-digital and digital-to-analog connections only includes direct connections between the analog and digital sections; connections made via a data converter are not counted. By designing a reconfigurable mixed-signal chip that can implement all the demonstration circuits, it is expected that the resource and architectural requirements of a general and widely applicable field-programmable mixed-analog-digital array will be elucidated.

Using the tabulated data along with the specifications of the existing designs (LEGO and FPAA) described in the previous chapter, a mixed-signal chip containing four digital tiles with sixteen lookup tables, one analog tile with four opamps, and four data converters can implement all of the demonstration circuits. It should be noted that one analog tile occupies approximately the same area as four digital tiles. The next section will describe the overall architecture of MADAR.

Circuit	Opamps	Lookup Tables	ADC	DAC	A-D inter-connects	D-A inter-connects
Sigma Delta ADC	3	14	-	-	1	1
Dual Slope ADC	2	10	-	-	1	3
PWM DAC	1	13	-	-	-	1
Noise Generator	1	5	-	-	-	1
PLL	3	1	-	-	-	1
AGC	4	12	1	1	-	-
Data Acquisition	4	0	2	2	-	-
Signal Processor	2	12	1	1	-	-

Table 3-1: Summary of mixed-signal resources required.

3.3 MADAR Architecture

Although the demonstration circuits provided valuable information about the type of resources required, the ratio of component count between analog and digital circuitry is misleading if used to estimate the die area. The data extracted from the examples seems to suggest an equal area ratio; however, the area consumed by the digital portion is usually much greater due to other complex digital signal processing circuitry. For example, a 300 MHz 16-bit digital signal processing chip [Nomu94] implemented in a 0.5 μm BiCMOS process consumed an area of 3.9 mm x 4.6 mm.

Further examination of the demonstration circuits reveals that much of the digital circuitry is datapath oriented. By sharing programming bits among the bit slices of a datapath-oriented circuit, the density of an FPGA can be increased. An FPGA designed specifically for datapath-oriented circuits, DP-FPGA, has been implemented at the University of Toronto [Cher94]. Although the DP-FPGA tile offers a denser design, we have opted for the more granular LEGO tile as the digital building block in MADAR, because the demonstration circuits also contained random logic.

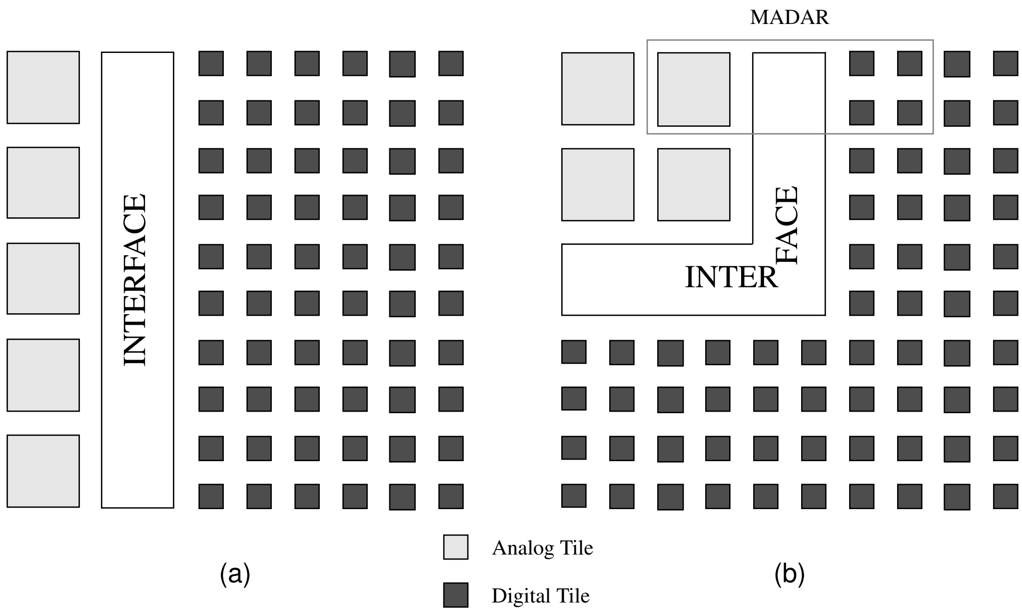

Figure 3-10: Field-programmable mixed-analog-digital array architectures.

Two possible architectures for a scalable field-programmable mixed-analog-digital array are shown in Figure 3-10. Both architectures consist of an array of analog and digital tiles connected by a mixed-signal interface. The analog tiles of the FPAA occupy approximately the same area as four LEGO digital tiles. In Figure 3-10(a), the analog tiles form a one-dimensional array in the vertical direction. This approach is viable, because analog signal processing often proceeds in a serial fashion without the need for long feedback paths. Also, long analog interconnection lines should be avoided to reduce the possibility of noise coupling into the signal path. Therefore, the connectivity should be limited to neighboring tiles only. An alternative approach is shown in Figure 3-10(b). Here, the organization of the analog tiles provides more flexible connections between the neighboring tiles. Furthermore, the analog tile located in the upper left corner is better isolated from the digital tiles so the most sensitive circuits can be mapped there. This is important because switching transients from digital circuits can adversely affect analog circuits by coupling through the common substrate. A recent study [Su93] has shown that the substrate noise in lightly-doped substrates is proportional to the physical separation between the analog and digital circuitry. It is worth noting that a large portion of the digital tiles are occupied by SRAMs which do not switch and hence do not contribute switching noise. The next section will discuss other issues that must be addressed in mixed-signal design.

3.3.1 Design Issues

The primary problem in mixed-signal circuits is noise coupling or crosstalk between the digital and analog sections. We have already mentioned physical separation as a means to limit the substrate noise. Another method involves the use of guard rings connected to a quiet power supply by a low impedance path to shield the sensitive analog circuitry. Device simulations in [Su93] [Stan94] have shown that the peak-to-peak noise voltage can be reduced by an order of magnitude when guard rings are used in lightly-doped substrates. Furthermore, they show that the substrate noise can be significantly reduced by increasing the number of package pins used to bias the substrate contacts. The increase in pins reduces the effective series inductance of the substrate bias.

Another source of noise coupling occurs over the power supply connections [OLea91]. Switching in digital circuits introduce transient currents in the power supply, which result in voltage variations that are unacceptable to sensitive analog circuits. The best method to combat this noise is to have separate pins for the analog and digital supplies.

Crosstalk between analog and digital signal lines occur through the mutual capacitance between the two lines [OLea91]. Care must be taken in the layout to reduce the overlap between the two signals. When a digital signal has to run parallel to an analog signal, an analog ground line can be inserted to decouple the two lines. Furthermore, short analog interconnections should be used to minimize the possibility of parasitic coupling.

Noise immunity can be achieved by using fully-differential circuit techniques. Noise is seen as a common-mode disturbance that will be rejected by a differential circuit due to its symmetrical nature [Sedr94]. Furthermore, differential circuits reduce the effect of offset and feedthrough due to charge injection in clocked circuits.

The design of MADAR took into consideration all of the issues mentioned. Guard rings were used to shield the analog circuitry, and the analog array is separated from the digital array by the interface. Separate pins were used supply the power (±3 V) to the analog and digital arrays; in addition, a separate pin was dedicated to the substrate bias and guard rings. Fully-differential circuit techniques are used throughout the design of the mixed-signal interface, which is described in the next section.

3.4 Mixed-Signal Interface

The demonstration circuits in Section 3.2 have shown that an interface is required to connect the analog and digital circuits, and that this interface must be bidirectional. In some cases, there is a need to perform signal conversion using A/D converters and D/A converters, but there is also a need to provide direct connections between the two arrays. The mixed-signal interface that is implemented in MADAR will be described in this section. It contains data converters, and uses the connection resources available in FPAA and LEGO to provide the connectivity and routing.

It has been shown by the demonstration circuits that it is possible to build data converters out of the existing resources available in the array. However, these circuits are slow, and also use up the available resources. Therefore, we propose to place dedicated converters, which offer both higher conversion speeds and also occupy less area, but are less flexible. Flexibility, in this context, refers to the resolution of the converters. By building the converters out of the resources in the two arrays, the desired resolution can be programmed to meet the requirements of the application. However, with dedicated converters, the resolution is fixed. The penalty of reduced flexibility is addressed by putting some degree of flexibility into the converters. We have chosen two expandable architectures that can be configured to be a single converter or two converters with half the resolution. These architectures can be easily expanded by replicating circuitry to build higher resolution converters. Four bits has been chosen as the maximum resolution for the converter, which is dictated by the fact that each LEGO tile contains four lookup tables, and also to constrain the design to a reasonable size. Therefore, each data converter can be configured as either a single 4-bit converter or two 2-bit converters. The speed of the converters is dictated by the bandwidth of the analog array. Presently, the analog array can operate in the hundred kHz range. The converters must operate at a speed greater than the Nyquist rate; therefore, the data converters will be designed for 1 MHz operation. The design and implementation of these converters will be discussed in the following two chapters.

Figure 3-11 shows a block diagram of the mixed-signal interface. Included in the figure, are two digital tiles, the data converters, four columns of the signal-controlled interconnection network

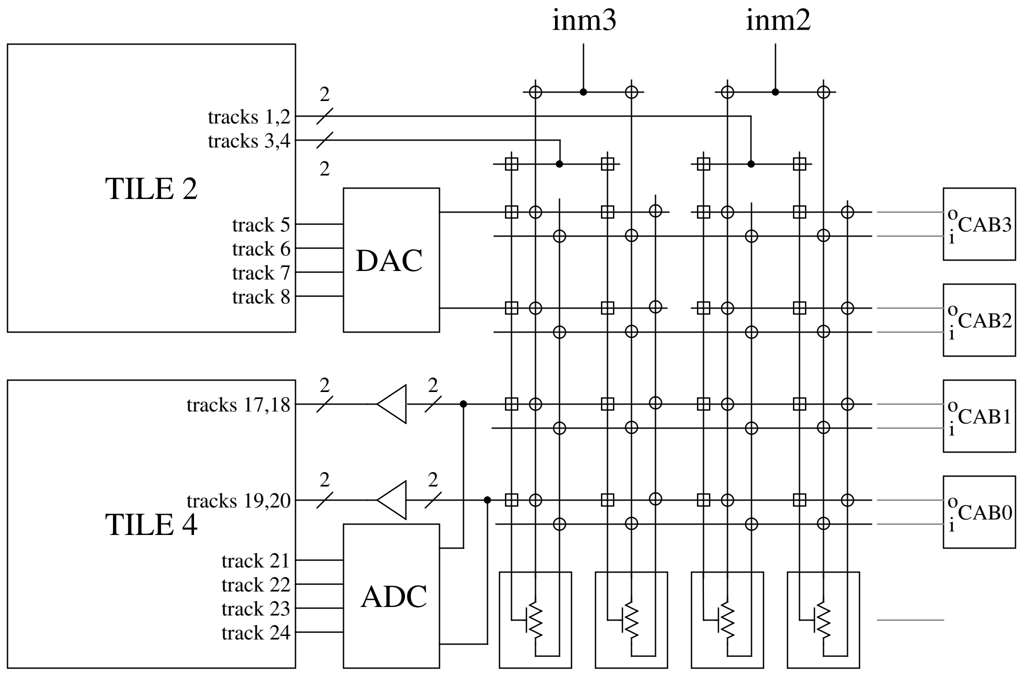

Figure 3-11: Block diagram of mixed-signal interface.

(SCIN), and four configurable analog blocks (CABs). The two digital tiles each contain 16 tracks for a total of 32 tracks. Eighteen are one-segment tracks of which sixteen are used to connect the digital and analog arrays. The analog input signals inm3 and inm2 come directly from the pins. The top half of the circuit handles signals propagating in the digital-to-analog direction, while the bottom half handles signal propagating in the reverse direction.

In the analog-to-digital direction, the analog signal comes from the output of a comparator (a CAB with the compensation capacitor disabled) so that it is already in a digital form. Since the comparator uses only p-type devices in the output driver, the minimum output voltage is one threshold above the negative supply. This signal is buffered to restore it to rail-to-rail voltage levels. A reconfigurable four-bit analog-to-digital converter is used to provide linear conversion of low-level signals in the analog-to-digital direction. The converted signals are connected directly to the one-segment tracks in the digital array because most of the interconnections occur only along the border. By using one-segment tracks only, the longer segment tracks are available for other signals with long paths. Once the signal is on a track, it can be connected to a lookup table through the connection block, or routed elsewhere through the switch blocks. By utilizing

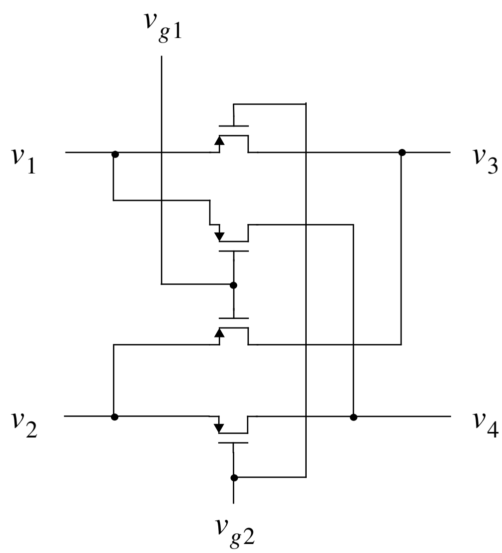

Figure 3-12: Four-transistor tranconductor.

the connection and routing resources of the digital array, a second level of hierarchical routing is avoided resulting in speed improvement and area savings.

In the digital-to-analog direction, the digital input comes from the one-segment tracks of the digital array, and connects to the SCIN of the analog array. From the demonstration circuits, we observe that digital signals are sometimes used to control switches, and sometimes they are used as direct inputs to a resistor or to control a voltage-controlled resistor. In the first case, rail-to-rail digital signals can be used because the transistor operates in either the linear or cutoff region. For convenience, the four-transistor transconductor is again shown in Figure 3-12. The four-transistor transconductor acts as a switch element by turning off the two middle transistors, and employing the two outside transistors as the switches. In the latter case, the digital signal cannot swing rail-to-rail otherwise the transconductors and opamps will leave the linear region of operation and go into saturation. The four-transistor transconductor can be used to accept a digital input by using it as a multiplexer. The digital input is applied to the terminals labelled v_{g1} and v_{g2}, and a small fixed differential voltage can be connected at the input terminals v_1 and v_2. The resulting voltage waveform at the output of the transconductor $v_3$and v_4 will be a scaled version of the digital input at v_1 and v_2. A reconfigurable four-bit D/A converter is also available to convert the digital data to an analog signal which can be fed directly as an input to the analog array. It can be level shifted when it is used as the controlling voltage of the transconductor in the SCIN to increase the input dynamic range.

3.5 Summary

This chapter described a number of mixed-signal circuits that will be used to prove the concept of a field-programmable mixed-analog-digital array. Information extracted from these circuits was used to determine the architecture of MADAR and the mixed-signal interface. The interface contains reconfigurable data converters. The design and implementation of a reconfigurable D/A converter and A/D converter are presented in Chapter 4 and Chapter 5, respectively.

Chapter 4

Reconfigurable Digital-to-Analog Converter

4.1 Introduction

Data converters play a crucial role in a mixed-mode environment that contains information in both analog and digital form. They serve as the interface between these two different environments, and convert the data from digital to analog or vice versa. On a mixed-signal chip, it is important that the data converters are as compact as possible to make more area available for the analog and digital functions. Moreover, the architectures chosen should be scalable, that is the resolution can be easily increased, for future implementations. This chapter will cover digital-to-analog conversion, and the reconfigurable bipolar D/A converter that is implemented in MADAR. Analog-to-digital conversion, and the reconfigurable bipolar A/D converter will be presented in the next chapter.

4.2 Digital-to-Analog Conversion

Digital-to-analog converters (DACs) take a digital input word and provide an analog output that represents the digital input word. The transfer characteristic of a D/A converter is given by

$$V_O = V_{FS}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) \tag{4-1}$$

where the analog output V_O is a function of the full scale voltage V_{FS}, and the binary coefficient bits b_1 through b_N [Greb84]. The most significant bit (MSB) of the digital word is b_1, and the least significant bit (LSB) is b_N. The output voltage V_O ranges from zero, when all the coefficients are equal to ‘0’, to a maximum value of

$$(V_O)_{max} = V_{FS}\left(\frac{2^N - 1}{2^N}\right) \tag{4-2}$$

when all the coefficients are equal to ‘1’. The minimum analog step size is equal to the full scale voltage divided by the total number of bits

$$\Delta V_O = \frac{V_{FS}}{2^N} \tag{4-3}$$

A D/A converter that can have both positive and negative output values is termed bipolar. There are many ways to represent signed numbers such as sign-magnitude, offset-binary, 1’s complement, 2’s complement, etc. For simplicity, we have chosen to represent the digital input using offset-binary notation, which assigns zero to the most negative number, and then proceeds to count up as in the unipolar case. The resulting output is given by

$$V_O = V_{FS}[(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) - 0.5] \tag{4-4}$$

Figure 4-1 shows the ideal transfer characteristic of a bipolar four-bit D/A converter with sixteen distinct output levels.

4.3 Binary-Weighted D/A Conversion Techniques

Although there are many ways to perform D/A conversion, the discussion will be limited to binary-weighted techniques using resistors and capacitors as they are directly related to the architecture chosen to implement the reconfigurable D/A converter. Figure 4-2 shows a binary-weighted resistor-based D/A converter [Greb84]. If the binary digit that controls a switch is a ‘1’, current flows into the virtual ground of the opamp and contributes to the output of the DAC; when it is a ‘0’, the current flows to ground. The resistors are sized so that the current is halved corresponding to the position of the bit in the digital input word. The resulting output

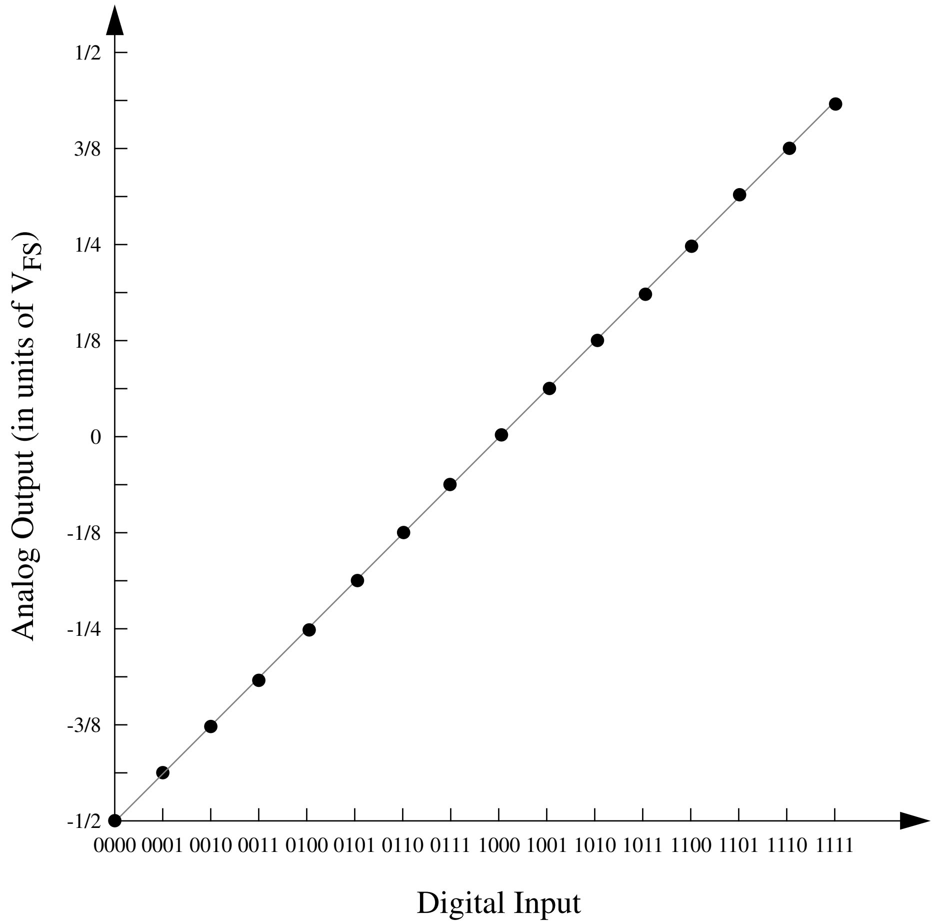

Figure 4-1: Transfer characteristic for a bipolar four-bit D/A converter.

voltage is proportional to the summation of all the currents that flow into the virtual ground and is given by (4-1). The drawback of this approach is that the resistor ratios required are on the order of 2^N, which is difficult to achieve on an integrated circuit. An architecture that alleviates this

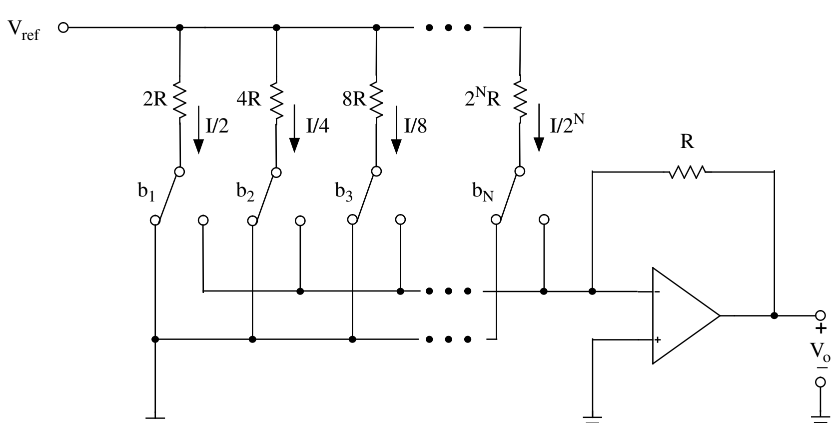

Figure 4-2: Binary-weighted resistor-based D/A converter.

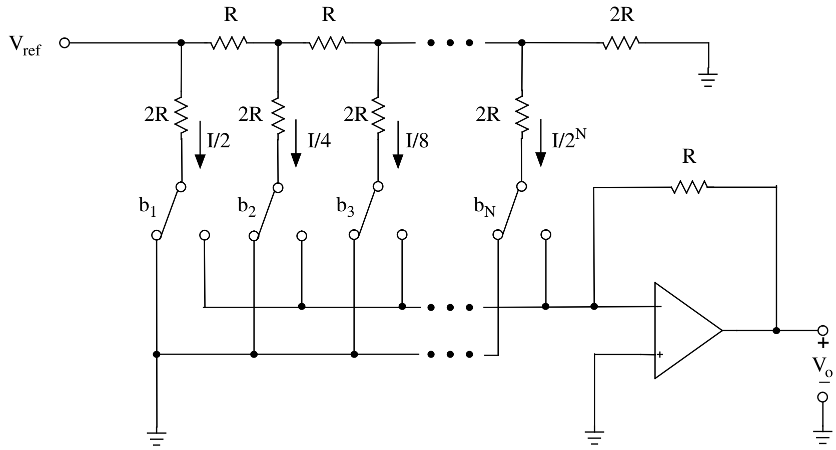

Figure 4-3: Binary-weighted R-2R-based D/A converter.

problem by reducing the range of resistor values required is based on an R-2R ladder configuration, shown in Figure 4-3. The R-2R network performs a binary division of the current by successively partitioning the current between the series (R) and shunt (2R) branches. This circuit reduces the resistor range required so that only two resistor values, R and 2R, are needed. The accuracy of these resistor-based architectures is dependent on the precise matching within the resistor network. The matching accuracy of integrated resistors is of the order 0.1%-0.4% making it possible to achieve a resolution of up to nine bits [Malo91a]. Higher resolutions may be achieved using expensive trimming techniques to improve the resistor matching.

A similar binary-weighted architecture can be realized using capacitors, which have better matching than resistors. In fact, the matching accuracy of integrated capacitors is on the order of 0.05%-0.2% which would allow up to 10-bit resolution [Malo91a] [Gray94]. Figure 4-4 shows a charge-scaling D/A converter implemented using binary-weighted capacitors [Greb84]. During ϕ_1, the capacitors in the capacitor array are charged to either V_{ref} or ground depending on the input word. A binary '1' connects the switch to V_{ref} while a binary '0' connects the switch to ground. During ϕ_2, the total charge sampled onto the capacitor array during ϕ_1 is transferred to the integrating capacitor. The resulting output voltage is proportional to the ratio of capacitances connected to V_{ref}, and the integrating capacitor. This is the desired analog output corresponding to the input digital word as given by (4-1). Again, the ratio of capacitor values required is on the order of 2^N, which is difficult to achieve in integrated form. The capacitor ratio can be reduced by

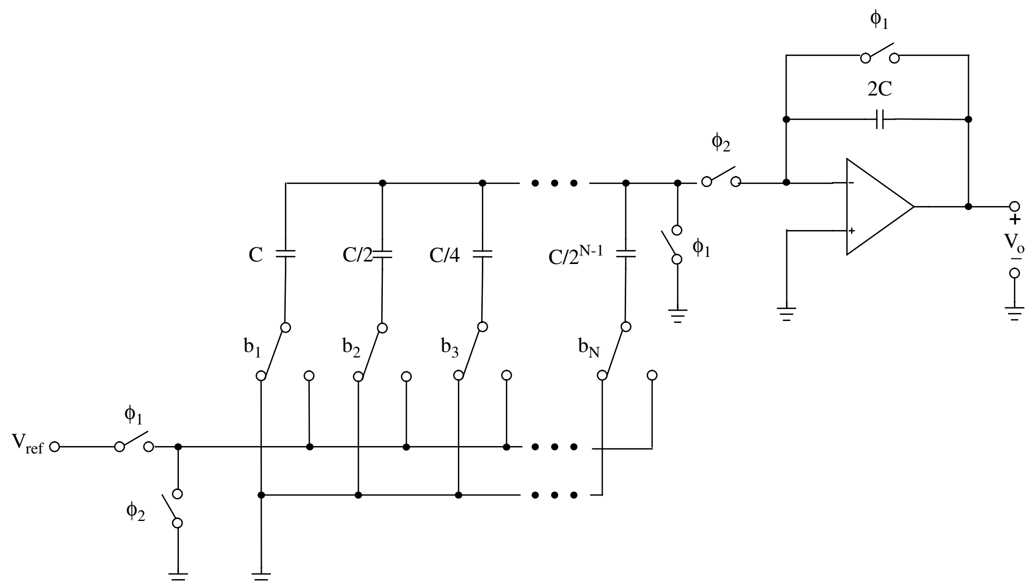

Figure 4-4: Binary-weighted charge-scaling D/A converter.

using a capacitor equivalent of the R-2R ladder; however, this circuit realization is sensitive to the bottom plate parasitics of MOS capacitors due to the floating series capacitors in the circuit.

The next section describes a method to perform current division that does not require either resistors or capacitors. The design of the reconfigurable D/A converter in MADAR will be based on this technique.

4.4 Linear Current Division Technique Using MOS Transistors

The D/A conversion methods described in the previous section used resistor or capacitor ladders to perform current or voltage division, while using MOS transistors as switches. However, the transistors can be used to perform both the division and switching functions, thus eliminating the need for resistors or capacitors [Bult92]. Figure 4-5 shows two MOS transistors with the same gate voltage V_g with respect to the substrate. The voltages V_1 and V_2 can have any DC value as long as the transistors are turned on; voltage differences between V_1 and V_2 will only introduce a DC offset current. An input current I_{in} is applied to the circuit; a portion of the current will flow

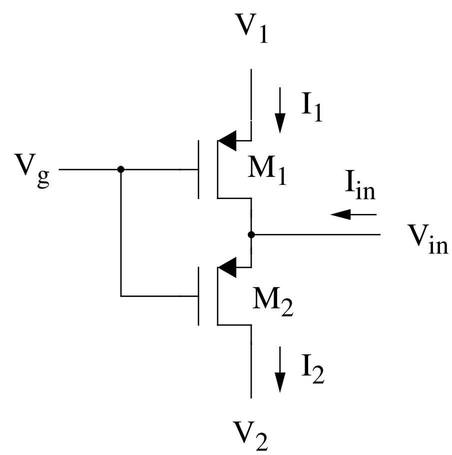

Figure 4-5: Linear current division technique.

into M_1, and the remainder into M_2. The current division principle states that the division of the applied current is dependent only on the geometry of the devices, with a ratio given by

$$\frac{\Delta I_1}{\Delta I_2} = -\frac{W_1/L_1}{W_2/L_2} \tag{4-5}$$

This method of current division can be used to realize a MOS transistor equivalent of the R-2R network. Consider the MOS transistor network shown in Figure 4-6. A unit MOS transistor is used to replace the series resistor in the R-2R ladder, and two unit transistors replace the corresponding shunt resistor. The effective W/L ratio of transistors 1a and 1b in the shunt path is

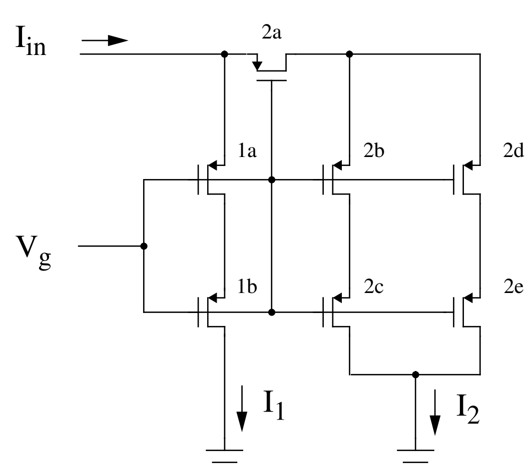

Figure 4-6: MOS transistor equivalent of R-2R network.

equal to half the W/L ratio of the unit transistor. The composite transistor formed by transistors 2a-2e also has the same effective W/L ratio. This MOS transistor network can be reduced to the two transistor circuit shown in Figure 4-5. Application of the current division principle results in an equal division of the current I_{in}, since the two composite transistors have equal effective W/L ratios, and input voltages.

The accuracy of this current division technique is affected only by mismatching of device geometries, while mismatches in the threshold voltages will lead to distortion. A volume control circuit utilizing this current division technique was fabricated [Bult92]. The measured attenuation error was less than 0.15 dB, and the total harmonic distortion was better than -85 dB.

This current division technique can be used to build a binary-weighted D/A converter using architectures similar to the ones described in the previous section [Bult94]. Furthermore, a degree of configurability will be added to the architecture for use in a field-programmable mixed-signal chip.

4.5 Reconfigurable D/A Converter Architecture

In the design of the reconfigurable D/A converter for MADAR, the constraints imposed by the existing analog and digital arrays must be considered. First, the bandwidth of the analog array is in the hundred kHz range. Since the data conversion rate should exceed the Nyquist rate, a 1 MHz conversion rate is chosen. Second, the maximum output voltage is chosen to be ±0.5 V so that the transconductors will remain in the linear region of operation. Last, a resolution of four bits is chosen to match the datapath width of the digital tile that contains four lookup tables. Since this D/A converter is part of a field-programmable system, it should have some degree of reconfigurability. We have chosen the resolution as the variable parameter in the design of a reconfigurable 1 MHz 4-bit D/A converter.

The current division technique is applied to realize a reconfigurable D/A converter with two modes of operation, which is shown in Figure 4-7. It can function as either a single 4-bit DAC or two 2-bit DACs. A single configuration bit determines the mode of operation; a binary ‘1’ indicates four-bit operation, and a binary ‘0’ indicates two-bit operation.

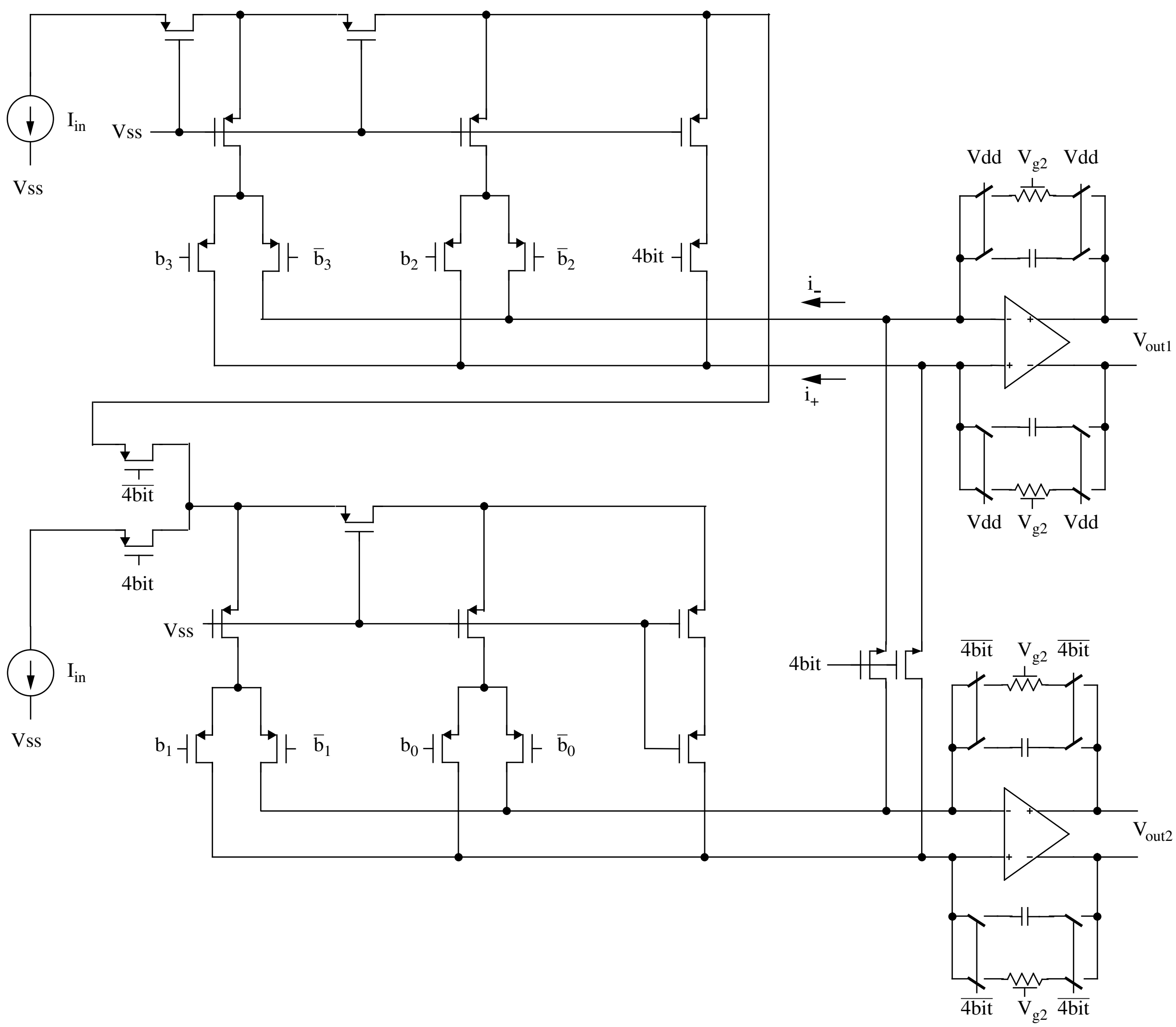

Figure 4-7: Reconfigurable D/A converter.

The reconfigurable D/A converter contains two independent 2-bit DACs that can be connected together to form a single 4-bit DAC. Fully differential signalling is used to increase the output dynamic range (2V), and also provide good noise rejection. Power is provided by ±3 V supplies, thus allowing bipolar operation. The reconfigurable D/A converter is designed to have a conversion time of 1 µs for both four-bit and two-bit modes of operation.

In two-bit mode, the two DACs function independently; each DAC has its own opamp and current source. The current I_{in} is provided by two current mirrors, and its value is set by an external resistor. The converter functions in much the same way as the binary-weighted R-2R D/A converter described in Section 4-2, only now the binary current division and switching is accomplished using only MOS transistors. Unit p-type MOS transistors measuring 6.4µm/6.4µm are used for all the transistors in the current division network, including the switches, which contribute to the effective W/L ratio. Since the D/A converter is implemented in a CMOS n-well process, p-type transistors are used because they offer better noise immunity. Consider the upper D/A converter in Figure 4-7, where b_3 is the MSB and b_2 is the LSB. Simple analysis gives the following set of equations.

$$i_- = I_{in}(b_3 2^{-1} + b_2 2^{-2}) \tag{4-6}$$

$$i_+ = I_{in}(1 - b_3 2^{-1} - b_2 2^{-2}) \tag{4-7}$$

$$i_+ - i_- = -2I_{in}[(b_3 2^{-1} + b_2 2^{-2}) - 0.5] \tag{4-8}$$

Conversion from current to voltage is performed by the fully-differential opamp and the modified transconductor, which is shown as a voltage-controlled resistor in Figure 4-7. The voltage-controlled resistor only shows a single control terminal, V_{g2}, because the other terminal, V_{g1}, is tied to the negative supply. The resulting output voltage for two-bit operation is given by

$$V_{out1,2\text{bit}} = \frac{-2I_{in}}{\mu C_{ox} W/L(V_{g1} - V_{g2})}[(b_3 2^{-1} + b_2 2^{-2}) - 0.5] \tag{4-9}$$

where V_{g2} is connected to a pin so that the desired full scale value can be set externally. A single 4-bit D/A converter is realized by combining the two current division networks. The upper network determines the current contribution from the two MSBs, while the lower network determines the current contribution from the two LSBs; consequently, all the currents in the lower network must be scaled by a factor of one quarter. The input current to the lower network can be supplied by a current source that is scaled by one quarter. However, the current in the final branch of the upper network is also equal to $I_{in}/4$. By using the current in the final branch of the upper network to supply the lower network, better matching and hence linearity will be achieved.

Now that the currents in the lower network are properly scaled, they are diverted to the upper network using MOS transistors. The modified transconductor in the lower network is turned off so that all of the current flows into the input terminals of the upper opamp. Although switches are not required in the feedback path of the upper opamp, they are included to preserve the symmetry in the two circuits. The resulting output voltage of the D/A converter for four-bit operation is given by

$$V_{out1,4\mathrm{bit}} = \frac{-2I_{in}}{\mu C_{ox} W/L \left(V_{g1} - V_{g2}\right)} \left[\left(b_3 2^{-1} + b_2 2^{-2} + b_1 2^{-3} + b_0 2^{-4}\right) - 0.5 \right] \qquad (4\text{-}10)$$

The addition of the switches into the circuit introduces non-linearity errors in the D/A converter. For equal current division to occur, the voltages at the drains of the shunt transistors must be equal. In the absence of the switches, the large open loop gain of the opamp maintains a very small voltage difference between the input nodes of the opamp, and thus the drains of the shunt transistors. With the addition of non-ideal switches, there is a voltage drop across them that leads to errors in the current division. Moreover, the voltage drop across the two switches is not identical because they are dependent on the current flow, which changes according to the digital input word. Therefore, large n-type transistors with a W/L ratio of 25/1 are used for the reconfiguration switches to minimize the voltage drop. Also the switches are placed in the lower network, which has the smaller current.

The differential opamps are the same as the ones used in the configurable analog blocks of the analog array, except the compensation capacitor is reduced because it does not have to drive a large off-chip load. The reduction in compensation results in an increase in the slew rate. Its simulated parameters are shown in Table 4-1. Capacitors are placed in the feedback loop of the

Item	Value
Open Loop Gain	78 dB
Unity Gain Frequency	11 MHz
Settling Time to 0.1%	300 ns
Slew Rate	18 V/µs
Power Dissipation	4.4 mW

Table 4-1: Simulation results for differential opamp with 0.5 pF loading.

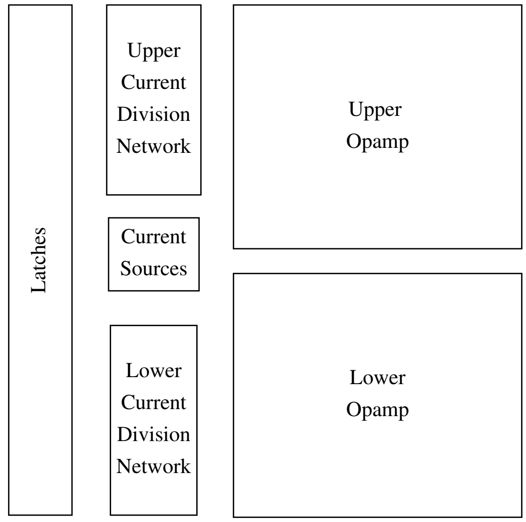

Figure 4-8: Floorplan of reconfigurable D/A converter.

opamps to reduce the glitches that occur when the digital input word changes, and also to dampen the circuit to reduce ringing.

The reconfigurable D/A converter measures only 554 μm x 487 μm, and its floorplan is shown in Figure 4-8. Latches are located at the extreme left to synchronize the digital input word. The current division network is located in the middle, along with the current sources. The opamps are located at the extreme right to isolate them from the digital circuitry. Higher resolutions are easily obtainable by simply adding more branches to the current division networks. The resulting increase in area is minimal since the most of the area is occupied by the opamps.

4.6 Simulation Results

The reconfigurable D/A converter was simulated using HSPICE [Meta91]. Figure 4-9 shows the output response of the converter to a digital input counting up from 0000 to 1111. The simulation results are presented in Table 4-2. Linearity errors caused by mismatching component geometries and threshold voltages are absent during simulation; therefore, we expect larger non-linearity errors from the experimental results of the fabricated circuit. The maximum settling time for the D/A converter to within ±0.5 LSB of the final value when the input code changes from 0000 to 1111 and vice versa was 0.68 μs, which satisfies the 1 MHz conversion requirement.

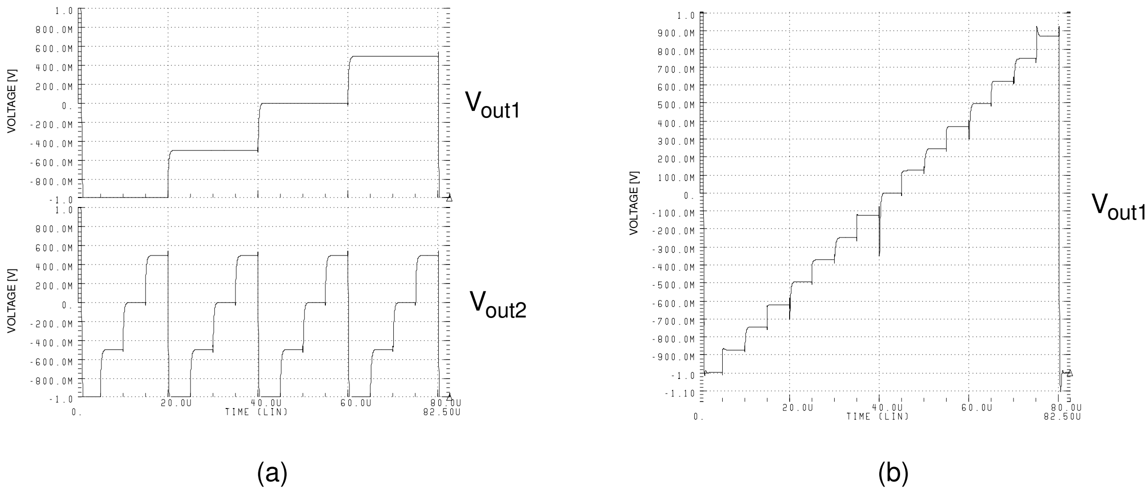

Figure 4-9: Simulation results for fully-differential reconfigurable D/A converter in (a) two-bit mode (b) four-bit mode.

Item	Value
Integral Non-linearity	±0.05 LSB
Differential Non-linearity	±0.03 LSB
Settling Time	< 1 μs
Power Dissipation	9 mW

Table 4-2: Simulation results for fully-differential reconfigurable D/A converter with 0.5 pF loading.

4.7 Experimental Results

A single-ended version of the reconfigurable D/A converter was fabricated and tested. Its performance is shown in Table 4-3 including both simulated and experimental results. The

Item	Simulated Value	Experimental Value
Integral Non-linearity	±0.31 LSB	±0.46 LSB
Differential Non-Linearity	±0.11 LSB	±0.31 LSB
Settling Time	< 1 μs	< 1 μs
Power Dissipation	7.8 mW	9 mW

Table 4-3: Simulation and experimental results for single-ended reconfigurable D/A converter.

(a) (b)

Figure 4-10: Experimental results for single-ended reconfigurable D/A converter in (a) two-bit mode (b) four-bit mode.

non-linearity error measurements were larger than the simulation results as expected due to mismatching component geometries. The settling time measurements showed that it could meet the 1 μs conversion time requirement. The poor performance of the single-ended version was due to the use of smaller unit transistors, smaller reconfiguration switches, and single-ended signalling. The staircase output waveforms of the reconfigurable D/A converter in two-bit mode and four-bit mode are shown in Figure 4-10(a) and Figure 4-10(b), respectively. The differential version will have much better performance than the single-ended version because the simulated non-linearity errors for the differential version were much less than those for the single-ended version. Also, we expect the experimental results to correlate better with the simulated results in the differential version, because larger unit transistors were used, which reduces the effect of mismatching geometries.

4.8 Summary

This chapter described the design and implementation of the reconfigurable bipolar 4-bit D/A converter that will be used in MADAR. The design is area-efficient, and capable of performing data conversion at 1 MHz. Simulation results for a fully-differential version are presented, and experimental results for an earlier single-ended version are provided.

The next chapter will discuss the design and implementation of a reconfigurable 4-bit A/D converter for use in MADAR.

Chapter 5

Reconfigurable Analog-to-Digital Converter

5.1 Introduction

Analog-to-digital converters perform the opposite function to the digital-to-analog converters discussed in the previous chapter. They take an analog input signal and convert it to a digital equivalent. Several A/D conversion techniques have already been presented by the demonstration circuits in Chapter 2. However, these are only suitable for low-speed applications. Today, there are many applications that require high speed conversion. For example, the HDTV standard requires A/D converters with ten-bit resolution that can operate at speeds up to 75 MHz [Yots93]. An architecture that can be used to build high speed converters will be introduced in this chapter. This architecture will be the basis of the reconfigurable bipolar 4-bit A/D converter that is implemented in MADAR.

5.2 Analog-to-Digital Conversion

An analog-to-digital converter converts an analog signal to its digital equivalent, where the two signals are related by

$$b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N} = \frac{V_i \pm V_e}{V_{FS}} \qquad (5\text{-}1)$$

where $-0.5LSB \le V_e \le 0.5LSB$

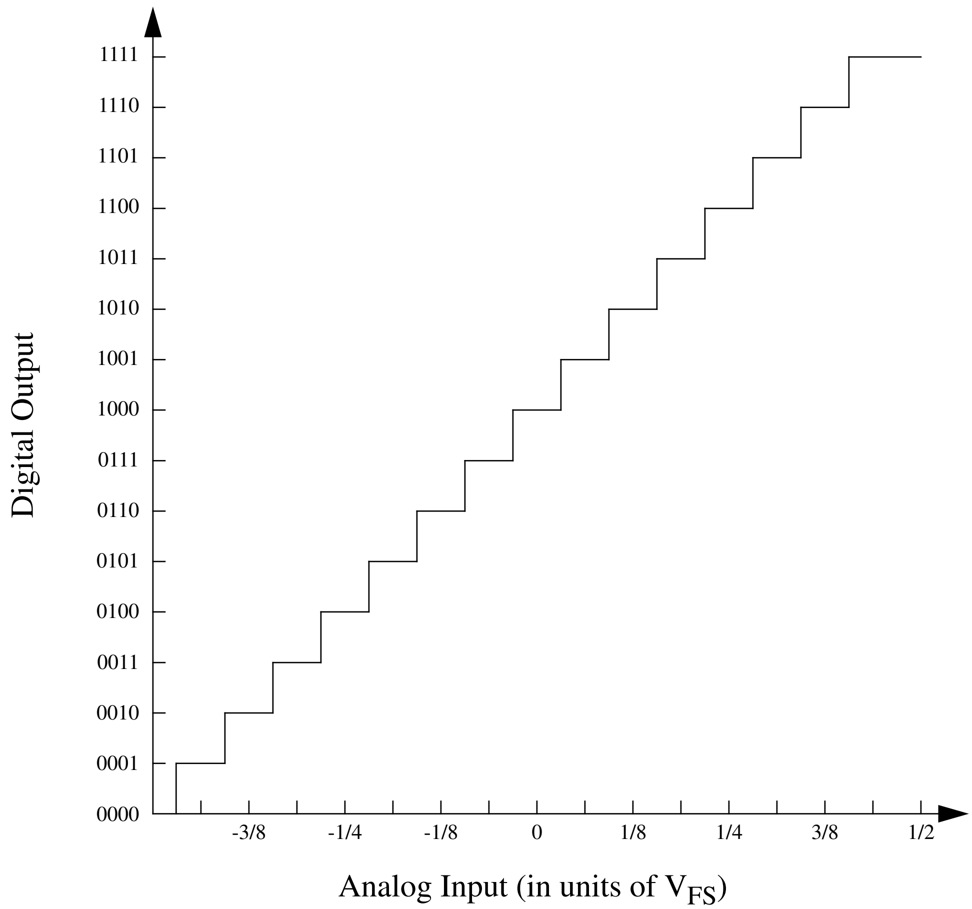

Figure 5-1: Transfer characteristic for a bipolar 4-bit A/D converter.

The digital word consists of the binary coefficients b_1 through b_N, which represents the ratio of the input voltage V_i and the full scale voltage V_{FS}. Since there is not a unique one-to-one relationship between the analog input and the digital output (that is, a given digital output can be produced by more than one analog input), a quantization error voltage, V_e, must be included in (5-1). Figure 5-1 shows the ideal transfer characteristic of a bipolar offset-binary-coded 4-bit A/D converter. Note that the transitions take place ±1/2 LSB away from the analog input voltage that corresponds to a particular digital output. The next section will describe a fast A/D conversion technique.

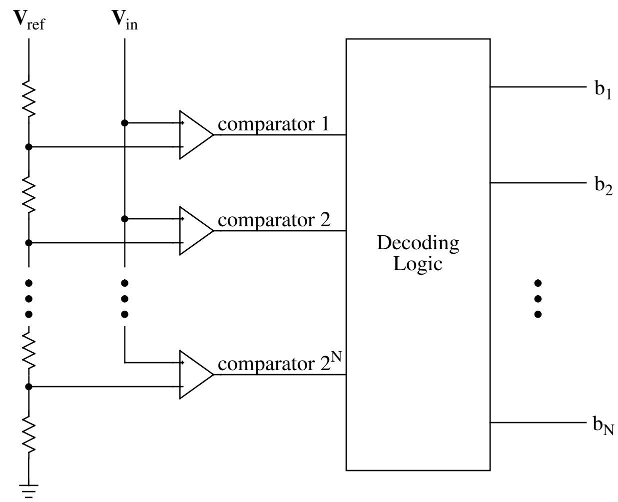

Figure 5-2: Block diagram of a flash converter.

5.3 Flash Architecture

Flash or parallel converters are the fastest A/D converters available [Greb84]. A functional block diagram of a flash A/D converter is shown in Figure 5-2. An analog input voltage V_{in} is compared against a set of monotonic reference voltages generated by a resistor string. When V_{in} is greater than the reference voltage, the comparator output is positive; when V_{in} is less than the reference voltage, the comparator output is negative. The resulting output from the set of comparators is a thermometer code equivalent of the analog input, which is then decoded to produce the final binary digital output.

Although this architecture is conceptually very simple, it is very difficult to realize high resolution converters using this architecture because of the amount of circuitry required. An N-bit converter requires 2^N comparators, and the decoding logic associated with it. For example, a 10-bit A/D converter would need 1024 comparators. The large number of comparators required to build high resolution converters consumes alot of area and power, plus the comparators contribute to create a large input capacitance. A technique that reduces the amount of circuitry required is the two-step approach, which will be described in the next section.

5.4 Two-Step Conversion

The functional block diagram of a two-step A/D converter is shown in Figure 5-3. The analog signal is fed into an M-bit A/D converter, which performs a coarse conversion to determine the M

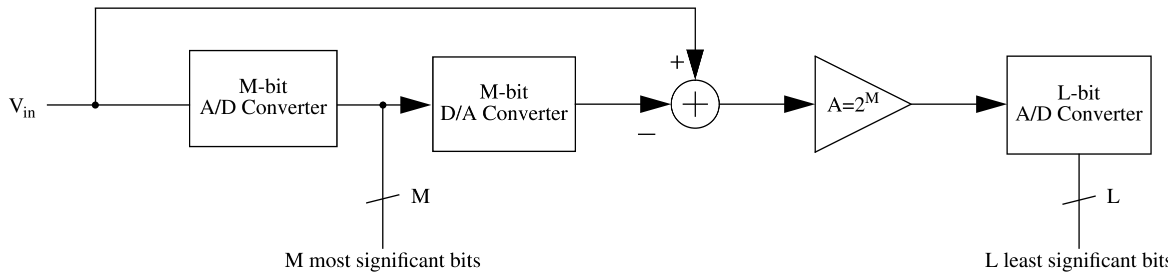

Figure 5-3: Two-step conversion.

most significant bits. These MSBs are fed into an M-bit D/A converter to give a quantized analog estimate of the original analog signal. Next, the output from the D/A converter is subtracted from the original analog input signal to give a residue, which is then amplified by a factor 2^M. This amplified residue voltage is fed into an L-bit A/D converter which performs a fine conversion to determine the L least significant bits. By combining the bits from the two A/D converters, a resolution of M+L bits is achieved. Combining the two-step approach with a flash architecture results in a significant savings in the amount of circuitry required. For example, a 10-bit A/D converter can be realized using two 5-bit A/D converters, which only require 64 comparators as opposed to the 1024 comparators that are required in the single-step method. The resulting savings in area and power is offset by a reduction in speed. The two-step approach along with flash A/D converters will be used to implement the reconfigurable A/D converter used in MADAR.

5.5 Reconfigurable A/D Converter Architecture

In the design of the reconfigurable A/D converter for MADAR, we must take into account the specifications of the existing analog and digital arrays. The design constraints are the same as those defined for the reconfigurable D/A converter in Section 4.5. Following these guidelines, a reconfigurable 1 MHz 4-bit A/D converter with two modes of operation is designed and implemented; it is based on a 5 MHz 12-bit A/D converter design found in [Raza92]. It can function as either a single 4-bit ADC or two 2-bit ADCs. A single configuration bit determines the mode of operation; a binary ‘1’ indicates four-bit operation, and a binary ‘0’ indicates two-bit operation.

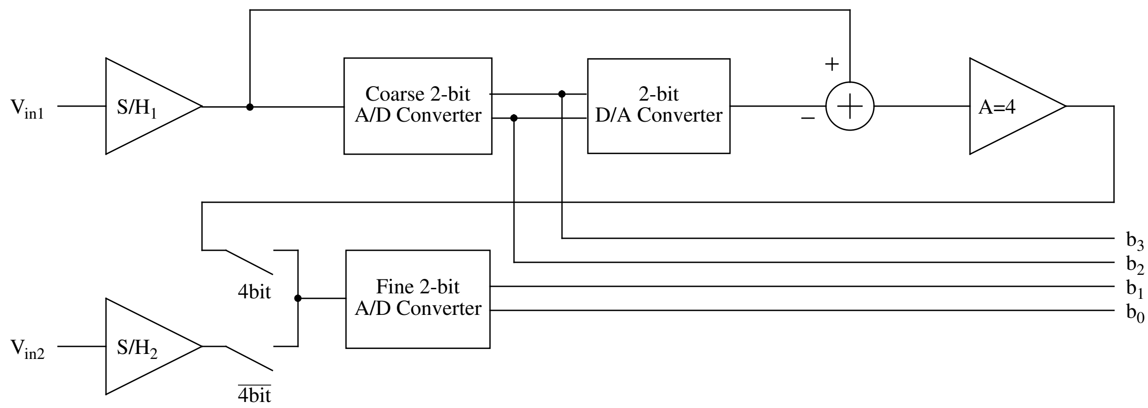

Figure 5-4: Reconfigurable 4-bit A/D converter.

The reconfigurable A/D converter, shown in Figure 5-4, takes advantage of the fact that a two-step converter consists of two independent A/D converters. For 4-bit resolution, the coarse and fine sections can be combined by closing the upper configuration switch to form a single 4-bit A/D converter; for 2-bit resolution, each A/D converter can function independently by closing the lower switch to give two 2-bit A/D converters. The coarse A/D converter supplies the two MSBs in the four-bit word, and the fine A/D converter supplies the two LSBs. The reconfigurable A/D converter consists of four major building blocks: the sample-and-hold circuit, the coarse A/D converter, the D/A converter and subtracter, and the fine A/D converter. A detailed description of each block is provided in the following sections.

5.5.1 Sample-and-Hold Circuit

The sample-and-hold circuit is a critical component in a flash A/D converter, and its performance is often the limiting factor in the speed of conversion. It must hold the value of the input signal constant while the comparison takes place for accurate data conversion. The sample-and-hold circuit, shown in Figure 5-5, has the same circuit topology as the one in [Lewi87]. Two-phase non-overlapping clocks ϕ_1 and ϕ_2 with a fifty per cent duty cycle were used to control the circuit. During the sample mode (ϕ_1 is high), the input is sampled onto sampling capacitor C_S, and the integrating capacitor C_I is reset. During the hold mode (ϕ_2 is high), the left side of the sampling capacitors are connected, and the charge from the sampling capacitors is transferred to the integrating capacitors. The resulting output is the equal to the final value of the sampled input. By using a fully-differential approach, the charge injected by the switches is

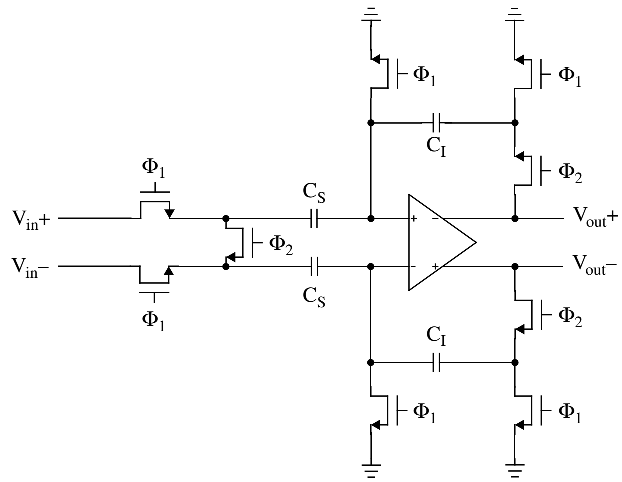

Figure 5-5: Sample-and-hold circuit.

turned into common mode disturbances. Also, the high gain of the opamp drives its differential input to zero in a closed loop configuration, hence, the gain of circuit is insensitive to parasitic capacitances on either the top or bottom plates of any of the capacitors.

The two-stage opamp used in the configurable analog block of the analog array does not have the bandwidth required to satisfy the 1 MHz operation required by the sample-and-hold circuit. However, the loading seen by the sample-and-hold circuit is purely capacitive, therefore, a low output impedance is not required. This allows an operational-transconductance amplifier (OTA) with increased bandwidth capability to be used, rather than the two-stage opamp. The schematic of the OTA is shown in Figure 5-6. The circuit consists of three stages: the bias stage, the input stage, and the common-mode feedback stage. Since the bias stage has two stable operating points, a startup circuit (not shown in figure) is used to ensure the correct operating point. The layout for the OTA was automatically generated using software developed at the University of Toronto [Univ94], and then manually compacted to reduce the area. Furthermore, the bias circuitry is shared by all the OTAs in the reconfigurable A/D converter to save additional area and power. The simulation results for the OTA are given in Table 5-1. By using the OTA, the output of the sample-and-hold circuit settles to an accuracy of 0.1% in 30 ns for a 2V differential input step and 1.0 pF loading.

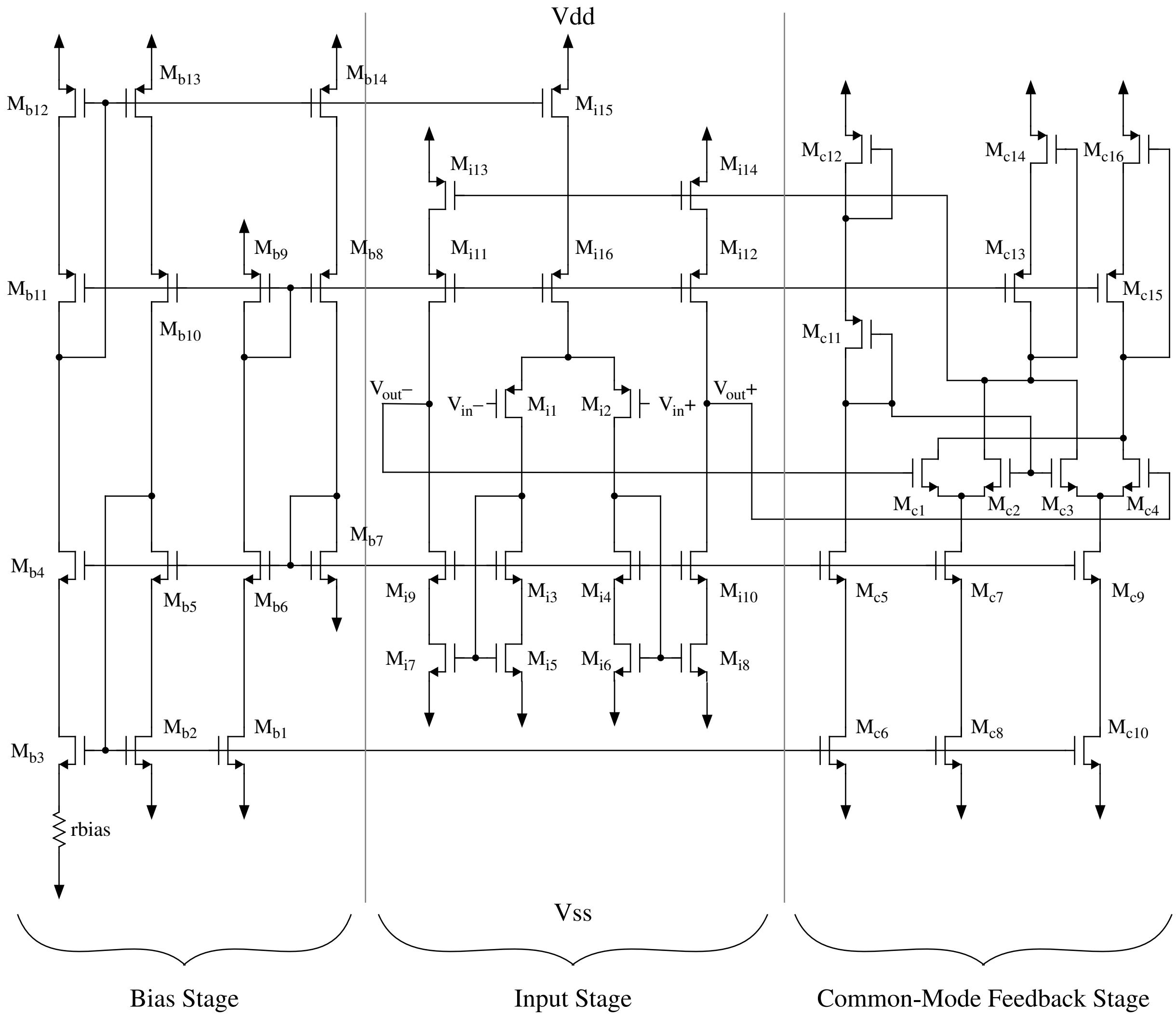

Figure 5-6: Operational-transconductance amplifier schematic.

Item	Value
Open Loop Gain	75 dB
Unity gain frequency	80 MHz
Settling Time to 0.1%	30 ns
Slew Rate	102 V/µs
Power Dissipation	10.3 mW

Table 5-1: Simulation results of OTA with 1.0 pF loading.

5.5.2 Coarse A/D Converter

The coarse A/D converter, shown in Figure 5-7, takes an analog input signal and produces the two most significant bits. The reference voltages are derived from a resistor string folded at its midpoint. It consists of 32 polysilicon resistors each with a width of 8 µm and a length of 32 µm, and a sheet resistivity of 30 $\Omega/\square$. In a normal flash 2-bit A/D converter, only four unit resistors are required in the resistor string. However, the reference voltages at which the transitions occur for a 2-bit A/D converter differ from those of a 4-bit A/D converter as shown in Figure 5-8. For example, in the 2-bit A/D converter, the first transition occurs at $-3/8V_{FS}$, and the first transition for the two MSBs in the 4-bit A/D converter occurs at $-9/32V_{FS}$. Since the coarse A/D converter has to function in both modes and the granularity of the voltages required is $1/32V_{FS}$, the number of unit resistors has to be increased to 32. Additionally, a level of multiplexing is required to select the appropriate reference depending on the mode of operation. This multiplexing is incorporated into the clock signals that control the access switches of the comparison circuit to reduce the number of series switching elements in the multiplexing path.

The voltage comparator is one of the crucial building blocks in an flash A/D converter. Offsets due to mismatches between threshold voltages lead to offset voltages at the comparator input. A fully-differential comparison technique with offset cancellation is shown in Figure 5-9 [Greb84]. During the sample mode (Φ_1 is high), the comparator is reset, and the sampling capacitor stores

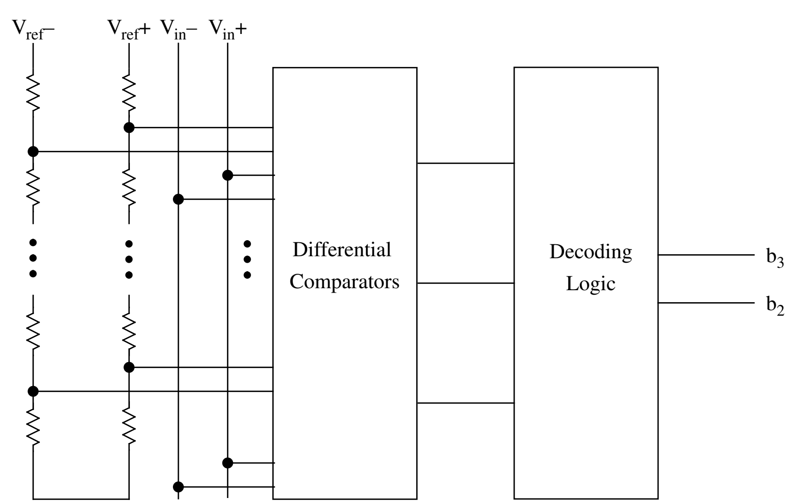

Figure 5-7: Coarse 2-bit A/D converter.

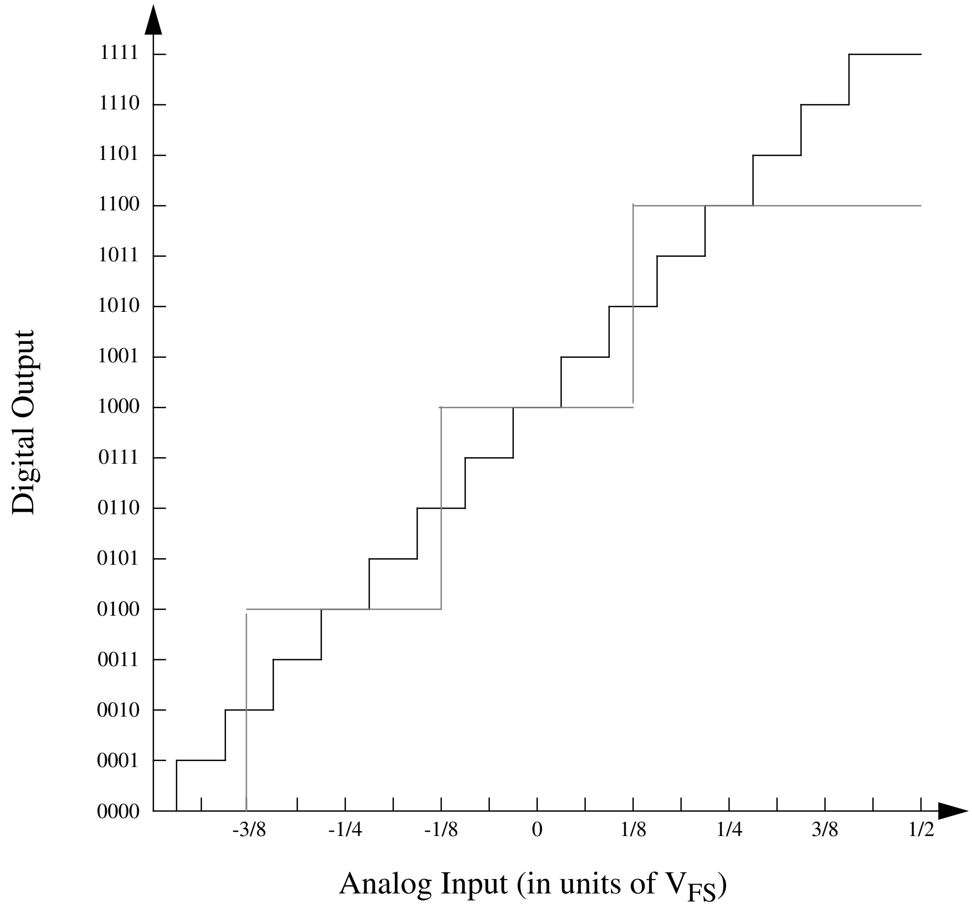

Figure 5-8: Transfer characteristic comparison between 2-bit and 4-bit converters.

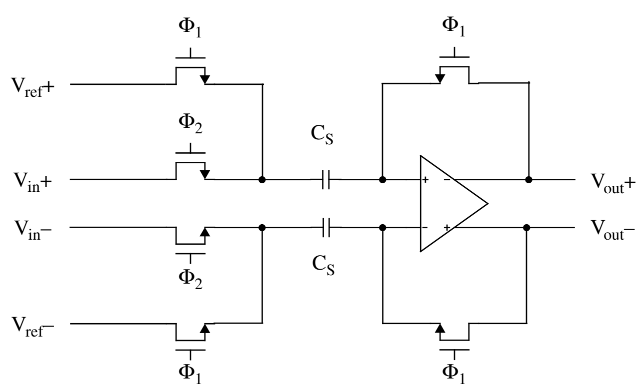

Figure 5-9: Fully-differential comparison circuit.

both the reference voltage and the comparator offset voltage simultaneously. During the hold mode (Φ_2 is high), the input voltage is sampled, and the difference between the input and reference voltages appears at the comparator inputs. This difference is amplified by the comparator to produce well-defined digital logic levels. Note that the offset voltage that is sampled during Φ_1 is subtracted from the actual input during Φ_2 to effectively cancel the offset voltage at the comparator input.

Figure 5-10 shows the single-stage fully-differential comparator used to perform the comparison; the design is similar to the one found in [Raza92]. The comparator itself consists of transistors M_1-M_4. Transistors M_1 and M_2 sense the voltage difference at the input terminals, and the difference is regenerated around M_3 and M_4 through the positive feedback. To avoid false regeneration and to reduce the input capacitance, delayed versions of the clocks are required.

The circuit operation can be described as follows. Initially, Φ_1 is high to sample the reference and offset voltages, and also reset the comparator. Next S_3-S_8 are turned off to end the sampling mode. Then S_1-S_2 are turned on to sample the input voltage, and a voltage difference (V_{in}-V_{ref}) develops at the input terminals of the comparator. Finally S_9 is turned off to allow regeneration around M_3 and M_4. Note that delayed versions of the clocks are used to account for the settling times of the input signals (the clock signal Φ_{1d1} is delayed by 50 ns with respect to Φ_1). Furthermore, by switching S_7 and S_8 off before switching S_1 and S_2 on, the input capacitance of

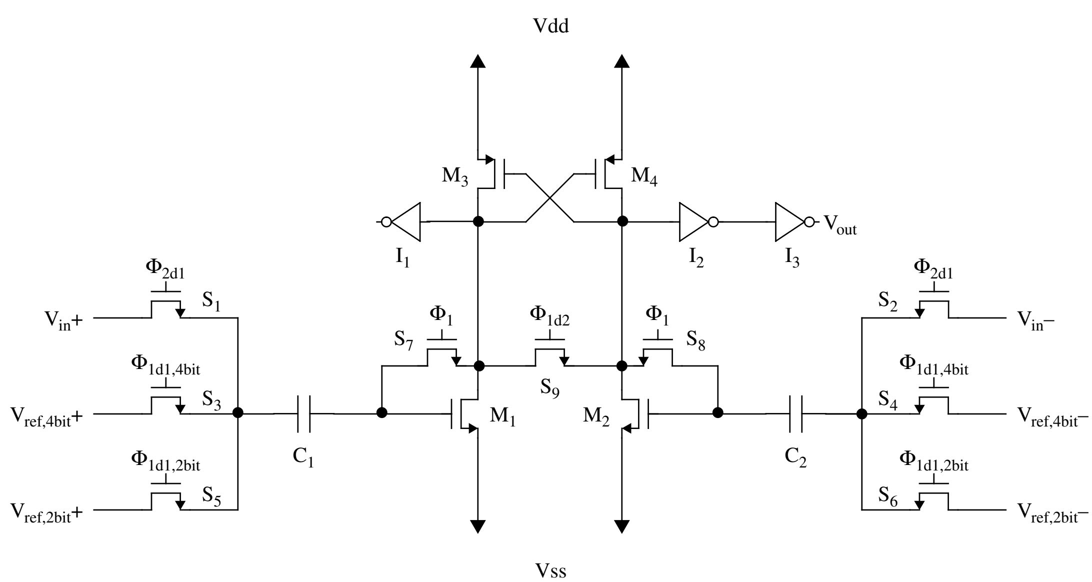

Figure 5-10: Fully-differential comparator schematic.

the circuit is significantly lowered because C_1 and C_2 then appear in series with the gate capacitances of the comparator. The output is buffered to obtain rail-to-rail voltages, and the inverter I_1 is used to balance the loading seen by the comparator.

A simple offset cancellation technique is used to reduce the offset voltage caused by mismatches in threshold voltages. This offset voltage is not completely cancelled due to the finite gain of the comparator. The residual offset voltage is given by

$$V_{OS} = \frac{V_{OS}'}{1 + A_d} \tag{5-2}$$

where V_{OS}' is the input offset voltage without offset cancellation, and A_d is the differential voltage gain of the comparator with the switch S_9 on. The differential gain A_d is given by

$$A_d = \frac{\dfrac{g_{mN}R_9}{2}}{1 - \dfrac{g_{mP}R_9}{2}} \tag{5-3}$$

where g_{mN} and g_{mP} are the small-signal transconductances of transistors M_1-M_2 and M_3-M_4, respectively, and R_9 is the small-signal resistance of S_9. Transistors M_1 and M_2 should have wide channels for high gain, while transistors M_3 and M_4 should have long channels for better matching. Following these design guidelines, transistors M_1-M_4 were sized to yield a differential gain of six. The comparator upon which this design is based exhibited offsets less than 5 mV [Raza92], which is sufficient to achieve the four-bit accuracy required.

As mentioned before, a level of multiplexing is required to select the appropriate reference voltages depending on the mode of operation. Switches S_3-S_4 are used during four-bit operation, and switches S_5-S_6 are used during two-bit operation. The multiplexing function is incorporated into the clocking circuitry that generates the two-phase non-overlapping clocks. Finally, the logic used to decode the thermometer code output from the comparators to a binary representation is composed of static CMOS gates.

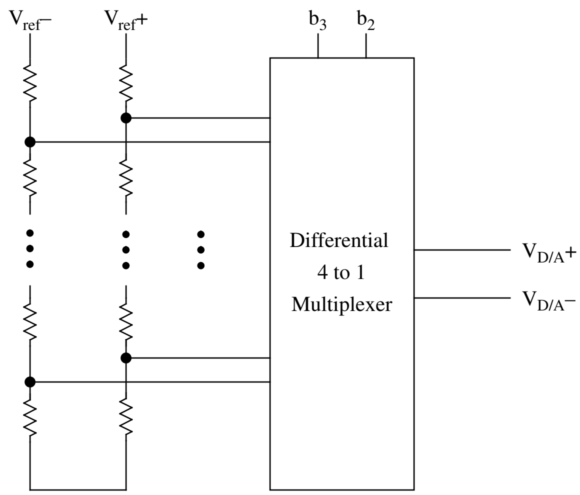

Figure 5-11: 2-bit D/A converter.

5.5.3 D/A Converter and Subtracter

The D/A converter takes the two most significant bits from the coarse A/D converter, and converts it to an analog voltage. Figure 5-11 shows the simple voltage-scaling D/A conversion scheme used [Greb84]. The digital bits control a multiplexer that selects the corresponding analog voltage from a resistor string. By using the same resistor string as the A/D converter, better matching is achieved. The analog voltages that are input to the multiplexer are ±13/32, ±5/32, ±3/32, and ±11/32. These voltages correspond to the midpoints of the transition levels in the coarse A/D converter. The subtracter, shown in Figure 5-12, takes the difference between the D/A output and the original analog input, and amplifies it by a factor of four (C_S=4C_I) before passing it to the fine A/D converter. The capacitors are laid out in a common centroid arrangement using

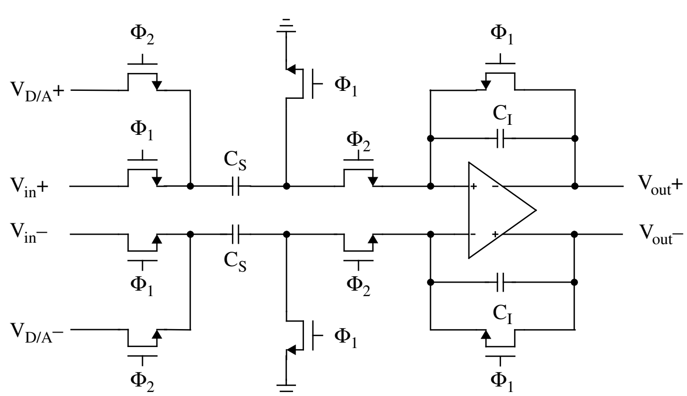

Figure 5-12: Subtracter circuit.

0.25 pF unit capacitors to achieve better matching. The OTA described in Section 5.5.1 is used to build the subtracter circuit. The output of the subtracter circuit settles to an accuracy of 0.1% in less than 25 ns for a 2V differential output and 0.5 pF loading.

5.5.4 Fine A/D Converter

The fine A/D converter has greater accuracy requirements than the coarse ADC, which suggests the need for higher resolution comparators plus better offset cancellation. However, since this design only requires four-bit resolution, and the accuracy of the coarse A/D converter meets the four-bit requirement; the circuits in the fine A/D converter are identical to those used in the coarse A/D converter. The coarse and fine A/D converters differ only by the reference voltages that are compared against.

5.6 Clocking

The reconfigurable four-bit A/D converter requires two clocks to control the coarse and fine sections, Aclk and Bclk, respectively. The timing diagrams for the clocks in the two modes of operation are shown in Figure 5-13. In two-bit mode, the two clocks both have a 50% duty cycle; however, in four-bit mode, Bclk has an 80% duty cycle. The A/D conversion in the fine stage must be delayed until the amplified residue is available from the subtracter. The sampling of the input signal occurs when the clocks are high, and the conversion is performed on the held signal when the clocks are low. These single phase clocks are converted into two-phase non-overlapping clocks by on-chip two-phase clock generators. Furthermore, delayed versions of the clocks are required to allow signals to settle before they are processed by the following stage. To provide

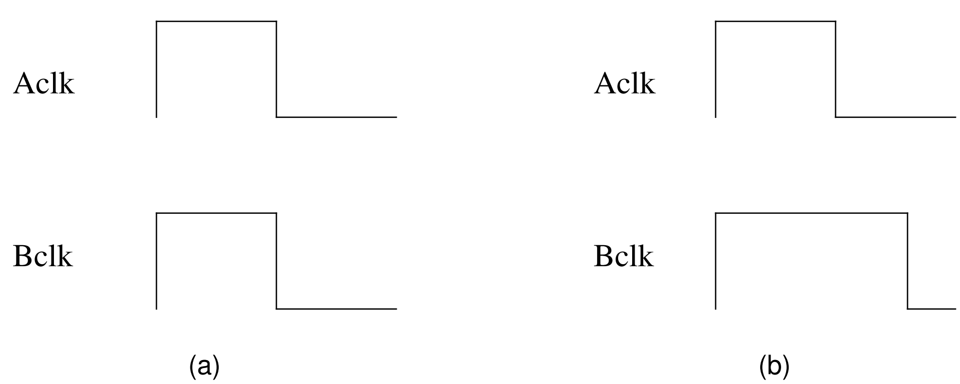

Figure 5-13: Clocks of A/D converter in (a) two-bit mode (b) four-bit mode.

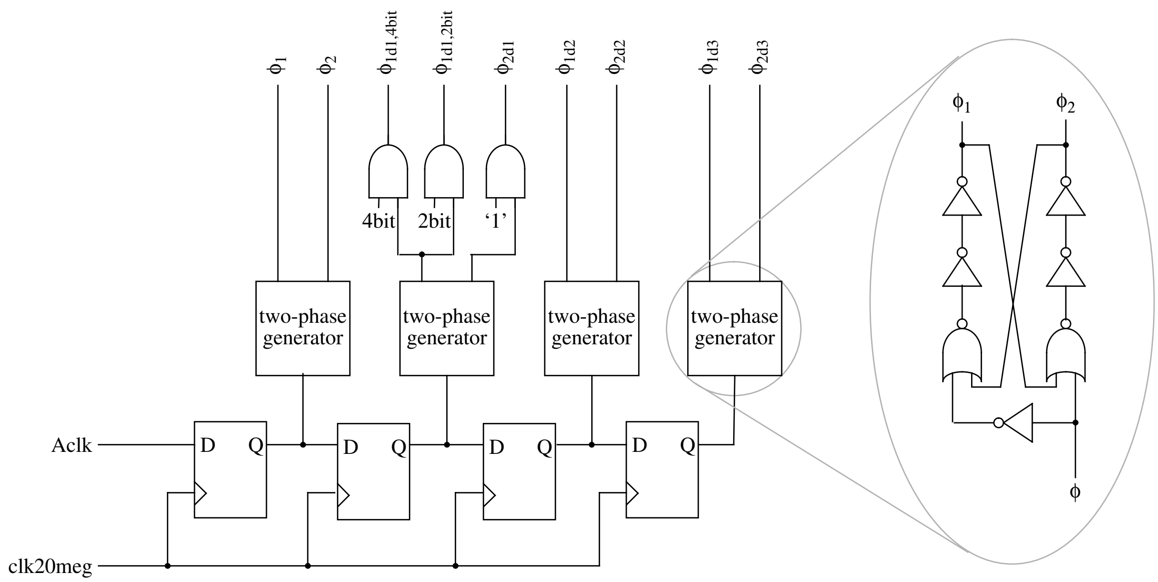

Figure 5-14: Clock generation circuit for coarse A/D converter and subtracter.

good controllability, a digital solution is used for clock generation. A 20 MHz clock, in conjunction with flip-flops and two-phase generators, is used to generate 50 ns delays. Additionally, the selection of the appropriate reference voltages in the flash A/D converters is accomplished in the clocking circuitry by gating the clock that controls the sampling switches with the configuration bit that selects the mode of operation. Figure 5-14 shows the clock generation circuit for the coarse A/D converter and the subtracter. The figure also shows an expanded view of the two-phase clock generator. The inverters in the feedback path are used to ensure that the two-phase clocks do not overlap. The clock generation circuit for the fine A/D converter is very similar.

5.7 Floorplan

The reconfigurable A/D converter measures 554 μm x 1615 μm, and its floorplan is shown in Figure 5-15. The building blocks are laid out as a one dimensional array in the vertical direction because the horizontal dimension was chosen to match the reconfigurable D/A converter. The clock generation circuits are located at the top and bottom of the layout. The layout of the interior blocks proceeds in the same manner as the signal flow. Higher resolutions can be obtained by increasing the resolution of the coarse and fine A/D converters. However, there will be a significant increase in area since the number of comparators in flash architectures is on the order

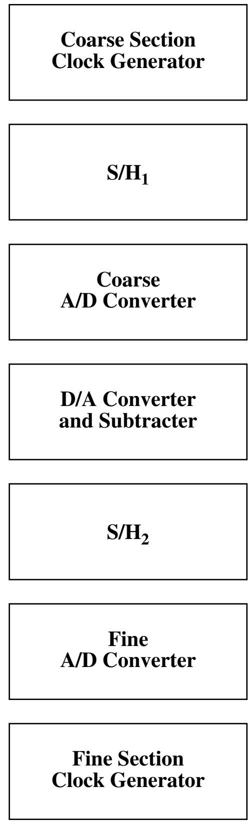

Figure 5-15: Floorplan of reconfigurable A/D converter.

of 2^N. Furthermore, the increased accuracy requirements lead to a much more complex circuit design.

5.8 Simulation Results

The extracted layout of the reconfigurable A/D converter was simulated using HSPICE. Figure 5-16(a) and Figure 5-16(b) show the output response of the A/D converter to a differential analog voltage that is ramped up from -1 V to 1V for two-bit mode and four-bit mode, respectively. To simulate the non-linearity errors, the exact transition points would have to be determined, which would have taken too many simulations. Instead, analog input voltages ±10 mV (±0.08 LSB) from the transition points are applied, and the digital output is recorded. If all the digital codes are correct, then the maximum integral non-linearity error is within ±0.08 LSB. The maximum differential non-linearity error has an upper bound equal to twice the maximum integral non-linearity error. The simulation results are presented in Table 5-2. Non-linearity errors caused by mismatching component geometries and threshold voltages are absent during simulation;

Item	Value
Integral Non-linearity	±0.08 LSB
Differential Non-linearity	±0.16 LSB
Conversion Rate	1 MS/s
Power	42 mW

Table 5-2: Simulation results for the fully-differential reconfigurable A/D converter.

therefore, we expect larger non-linearity errors from the experimental results of the fabricated circuit.

5.9 Experimental Results

A single-ended version of the reconfigurable A/D converter was fabricated and tested. Its performance is shown in Table 5-3 including both simulation and experimental results. The output response to a ramp waveform for two-bit mode and four-bit mode are shown in Figure 5-17(a) and Figure 5-17(b), respectively. In the single-ended design, offset cancellation was not implemented, which led to linearity errors. We expect better performance in the fully-differential design because offset cancellation was implemented for the comparators, and higher gain opamps were used.

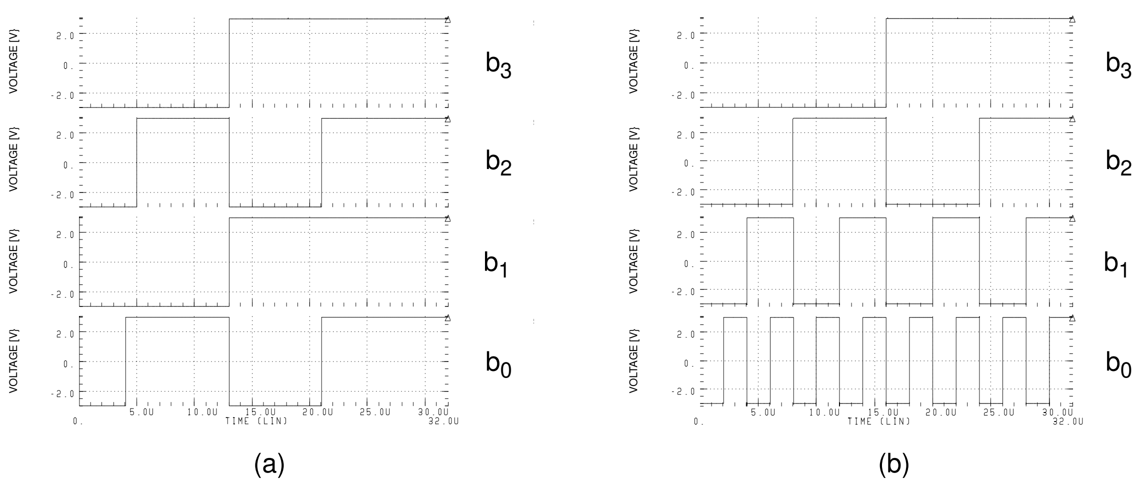

Figure 5-16: Simulation results for the fully-differential reconfigurable A/D converter in (a) two-bit mode (b) four-bit mode.

(a) (b)

Figure 5-17: Experimental results for the single-ended reconfigurable A/D converter in (a) two-bit mode (b) four-bit mode.

Item	Simulated Value	Experimental Value
Integral Non-linearity	±0.16 LSB	±0.21 LSB
Differential Non-linearity	±0.32 LSB	±0.33 LSB
Conversion Rate	1 MS/s	1 MS/s
Power	3.9 mW	5.3 mW

Table 5-3: Simulation and experimental results for the single-ended reconfigurable A/D converter.

5.10 Summary

This chapter described the design and implementation of the reconfigurable bipolar 4-bit A/D converter that is used in MADAR. The A/D converter uses a two-step approach to realize an area-efficient design, and is still capable of performing data conversion at a high speed (1 MHz). Simulation results for a fully-differential version are presented, and experimental results for an earlier single-ended version are provided.

The next chapter will describe the integration of the individual components (digital array, analog array, D/A converter, and A/D converter) to form MADAR. Also, the embedding of a demonstration circuit will be presented.

Chapter 6

MADAR

6.1 Introduction

In this chapter, we will present the final specifications for MADAR, and discuss the simulation strategy for the chip. Also, we will show how one of the demonstration circuits is embedded into MADAR, and show the simulation results. Finally, we will discuss what we have learned from the design and implementation of a field-programmable mixed-analog-digital array.

6.2 MADAR Specifications

The final MADAR chip was realized by combining all the layouts described in the previous sections: the analog array, the digital array, and the interface that contains the reconfigurable data converters. The chip, implemented in 1.2 µm CMOS, measures 7292 µm x 4279 µm, and its floorplan and corresponding pad assignment are shown in Figure 6-1. The specifications of MADAR are summarized in Table 6-1. The core area measures 6346 µm x 3224 µm; the digital array occupies 3076 µm x 3224 µm, the analog array occupies 2483 µm x 2528 µm, and the interface occupies 554 µm x 2485 µm. MADAR has a total of 86 I/O pins. Forty-four pins are used by the digital section, thirty-six by the analog section, and six by the interface. The pin definitions are described in Appendix A.

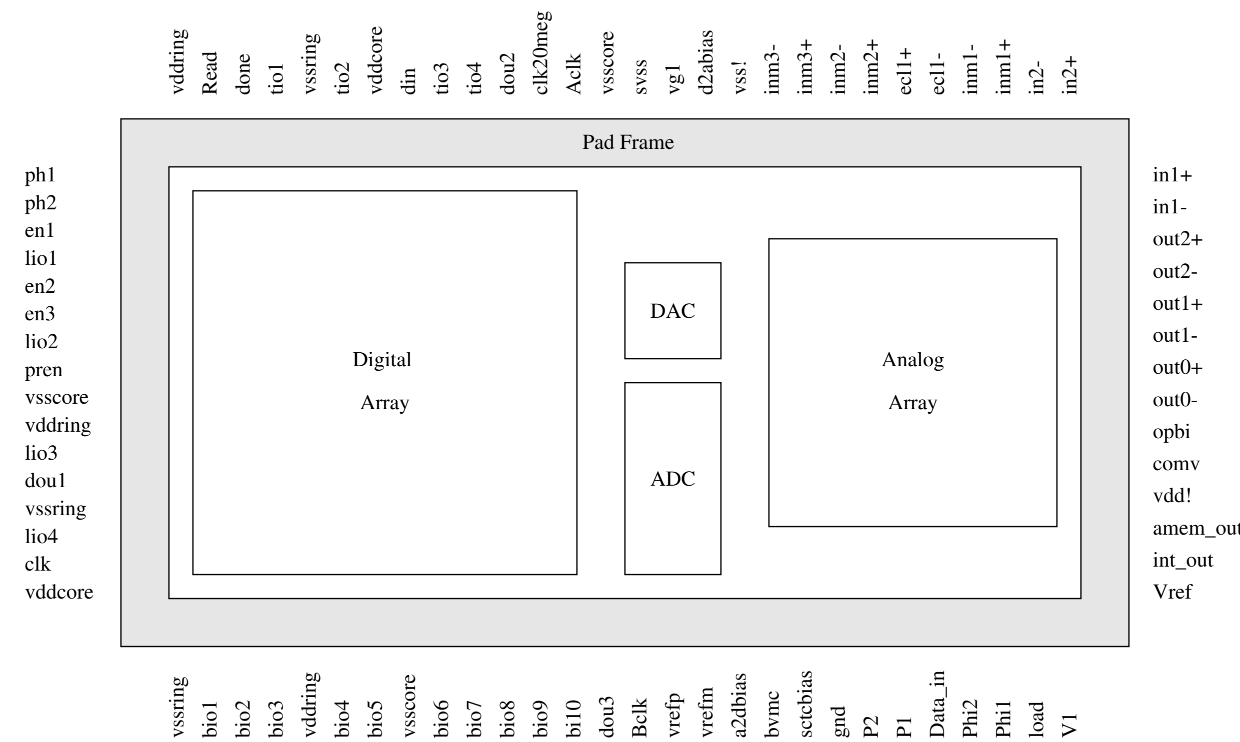

Figure 6-1: Floorplan and pad assignment.

Item	Value
Core Area	6346 µm x 3224 µm
Die Area	7292 µm x 4279 µm
Pins	86
Power Supply	±3 V
Configuration Bits	2471

Table 6-1: Specifications for MADAR.

A total of 2471 bits are required to program MADAR with the following distribution: 2116 bits for the digital section, 353 for the analog section, and 2 for the interface. The digital section is programmed using a serial-parallel approach, while the analog section uses a single shift register. The two configuration bits of the interface are connected to the end of the shift register in the analog section.

The power to all of the circuitry is provided by ±3 V supplies because the original analog array was designed to operate with these voltages. A conventional 5 V power supply with an analog ground situated at 2.5 V can be used, but we would have to redesign the opamps in the analog array for 5 V operation. Separate power pins are used to supply the analog and digital circuitry. Also, a dedicated VSS pin is used to bias the substrate of the interface, and a guard ring that surrounds the analog array. Finally two on-chip decoupling capacitors are used to reduce power supply noise.

6.3 Simulation Strategy

Due to limitations in the computing resources and CAD tools, the entire chip could not be simulated at once. Therefore, the following three sections were simulated independently using the appropriate CAD tool: the digital array, the interface, and the analog array. The functionality of the digital array is verified using a circuit-level simulator called AWSIM [Lewi92] for the following reasons. First, the digital array consists of more than 20,000 transistors plus many parasitic capacitors. Simulation of this many components using HSPICE would take too much time and memory. Second, since the signals are digital, there is no need for the accuracy offered by HSPICE. The verification of the interface, on the other hand, demands much greater accuracy because the signals are analog. Since the interface contains a more manageable number of transistors (1000), HSPICE is used to perform the simulation. The analog array layout incurred only minor changes; therefore, it was not simulated because it has already been fabricated and tested. Instead, after the entire chip was extracted, the shift register chain of the analog array and the interface was verified using AWSIM.

This approach, where the three main parts are separately verified, is feasible because there is only a total of eight routing connections between the digital array and the interface. Similarly, there are eight routing connections between the interface and the analog array. There are three additional wires between the interface and the analog array that are used to connect the configuration bits of the interface to the end of the shift register used to program the analog array.

6.4 Circuit Embedding

The dual-slope A/D converter in Section 2.2 will be used to illustrate the embedding of a mixed-signal circuit into MADAR. Figure 6-2(a) shows the schematic for the dual-slope A/D converter, and Figure 6-2(b) shows how the circuit is embedded into the chip. The counter is mapped into tile 1, the register is mapped into tile 3, and the rest of the digital logic is mapped into tiles 2 and 4. Signals that propagate in the digital-to-analog direction must go through tile 2, and signals in the reverse direction must pass through tile 4. The programming of the crossbar interconnect in the analog array is indicated by the solid circles and squares. CAB1 is used for the integrator and CAB0 is used for the comparator. The input signals V_{in} and V_{ref}, and the output signals b_2, b_1, and b_0 are all connected to pins.

6.4.1 Simulation Results

The circuit was simulated using a mixed-mode simulator called Saber. The digital circuitry is modelled behaviorally, while the analog portion is modelled at the circuit level. Figure 6-3shows the output response of the dual-slope A/D converter to an analog input staircase waveform. The resulting digital output counts up from 000 up to 111. The maximum conversion rate of this 3-bit A/D converter is limited by the maximum clock frequency of the digital array. If we use a conservative estimate for the maximum clock frequency (25 MHz), we can get an A/D conversion rate of 1.5 MHz.

6.5 Discussion

The implementation of MADAR has provided valuable information in the design of field-programmable mixed-analog-digital arrays. Using a small collection of mixed-signal circuits, we were able to determine the type of connections required between the analog and digital functions. We also notice that the number of connections between the two arrays is typically less than the number within the arrays. Therefore, the routing resources in the interface should be minimized. In MADAR, there are no resources devoted to the routing function such as connection blocks and switch blocks. Instead, fixed connections are used to connect the two arrays, and the routing resources within the arrays are used, which greatly reduces the area required for the interface. Moreover, the area of the interface should be significantly less

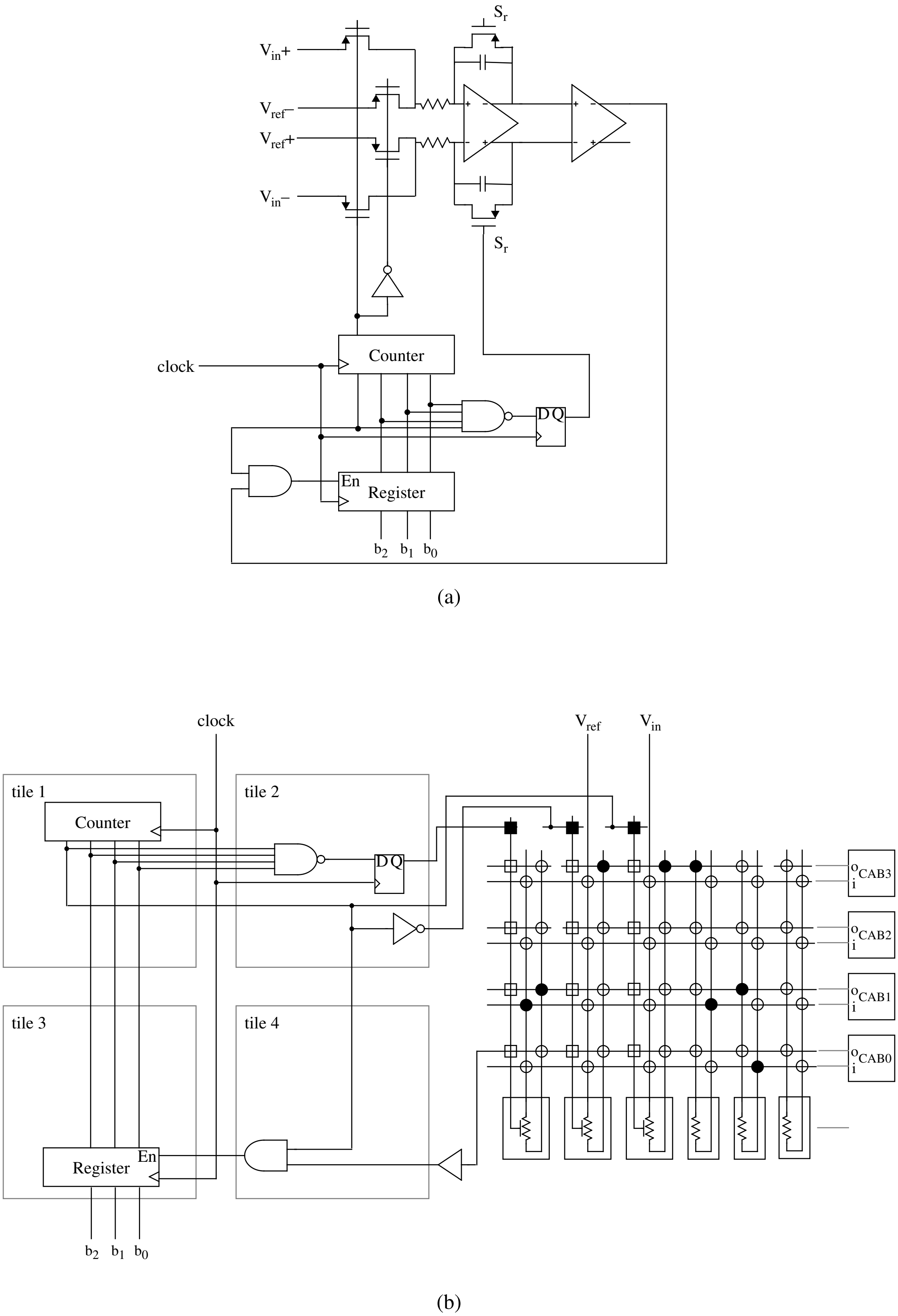

Figure 6-2: Embedding of dual-slope A/D converter into MADAR (a) dual-slope A/D converter schematic (b) embedding into MADAR.

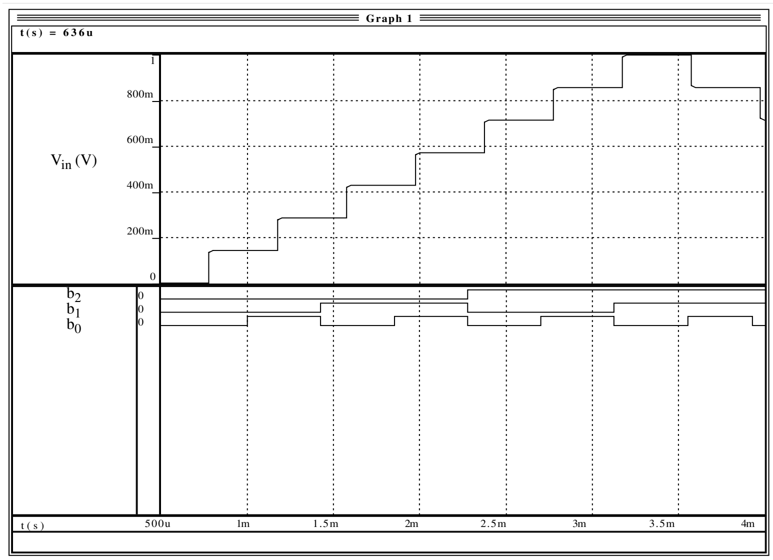

Figure 6-3: Saber simulation of dual-slope A/D converter.

compared to the analog and digital arrays. In MADAR, the interface consumes 6.7% of the area, while the analog and digital arrays consume 30.7% and 48.5%, respectively.

Further examination of the demonstration circuits reveals that the circuitry at the border of a mixed-signal system is very similar. On the digital side, many of the circuits are datapath-oriented such as counters, registers, comparators, etc. This suggests using either dedicated reconfigurable blocks that can provide a fixed number of functions, or more generally, a datapath FPGA that can provide a high degree of flexibility as described in [Cher94]. More area-efficient architectures for a digital array may be realized by building a heterogeneous digital array that includes LEGO tiles for control functions, and datapath tiles for datapath-oriented functions such as digital signal processing.

On the analog side, the comparator is a key component when signals propagate in the analog-to-digital direction because the comparator produces a binary output. Therefore, fast and accurate comparators with latching capability should be made available. In the digital-to-analog direction, the switch is a major element; therefore, some columns of the analog array could be used specifically as switches. These switches would be implemented using short-channel transistors to minimize the on resistance. These switch columns would therefore require significantly less area than the resistor columns since long-channel transistors and the circuits used to generate the voltages that set the resistance value are not required.

Noise immunity is a main design issue in a mixed-signal chip. In MADAR, the noise was suppressed in a number of ways. First, the analog and digital circuitry were isolated by physical separation. Second, all the analog circuitry is fully-differential so that the noise appears as a common-mode disturbance that can be rejected. Third, separate power supply pins were used for the analog and digital arrays. Lastly, guard rings that are connected to a quiet low-impedance supply were used to shield the analog circuitry from substrate noise. Processing technologies that are more suitable for mixed-signal chips are available. In such processes, the substrate consists of a heavily-doped bulk and a lightly-doped epitaxial layer deposited on the surface. The majority of the noise propagates through the lower resistance of the bulk, thus the epitaxial layer, which contains the transistors, remains quiet.

6.6 Status

We intend to send the MADAR chip to CMC for fabrication in November 1994.

6.7 Summary

This chapter has described the final specifications for the field-programmable mixed-analog-digital array called MADAR. An example is given to show how a circuit is embedded into the chip, and simulation results are provided. We believe that the MADAR prototype chip proves the concept of a field-programmable mixed-analog-digital array. By implementing the mixed-signal circuits on the fabricated prototype, we will demonstrate the feasibility of reconfigurable single-chip systems. The MADAR chip will be sent for fabrication in November, 1994.

The next chapter concludes this thesis and provides some suggestions for future research.

Chapter 7

Conclusions and Future Research

7.1 Conclusions

This thesis has described the complete design and implementation of the first field-programmable mixed-analog-digital array, called MADAR. This design included field-programmable analog and digital arrays, and an interface that contained reconfigurable data converters. The main focus was on the design of the interface that connects the analog and digital arrays. As a starting point, a set of small mixed-signal circuits was used to determine the resources required for the arrays and the interface. With this information, the architecture of MADAR was designed.

Data converters are essential in a field-programmable mixed-analog-digital array, because it would be area-inefficient to build them out of the resources from the analog and digital arrays, and only low conversion rates would be attainable. Therefore, dedicated data converters have been designed and implemented in MADAR. The data converters were area-efficient, and have resolution (4-bit) and a conversion speed (1 MHz) that are compatible with the analog and digital arrays. Furthermore, the data converters can be configured as either a single 4-bit converter or two 2-bit converters to allow for some flexibility in the interface.

MADAR can implement all of the mixed-signal demonstration circuits described in Section 3.2. In this way, the concept of a field-programmable mixed-analog-digital array has been demonstrated.

7.2 Future Work

The area of mixed-signal circuits is very broad as there are many different applications. In this thesis, only a very small set of circuits was considered. Therefore, a survey of commercial mixed-signal chips in various applications is required to better determine the resources needed. This survey should include information on the amount of analog circuitry in relation to the amount of digital circuitry, the number and types of interconnections, and the number of data converters. Also, information concerning the resolution, speed, and area of the data converters is important. It may be necessary to have different families of field-programmable mixed-analog-digital arrays each tailored to a specific application. For example, the data converters in audio applications require high resolution and moderate speed, while the converters in video applications require lower resolution but higher speeds.

Since the digital array in MADAR was so small, we chose to use LEGO tiles, which provided the maximum flexibility. However, in a larger design, better architectures may be realized by building a heterogeneous digital array that includes LEGO tiles for control functions, and datapath tiles for datapath-oriented functions such as digital signal processing.

The issue of routing has not been dealt with in this thesis. The MADAR architecture primarily uses the routing resources already available in the analog and digital arrays. Whether routing is required in the interface is arguable, and if it is, then how much routing is required? Again, an analysis of netlists from large commercial designs would reveal the number of interconnections needed between the analog and digital circuits. If this number is small, the benefit gained by providing routing in the interface is outweighed by the additional area needed for the switches and programming bits.

Currently, the programming of MADAR is separated because the analog and digital arrays use different programming styles, serial and serial-parallel, respectively. In the future, a uniform programming method should be used, which will reduce the number of programming pins.

The data converters in MADAR have been designed to be compatible with the analog and digital arrays. Typically, data converters are designed to meet the needs of a specific application. Often, there exists several architectures that can satisfy the requirements. We have chosen fast area-efficient architectures that are easily expandable to higher resolutions. But even within these architectures, there are trade-offs between speed, resolution, area, and power. Further work is required to improve the performance of the data converter in MADAR either by better circuit design or exploring different architectures. For example, to reduce the area, the two-step approach used to design the reconfigurable A/D converter can be generalized to an N-step or pipelined A/D converter. Several area-efficient pipelined A/D converter designs have already been implemented [Conr93] [Lewi87].

In a field-programmable system, we have added another parameter to the design of data converters, reconfigurability. In our case, two data converters could be combined to provide higher resolution. Should this feature be generalized so that N 1-bit converters can be combined to form 1 N-bit converter or two N/2-bit converter and so on? In a prototyping environment, this is a useful feature when the number of converters required may not be known.

To achieve a true field-programmable single-chip system, several other important components should be included such as memories, sensors, and line drivers. This may be possible in the near future with improvements in process technology and shrinking geometries. Currently, the performance bottleneck seems to be the bandwidth of the analog array, which can achieve speeds in the hundred kHz range. However, with process technologies such as BiCMOS, the speed of the analog circuitry can be improved by using higher bandwidth bipolar transistors. The digital array is capable of speeds in the ten MHz range. Thus, the current version of MADAR can be used in audio and instrumentation applications. By increasing the speed of the analog arrays, digital arrays and data converters, the chip can be used in video and high-speed telecommunication applications.

Another important area of research is the development of CAD tools and a methodology for field-programmable mixed-analog-digital arrays. The CAD tools would have to include design capture, mixed-signal simulators, and technology mappers. In addition, simulators to assess the effect of substrate noise are needed. Moreover, tools to help develop intelligent partitioning between the analog and digital functions would be beneficial.

References

[Agar94] Aditya A. Agarwal and David M. Lewis, "Routing Architectures for Hierarchical Field Programmable Gate Arrays", *FPGA'94*, Feb. 1994.

[Anal92] Analogy Inc., *Saber User's Manual*, Beaverton, OR., 1992.

[B&B89] B & B Consultants, *The Analog ASIC Market*, Electronic Trend Publications, 1989.

[Brit93] Barry K. Britton, Dwight D. Hill, William Oswald, Nam-Sung Woo and Satwant Singh, "Optimized Rconfigurable Cell Array Architecture for High-Performance Field-Programmable Gate Arrays", *Proc. 1993 Custom Integrated Circuits Conference*, pp. 7.2.1- 7.2.5, March 1993.

[Brow92] S. Brown, R. Francis, J. Rose, and Z. Vranesic, *Field Programmable Gate Arrays*, Kluwer Academic Publishers, 1992.

[Bult92] Klaas Bult, and Govert Geelen, "An Inherently Linear and Compact MOST-Only Current-Division Technique", *IEEE JSSC*, vol. 27(12), pp. 1730-1735, Dec. 1992.

[Bult94] Klaas Bult, "Basic CMOS Circuit Techniques", in *Analog VLSI Signal and Information Processing*, Mohammed Ismail and Terri Fiez, Ed., McGraw-Hill Inc., pp. 12-56, 1994.

[Chow93] Paul Chow, Soon Ong Seo, Kevin Chung, Gerard Paez and Jonathan Rose, "A High-Speed FPGA Using Programmable Mini-tiles", *Proc. 1993 Symposium of Integrated Systems*, March 1993.

[Cher94] Don Cherepacha, and David Lewis, "DP-FPGA: An FPGA Architecture Optimized for Datapaths",

[Conr93] Cormac S. G. Conroy, David W. Cline, and Paul Gray, "An 8-b 85-MS/s Parallel Pipeline A/D Convertor in 1-um CMOS", *IEEE JSSC*, vol. 28(4), pp. 447-454, Apr. 1993.

[Cope91] Miles A. Copeland, "VLSI for Analog/Digital Communication", *IEEE Communications Magazine*, vol. 29, pp. 25-30, May 1991.

[Dupu90] S. Dupuie and M. Ismail, "High Frequency CMOS Transconductors", *Analogue IC Design: the Current-Mode Approach*, C. Toumazou, F.J. Lidgey and D.G. Haigh, Ed., Peter Peregrinus Ltd., pp. 181-238, 1990.

[Gray94] Paul R. Gray and Robert R. Neff, "Analog-Digital Conversion Techniques for Telecommunications Applications", in *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Second Edition, Jose E. Franca and Yannis Tsividis, Ed., Prentice Hall, pp. 289-316, 1994.

[Greb84] Alan B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, John Wiley & Sons, 1984.

[Horo80] Paul Horowitz, *The Art of Electronics*, Cambridge University Press, 1980.

[Hsie90] H. Hsieh, K. Duong, J.Ja, R. Kanazawa, L. Ngo, L. Tinkey, W. Carter and R. Freeman, "Third-Generation Architecture Boosts Speed and Density of Field-Programmmable Gate Arrays", *Proc. 1990 Custom Integrated Circuits Conference*, pp. 31.2.1 - 31.2.7, May 1990.

[Lee91] E. Lee and P. Gulak, "A CMOS field programmable analog array", *1991 IEEE ISSCC Dig. Technical Papers*, pp. 186-187.

[Lee92] E. Lee and P. Gulak, "Field Programmable Analogue Array Based on MOSFET Transconductors", *Electronics Letters*, vol. 28(1), pp. 28-29, Jan. 1992.

[Lee94] E. Lee and P. Gulak, "A Transconductor-Based Field-Programmable Analog Array", submitted to JSSC, 1994.

[Lewi87] Stephen H. Lewis and Paul R. Gray, "A pipelined 5-Msample/s 9-bit Analog-to-Digital Converter", *IEEE JSSC*, vol. sc-22(6), pp. 954-961, Dec. 1987.

[Lewi92] David M. Lewis, "A Compiled-Code Hardware Accelerator for Circuit Simulation", *IEEE Transactions on Computer-Aided Design*, Vol. No. 5, May 1992.

[Malo91a] Franco Maloberti, "Data Converters", in *Analogue-Digital ASICs circuit techniques, design tools, and applications*, R. Soin, F. Maloberti and J. Franca, Ed., Peter Peregrinus Ltd., pp. 117-142, 1991.

[Malo91b] Franco Maloberti, and Paul O'Leary, "Over Sampling Converters", in *Analogue-Digital ASICs circuit techniques, design tools, and applications*, R. Soin, F. Maloberti and J. Franca, Ed., Peter Peregrinus Ltd., pp. 143-172, 1991.

[Meta91] Meta-Software Inc., *HSPICE User's Manual*, Campbell, CA., 1991.

[Nomu94] Masahiro Nomura, Masakazu Yamashina, Junichi Goto, Toshiaki Inoue, Kazumasa Suzuki, Masato Motomura, Youichi Koseki, Benjamin S. Shih, Tadahiko Horiuchi, Nobuhisa Hamatake, Kouichi Kumagai, Tadayoshi Enomoto, and Hachiro Yamada, "A 300-MHz 16-b 0.5-mm BiCMOS Digital Signal Processor Core LSI", *IEEE JSSC*, vol. 29(3), pp. 290-297, Mar. 1994.

[Ohta90] Mitsuhiko Ohta, Kiyoshi Kohiyama, Noriaki Tahara, Koi Sugihara, Fumitaka Asami, Osamu Kobayashi, Yoji Hino, and Toshihiko Akiba, "A Single-Chip CMOS Analog/Digital Mixed NTSC Decoder", *IEEE JSSC*, vol. 25(6), pp. 1464-1469, Dec. 1990.

[OLea91] Paul O'Leary, "Practical Aspects of Mixed Analogue and Digital Design", in *Analogue-Digital ASICs circuit techniques, design tools, and applications*, R. Soin, F. Maloberti and J. Franca, Ed., Peter Peregrinus Ltd., pp. 213-238, 1991.

[Raza92] Behzad Razavi, and Bruce A. Wooley, "A 12-b 5-MSample/s Two-Step CMOS A/D Converter", *IEEE JSSC*, vol. 27(12), pp. 1667-1678, Dec. 1992.

[Sedr94] Adel S. Sedra, and Martin Snelgrove, "Switched-Capacitor Filter Synthesis", in *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Second Edition, Jose E. Franca and Yannis Tsividis, Ed., Prentice Hall, pp. 213-250, 1994.

[Soin91] Randeep Singh Soin, Steve Morris, and Franco Maloberti, "Some Applications of Mixed Signal ASICS", in *Analogue-Digital ASICs circuit techniques, design tools, and applications*, R. Soin, F. Maloberti and J. Franca, Ed., Peter Peregrinus Ltd., pp. 239-272, 1991.

[Stan94] Balsha R. Stanisic, Nishath K. Verghese, Rob A. Rutenbar, L. Richard Carley, and David J. Allstot, "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis", *IEEE JSSC*, vol. 29(3), pp. 226-238, Mar. 1994.

[Su93] David K. Su, Marc J. Loinaz, Soichi Masui, and Bruce A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE JSSC*, vol. 28(4), pp. 420-430, Apr. 1993.

[Tsiv94] Yannis P. Tsividis, and Venugopal Gopinathan, "Continuous-Time Filters" in *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Second Edition, Jose E. Franca and Yannis Tsividis, Ed., Prentice Hall, pp. 177-212, 1994.

[Univ94] University of Toronto Analog IC Group EA104, *Automatic Opamp Layout Generator*, 1994.

[Wolf83] Stanley Wolf, *Guide to Electronic Measurements and Laboratory Practice*, Prentice-Hall Inc., 1983.

[Yots93] Michio Yotsuyanagi, Toshiyuki Etoh, and Kazumi Hirata, "A 10-b 50-MHz Pipelined CMOS A/D Converter with S/H", *IEEE JSSC*, vol. 28(3), pp. 292-300, Mar. 1993.