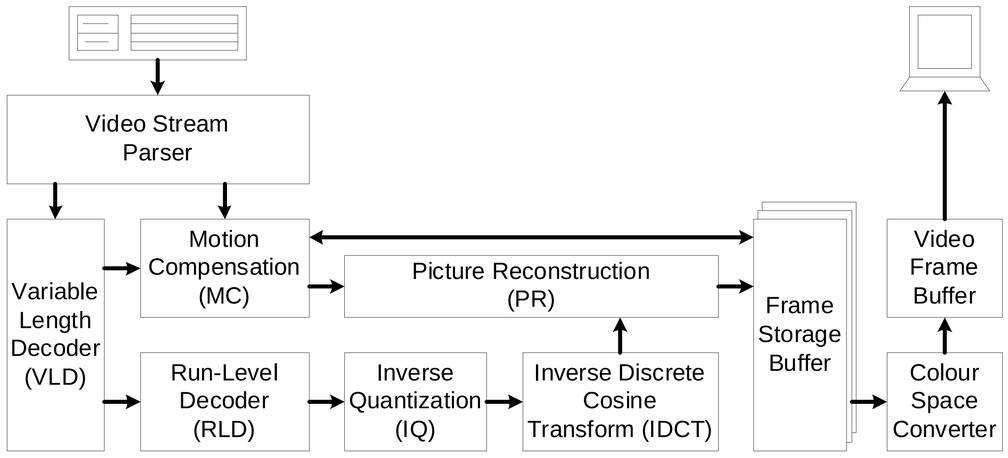
Designing an FPGA SoC using a Standardized IP Block Interface

Lesley Shannon, Blair Fort, Arun Patel, Samir Parikh, Manuel Saldana, and Paul Chow
Department of Electrical and Computer Engineering University of Toronto, Canada {lesley, fort, apatel, parikh, msaldana, pc}@eecg.toronto.edu

Application: MPEG-1 Video Decoder to RGB Display

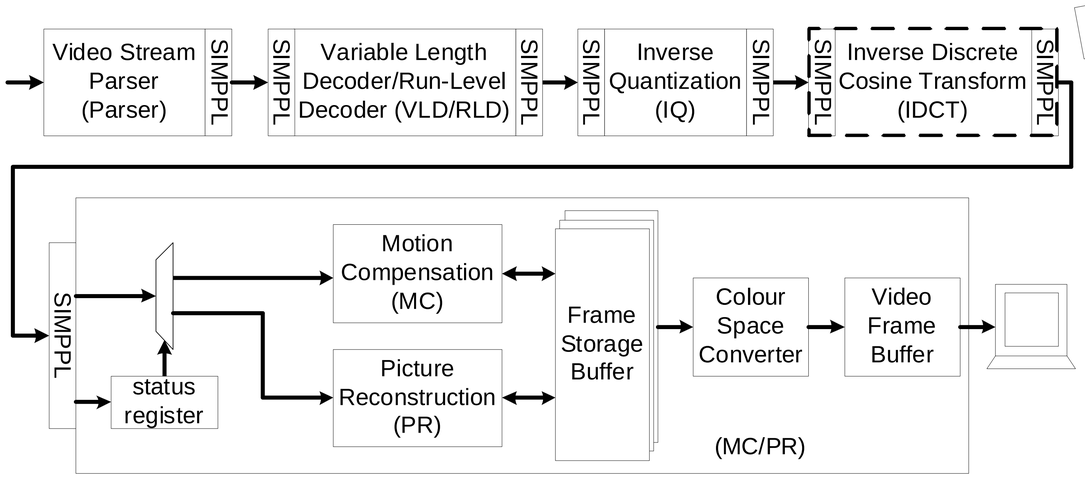
Datapath Block Diagram



FPGAs are now large enough to implement complex systems on a single chip, such as the MPEG-1 video decoder.

Previous work introduced the idea of modelling SoCs as **S**ystems **I**ntegrating **M**odules with **P**redefined **P**hysical **L**inks (SIMPPL).

SIMPPL Implementation Block Diagram

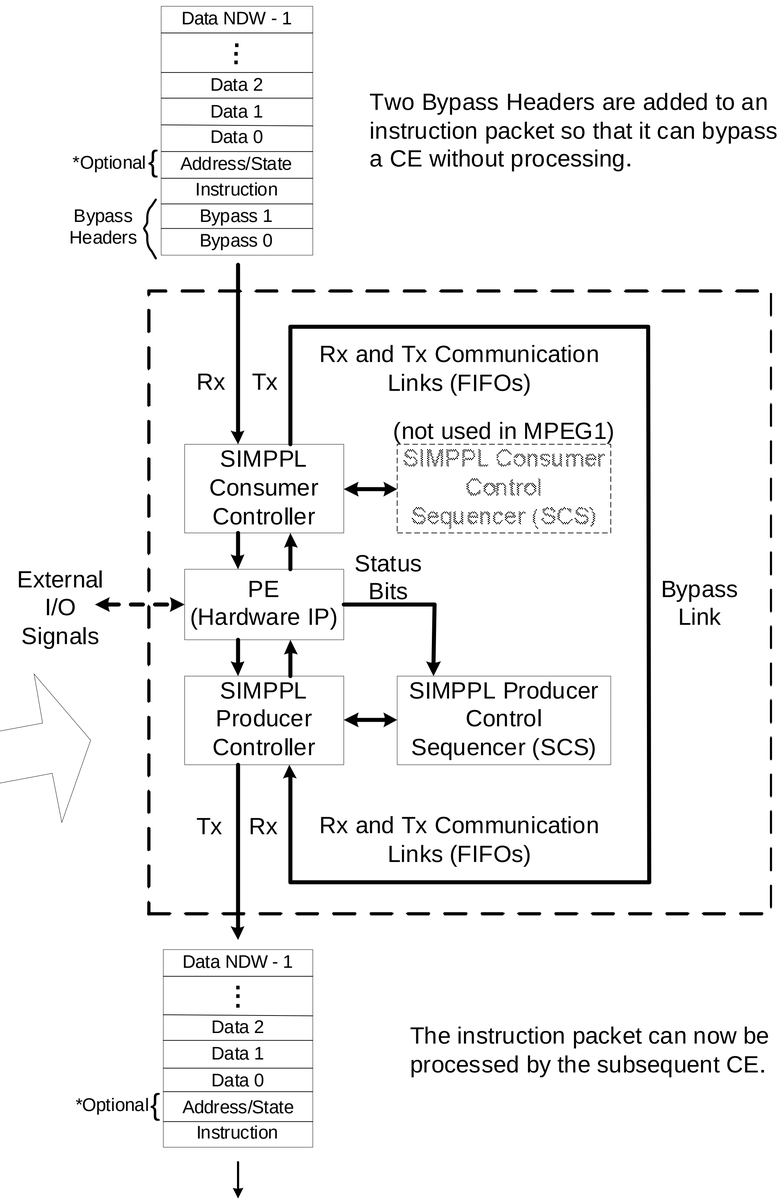


SIMPPL models SoCs as a network of Computing Elements (CEs) interconnected with point-to-point links.

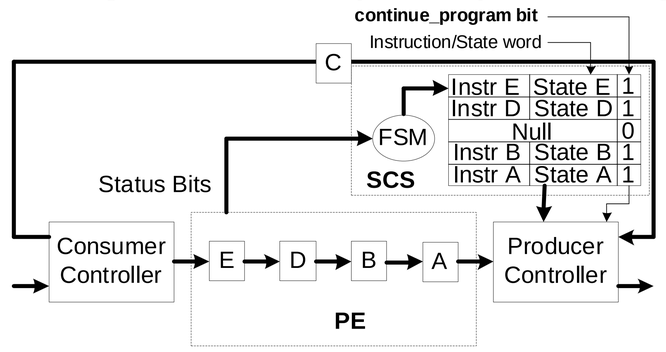
The CE's architecture can be adapted to application specific requirements.

Computing Element Architecture

Pipelining a Computing Element



Maintaining Order with multiple data packets in flight.



The continue_program bit ensures allows the user to vary the priority of instruction execution between the SCS and the Rx Link.

Implementation Results

Table 1: Resource usage for individual CEs and the total system.

Module Name	Number of LUTs (PE/SCS)	Number of Flipflops (PE/SCS)	Number of PE BRAMs/ Multipliers	Consumer (LUTs/ Flipflops)	Producer (LUTs/ Flipflops)	Percentage Overhead (LUTs/ Flipflops)
VLD/RLD CE	606/92	699/98	9/0	119/70	217/42	70.6/30.0
IQ CE	429/86	201/13	2/2	126/70	302/106	119.8/94.0
IDCT CE	1091/67	1217/24	3/16	126/70	302/106	45.4/16.4
MMR CE	141/47	152/32	0/0	115/69	217/42	268.8/94.1
MC/PR CE	1705/0	742/0	2/5	115/69	0/0	6.7/9.3
Total System	**7248/292**	**4118/167**	**16/23**	**601/348**	**1038/296**	**26.6/19.7**

Table 2: CE design and integration times reported in hours.

Measured Design Time	VLD/RLD CE	IQ CE	IDCT CE	MMR CE	MC/PR CE	Percentage of Total Time
PE design and initial debugging	480	80	96	19	700	85.6%
PE-Consumer Integration	3.5	4	1	0.25	15	1.5%
PE-Producer Integration	10	4	1	0.25	0	0.9%
Producer's SCS Design	1.5	3	1	0.5	0	0.4%
CE Testing	2	5	3	0.5	5	1.0%
Second Phase PE Verification	9	8	16	1.5	125	9.9%

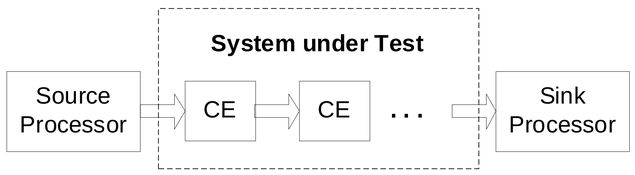
Creating a separate CE for the MMR CE increased system overhead, but reduced the design time penalty.

Table 3: System design and integration times reported in hours.

Total System Integration Design	12
Total System Design Time	1607

System integration time is only 0.4% of total design time.

On-Chip Testbed for Debugging CEs



The standardized CE interface supports the use of a generic testbed that runs orders of magnitude faster than simulation.

Using a processor to supply the test vectors allows new test vectors to be downloaded to the FPGA without resynthesizing the design.

Allowed designers to quickly detect an error in the MC/PR CE, which they fixed by patching a new CE into the pipeline: the Missing Macroblock Replacer (MMR).

Conclusions and Future Work

We demonstrated that while using a programmable controller as an interface increases resource usage, it facilitates integration and debugging.

Implementing the MPEG-1 Video using SIMPPL required 23% more LUTs and 16% more Flipflops.

The designers required only 4% of the overal design time to adapt the IP modules into CEs.

The system-level inegration time was 12 hours (0.4% of the total design time).

The on-chip testbed allows designers to quickly debug one or more CEs with a large number of test vectors and is easily reprogrammable.

Need to create support for debugging CEs at a finer granularity.

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