OneChip: An FPGA Processor With Reconfigurable Logic

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Ralph D. Wittig and Paul Chow

Department of Electrical & Computer Engineering

University of Toronto

Motivation

Computing:

1. FPGAs

- ✔ save logic development cost and time (vs. ASIC)
- ✔ reusable for numerous applications
- ✔ configurable to precise needs of applications
- ✘ slower than custom silicon

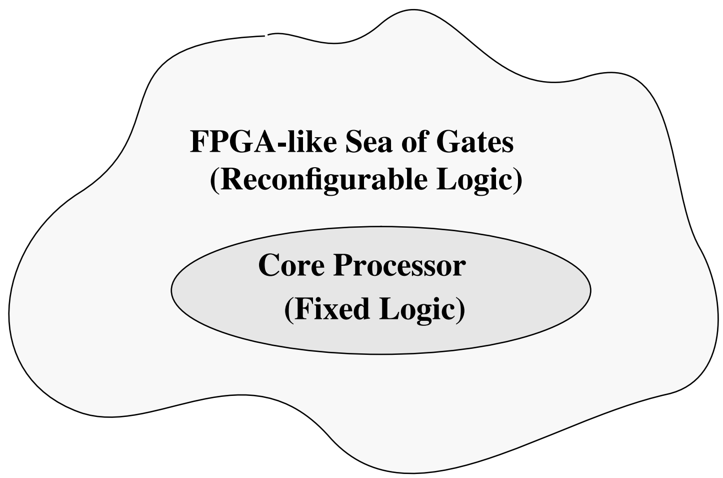
2. CPUs

- ✔ fast execution units
- ✔ designed for general-purpose applications
- ✘ slow execution of unsupported instructions
- ✘ general-purpose instruction set is fixed

Hybrid Solution ?

Custom Compute Machines (CCM)

this work: a CCM called *OneChip*



Proposed OneChip System

Features:

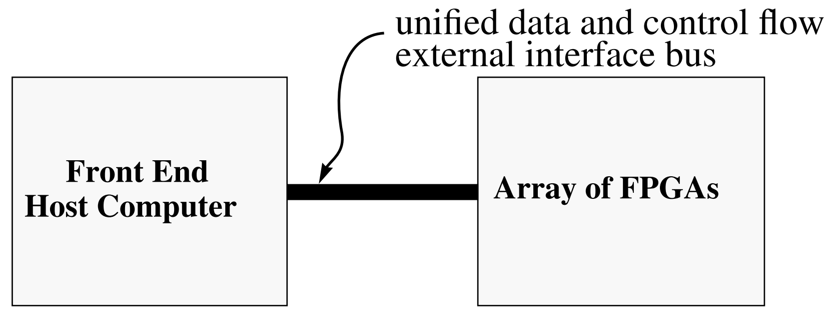
- fixed and reconfigurable logic structures combined
- fixed set of fast, general-purpose instructions
- reconfigurable set of optimized, custom instructions
- MIPS 90/10 rule exploited on a per application basis

Presentation Outline

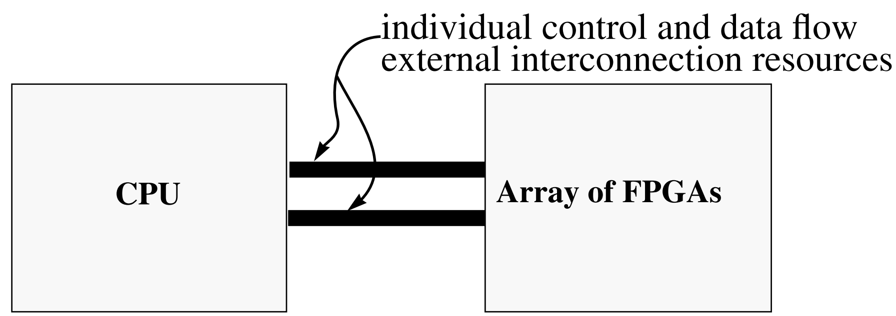
- Existing CCM Systems
- OneChip Architecture
- OneChip Implementation
- Applications
- Conclusions / Future Work

CCM Systems Review

- DEC Perle
- SRC Splash
- NCSU AnyBoard

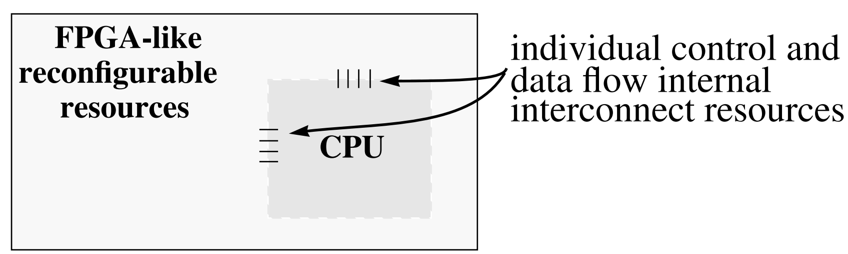


- BU PRISM
- UofT Reconfigurable Coprocessor



- bandwidth limitations on existing CCMs

- Harvard PRISC
- MIT DPGA Coupled Microprocessor



- other systems only theoretically proposed

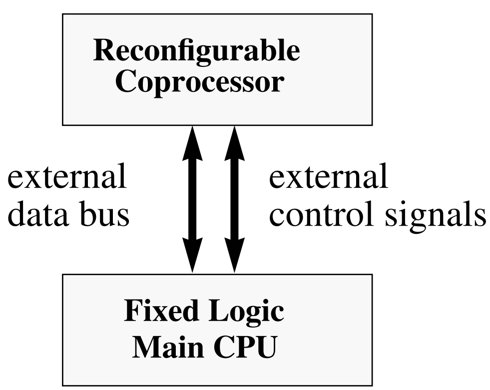
Overcoming B/W Limitations

Existing CCM Systems:

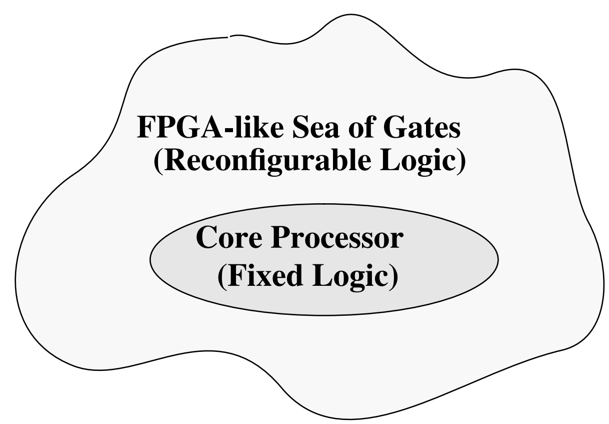
- multi-chip architecture with external buses
- limited control flow
- limited data flow

OneChip System:

- processor core and reconfigurable resources on one die
- tight integration to overcome B/W limitations



Existing CCM Systems



Proposed OneChip System

OneChip Architecture Requirements

- tight integration of the reconfigurable resources
- use of standard processor datapath and functional modules
- employment of standard scheduling and forwarding schemes
- binary code compatibility with existing processor

Integration Approach ?

The Programmable Functional Unit (PFU)

The OneChip system with integrated reconfigurable logic:

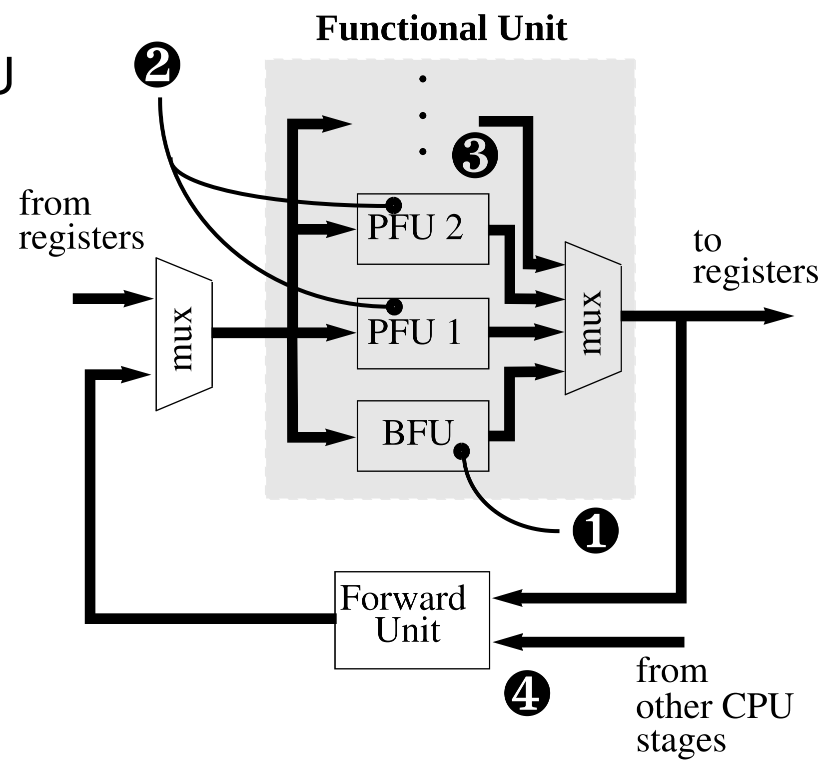
- minimal MIPS-like single issue CPU
- fixed, 32-bit wide datapath
- enhanced functional unit with:

  ❶ one basic functional unit (BFU)

  ❷ one or more programmable functional units (PFU)

  ❸ variable, multiple clock cycle latency on PFU components

  ❹ forwarding module to handle dependency checking



Architectural Prototyping

Means:

Transmogrifier-1 (TM-1):

- four XC4010 (~10k gates each)
- full, programmable crossbar interconnect
- four 32k x 9-bit SRAMs
- link to host computer for programming / debugging purposes

Approach:

- processor core and PFU implemented inside FPGAs
- hardware synthesized from VHDL code constructs

Benefits:

- access to the internals of a CPU
- interfacing strategies can be evaluated rapidly
- implementation of several PFU applications

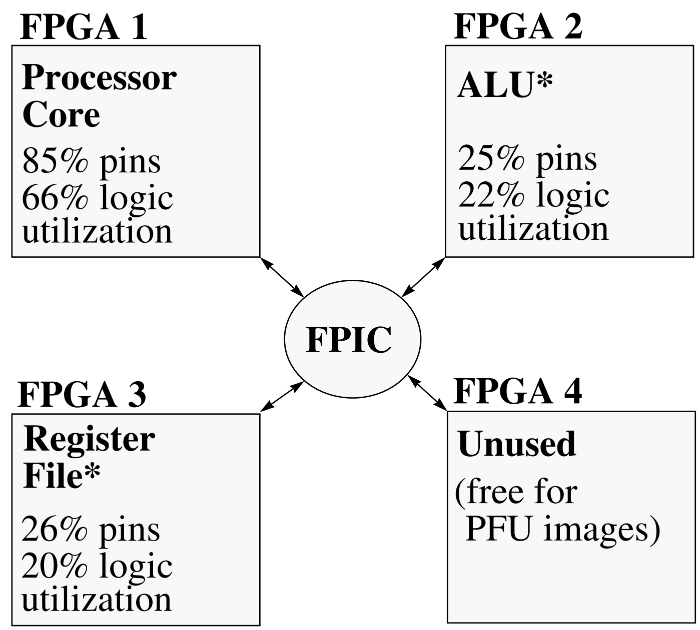
TM-1 Implementation

Implementation Difficulties

- multi-chip partitioning due to logic complexity
- time-division multiplexing of interconnect wires due to pin constraints
- complex memory controller module to access TM-1 SRAMs

Processor Performance

- 10.0 MHz (sub-components)
- 1.25 MHz (CPU pipeline)
- limited by the interconnect delay

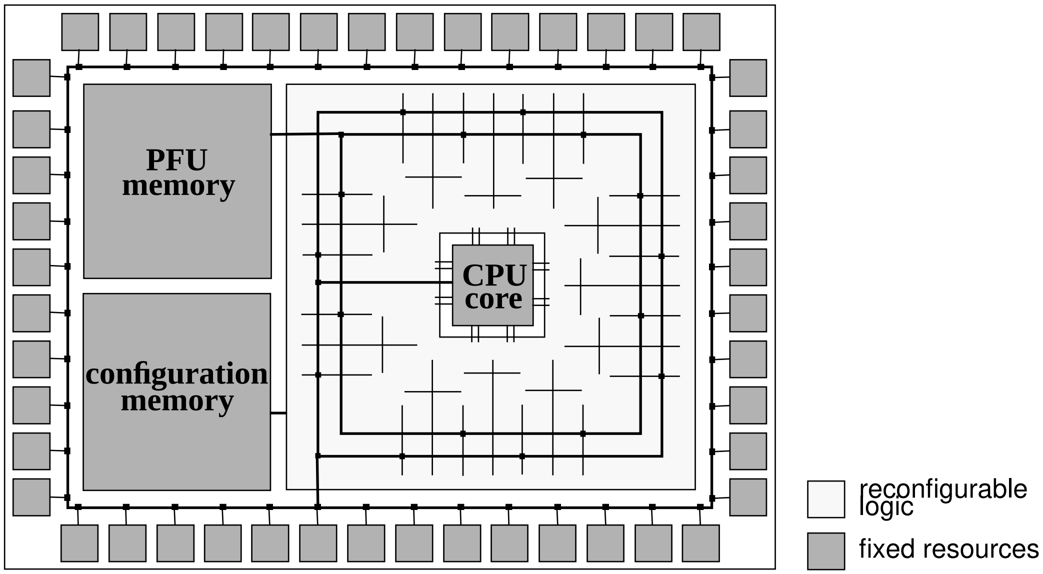


* ALU implements nine instructions
Register File implements six 32-bit registers

Implementation Alternative ?

(Envisioned) Custom Silicon Implementation

- single chip solution
- optimized fixed logic, flexible logic and pin placement
- reconfigurable logic structures like XC4010 plus:
  - application memory array
  - configuration memory array
  - datapath specific features



- processor occupies less than 10% of XC4010 silicon area

Embedded Controller Applications

"OneChip: *the reconfigurable microcontroller*"

Advantages:

- customization of I/O interfaces
- simplification of general-purpose glue logic
- additional pre/post FU processing possible

Disadvantage:

- reconfigurable logic less dense than custom logic

Determine area penalty by analyzing:

- UART
- DRAM controller
- Parallel Port

Area Penalty

Comparison Methodology:

- custom area: VHDL->Synopsys->Cadence->0.8μm process
- FPGA area: 0.8μm XC4010 contains 400 CLBs on 144 mm^2

Area Penalty:

- direct: (up to) 23.7
- reduced (application specific): (as low as) 3.58

Application		Custom Silicon Implementation area (mm^2)	FPGA Implementation # of CLBs	FPGA Implementation area (mm^2)
UART		2.879	124	44.64
DRAM Controller		2.174	141	50.76
Parallel Port 16x1-bit I/O ports	memory addressed, bit-wise programmable	0.804	53	19.08
Parallel Port 8 inputs, 8 outputs	instruction addressed, fixed directionality	0.231	8	2.880
Parallel Port 9 inputs, 19 outputs		0.394	14	5.040

Performance Enhancement Applications

"OneChip: *the reconfigurable processor*"

Speedup Potential:

- operations that do not utilize the full FU bit-width
- code constructs that evaluate with multiple cycle latency
- programs that exceed the local store of the R-file

Application Selection:

- discrete cosine transform (DCT)
- found in every JPEG and MPEG codec
- responsible for 40% of MPEG decode computations

DCT Characteristics

One-Dimensional DCT:

- 17 additions
- 12 subtractions
- 1 multiplication
- 8 eight-bit operands
- implemented as six-stage pipelined PFU module

Two-Dimensional DCT:

- eight 1-D DCT operations
- transpose of intermediate results
- another eight 1-D DCT operations

Speedup Evaluation Methodology

Relative Comparisons:

1) H/W OneChip DCT versus S/W OneChip DCT
2) H/W enhanced R4400 DCT versus S/W basic R4400 DCT

Required System Setups:

System		Memory Access	DCT Computation
1 a)	basic OneChip prototype	TM-1 specific (slow)	TM-1 general-purpose ALU (slow)
1 b)	optimized OneChip prototype	TM-1 specific (slow)	TM-1 DCT optimized PFU (fast)
2 a)	commercial R4400	R4400 specific (fast)	R4400 general-purpose ALU (slow)
2 b)	envisioned commercial OneChip	R4400 specific (fast)	TM-1 DCT optimized PFU (fast)

DCT Configurations

Three Optimization Levels:

a) hardware 1-D DCT evaluation (30 operations => 1 operation)

b) multiple data bytes per memory access

c) extra registers inside DCT PFU for transpose operation

Three DCT Versions:

I : 2-D DCT, optimized with a)

II : 2-D DCT, optimized with a) and b)

III : 2-D DCT, optimized with a), b) and c)

Speedup Results

1) OneChip Prototype:

- 32-bit core processor running at 2.5 MHz
- TM-1 implemented DCT PFU clocked at 2.5 MHz

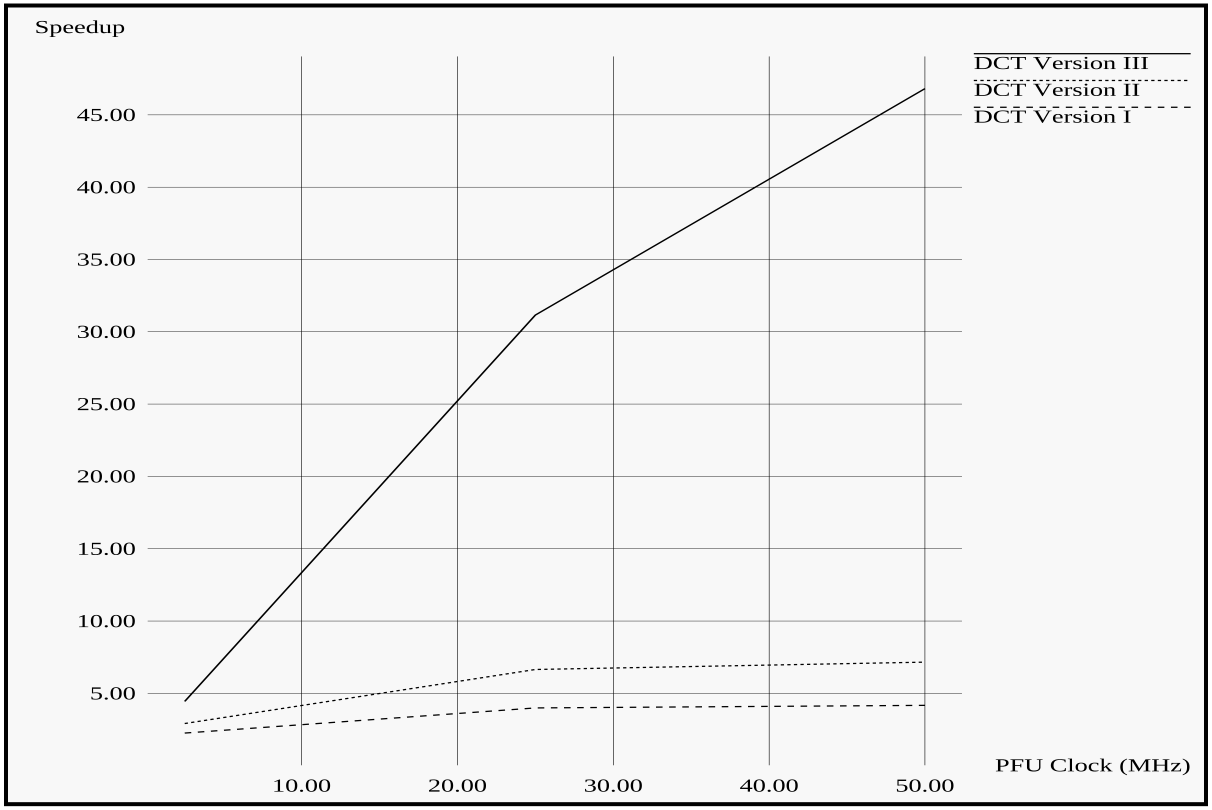
DCT Version I	DCT Version II	DCT Version III
7.06	24.0	40.0

Speedup of H/W OneChip DCT over S/W OneChip DCT

Speedup Results

2) Envisioned Commercial OneChip System:

- 64-bit core processor running at 150 MHz
- TM-1-like DCT PFU clocked at 2.5, 25 and 50 MHz



Speedup of H/W enhanced R4400 DCT over S/W basic R4400 DCT

Conclusions

OneChip Architecture

- tightly merges fixed and reconfigurable logic structures
- employs the Programmable Functional Unit interfacing scheme

OneChip Prototype

- implemented on the Transmogrifier-1
- fully operational
- performance limited by interconnect to 1.25 Mhz

Embedded Controller Applications

- design flexibility for external interface and glue logic
- area penalty over custom implementations of at least 3.5

Performance Enhancement Applications

- speedups of over 40 obtained
- achieved using state-of-the-art processor and FPGA technology

Future Work

- **custom silicon OneChip implementation**
  - overcome TM-1 limitations
  - OneChip specific hardware optimizations
- **prototype extension**
  - additional fixed instructions
  - complete register file
  - cache / multi-level memory system
- **superscalar, time-shared OneChip architecture**
  - resource sharing across several processes and functional units
  - computational state of processes sharing one PFU ?
- **software environment**
  - completely automatic operation
  - dynamic PFU image generation ?
  - run-time reconfiguration ?