Real-Time Seizure Monitoring and Spectral Analysis Microsystem

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***Abstract*— We present a neural recording and spectral analysis integrated microsystem. It is the instrumentational and computational core of an envisioned miniature implantable brain implant for automated epileptic seizure therapy. The microsystem combines two functional blocks: the neural recording interface and the spectral analysis processor. The neural interface contains 256 signal acquisition channels recording neural field potentials from an array of 16x16 electrodes simultaneously, in a distributed fashion. The spectral analysis processor computes a wavelet-based time-frequency map (spectrogram) of the neural recording. We demonstrate the functionality of the integrated microsystem in real-time epileptic seizure monitoring and spectral analysis, as necessary for subsequent automated seizure prediction and prevention.**

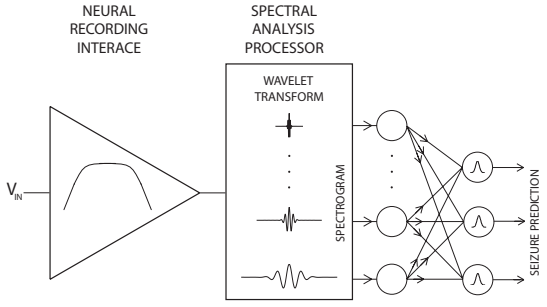

Fig. 1. Architecture of an envisioned brain implant for seizure prediction.

I. Introduction

Approximately 50 million people throughout the world suffer from epilepsy. Almost 25 percent of them have seizures that are not controlled by any available therapy. For the remaining epileptics there are several existing therapies, but most are of limited benefit. None of the present day therapies consider the nonlinear dynamics of dysfunctional brain activity. Computer-based spectral analysis of the dynamics of the brain activity coupled with artificial neural networks and prediction-triggered brain stimulation has been successfully demonstrated in automated prediction and prevention of seizures [1]. On-line implementation of this technology on a miniature implantable platform requires integration of low-power multi-site neural activity recording and real-time spectral analysis functionalities in a single microsystem.

Recording of neural activity has been traditionally performed using bench-top biomedical instrumentation equipment. These instruments are generally stationary, bulky, limited to one or a few acquisition channels, and prone to excessive noise due to wiring. Integrated neural interfaces, fabricated on a single miniature physical substrate, lack these drawbacks. They offer a small, low power, low noise, and cost effective *chronically implantable* alternative to commercial bench-top instruments. Integrated neural interfaces perform signal acquisition, amplification, filtering, and, in some instances, quantization and stimulation [2], [3], [4], [5], [6], [7]. They may also provide wireless data interface on the same chip [8]. To date, brain activity analysis techniques have been mainly implemented off-chip, on a stationary computer. Integrated neural interfaces allow for in-implant intelligent signal processing, extending their functionality beyond signal acquisition and conditioning. An electronic microsystem with both recording and local signal processing capability is an ideal platform for brain-implantable automated medical diagnostics and therapy.

We present a multi-channel neural recording and spectral analysis integrated microsystem. The microsystem is the instrumentational and computational core of an envisioned miniature brain implant for seizure prediction shown in Figure 1. It combines two functional blocks: the neural recording interface and the wavelet spectral analysis processor. The neural recording interface contains 256 signal acquisition channels recording neural field potentials from an array of 16x16 electrodes simultaneously, in a distributed fashion. It also performs spatio-temporal signal pre-processing of neural activity across all channels directly on the sensory plane as discussed in detail in [9]. The spatio-temporal pre-processing allows to identify a dynamic spatial pattern in the action potential field, and may assist in selecting an optimum recording location where the spectral analysis should be performed (e.g., the focus of a seizure, if one is present) [9]. The spectral analysis processor computes a wavelet-based time-frequency map (spectrogram)

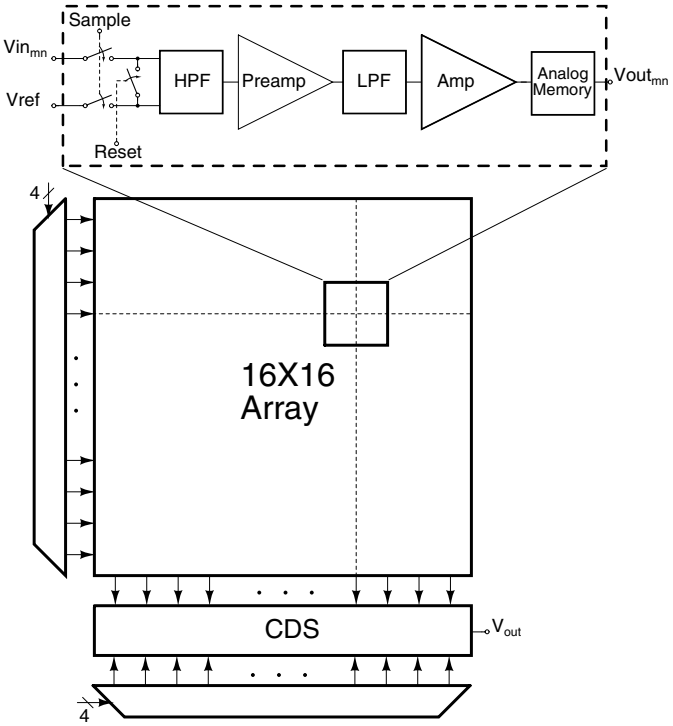

Fig. 2. Architecture of the integrated neural interface and spatio-temporal signal processor.

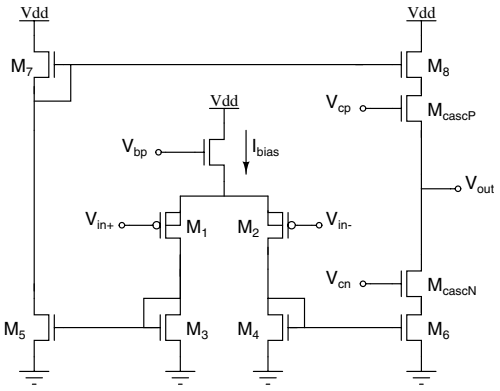

Fig. 3. The low-noise transconductance amplifier.

TABLE I

TRANSCONDUCTANCE AMPLIFIER DESIGN PARAMETERS.

Transistor	W/L (μm)	$I_D(nA)$	$g_m(\mu A/V)$	$g_m/I_D(V^{-1})$
M_1,M_2	400/15	125	3.14	25.17
M_3,M_4	10/400	125	0.83	6.64
M_5,M_6	10/400	125	0.83	6.64
M_7,M_8	10/200	125	0.65	5.2
M_9	45/45	250	3.79	15.16
M_{cascN}	18/8	125	3.1	24.8
M_{cascP}	25/8	125	2.65	21.2

of the neural recording on any selected channel, as necessary for subsequent seizure prediction and prevention. The rest of this paper is organized as follows. Section II presents the architecture and VLSI implementation of the integrated neural recording interface. Section III presents a mixed-signal wavelet processor which performs the computationally intensive task of spectral analysis. Experimental results of real-time seizure recording and spectral analysis are presented in section IV.

II. INTEGRATED NEURAL INTERFACE

A. Architecture

Most of the frequency content of extracellular action potentials in the brain is concentrated between 0.1Hz and 10kHz. Signal amplitudes range from 50 μV to 500 μV, with 100 μV being a typical average value. For low-noise distributed neural potential field recording, a multi-channel integrated neural interface has been designed and prototyped. The neural interface acquires voltages on 256 independent channels simultaneously. The signal acquisition circuits are organized in a 16x16 array as shown in Figure 2.

Each channel in the array shown in Figure 2 contains a high-pass filter (HPF), a low-pass filter (LPF) and two amplification stages. Each channel also contains a sample-and-hold cell with double analog memory. A bank of correlated double sampling (CDS) cells sample the two analog memories, one row at a time, to remove offsets, resulting from device mismatches and to allow for spatio-temporal neural signal processing [9]. Array readout is implemented in a serial fashion as controlled by row and column address decoders. Each channel is connected to on-chip differential recording electrodes through non-passivated top-most metal.

B. VLSI Implementation

A single-stage wide-swing cascoded transconductance amplifier with p-channel MOS input differential pair shown in Figure 3 is employed, both for the preamplifier and the amplifier in each signal acquisition channel. The transconductance amplifier is optimized for low rms noise of 13 μV under the 170 μm pitch cell integration area constraint and 6mW overall power dissipation constraints. The low noise amplifier design procedure employed is detailed in [5]. Design parameters are given in Table I.

Closed-loop signal amplification and high pass filtering are implemented by a frequency selective feedback [5] as shown in Figure 4. The first stage has a fixed gain of 100 and the

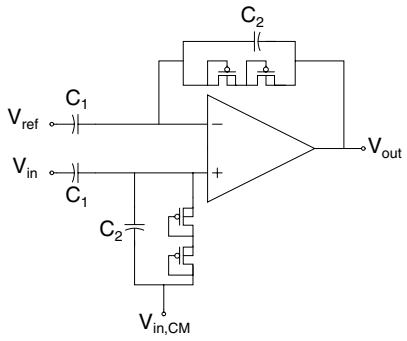

Fig. 4. The closed-loop amplifier and high-pass filter.

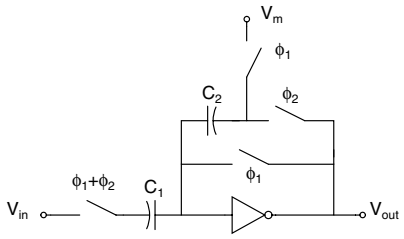

Fig. 5. The schematic of the CDS circuit.

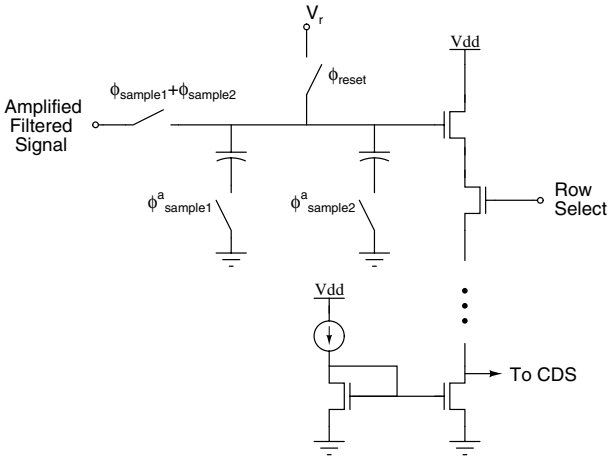

Fig. 6. Sample-and-hold cell with double analog memory for simultaneous sampling.

second stage has a programmable gain of 2, 10, 25 and 50. High pass filtering with a cut-off frequency below 0.1Hz in the first amplification stage prevents DC signals, generated at the electrode-tissue interface, from saturating the amplifiers. The anti-aliasing low-pass filter is implemented by starving the bias current of the second amplifier, with cut-off frequency tunable in the range of 1kHz-10kHz. A column-parallel correlated double sampling (CDS) circuit shown in Figure 5 removes offsets due to mismatches across cells.

Neural activity is sampled simultaneously in all channels by the sample-and-hold cell shown in Figure 6. This eliminates the rolling delay during serial read-out. The local memory cell also reduces substrate coupling by time-multiplexing low-noise signal acquisition and high-noise peripheral switch capacitor signal processing and read-out. The two time-advanced versions of the clock signals in Figure 6 keep the charge injection on the sampling capacitance C_s independent of the stored signal. Charge sharing between the two sampling capacitors is cancelled by resetting the initial voltage to a fixed value.

The 256-channel integrated neural interface and signal processor was fabricated on a $3\text{mm} \times 4.5\text{mm}$ die in a $0.35\ \mu m$ double-poly CMOS technology. The die micrograph is shown in Figure 7. The golden electrodes were post-fabricated on the surface of the die to contact directly with non-passivated aluminum pads. Each electrode is 100 microns high.

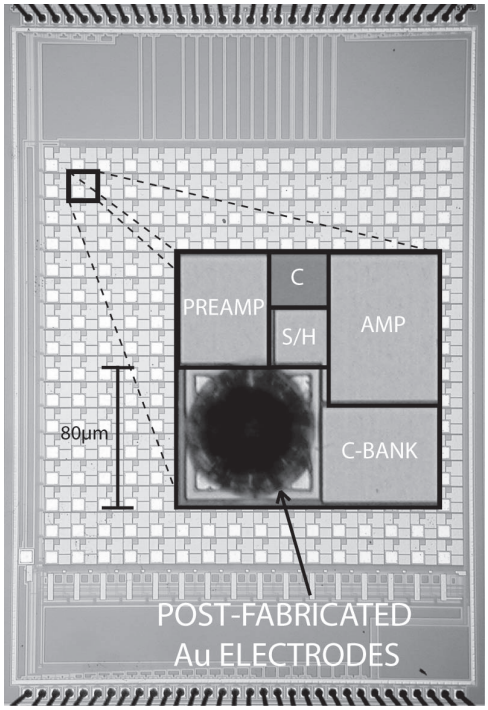

Fig. 7. Micrograph of the 256-channel integrated neural interface. The $3 \times 4.5\ \text{mm}^2$ die was fabricated in a 0.35 μm CMOS technology. Electrode pitch is 170 μm.

III. Wavelet Spectral Analysis Processor

The artificial neural network based seizure prediction algorithm in [1] requires extensive computing resources in order to operate in real time with a high detection rate. This computational throughput is beyond the capabilities of a desktop computer with a Pentium processor, particularly when more than one recording channel is used. The main computational burden, by far, is performing wavelet decomposition of the neural recording signal, which is necessary to train and run the artificial neural network as shown in Figure 1.

The wavelet spectral analysis processor shown in Figure 8 is a densely integrated, massively parallel energy efficient mixed-signal VLSI processor [10], [11]. It delivers over one billion operations per second for every milliwatt of power. Implemented in a 0.5-micron integration technology, the processor yields over one billion operations per second on each square millimeter of silicon area. Such computational efficiency and integration density are several orders of magnitude higher than those available from existing digital processors. This represents an energy-efficient and cost-effective solution for implementations of very computationally intensive learning algorithms, such as epileptic seizure prediction algorithms in real time, particularly on an implantable platform.

Morlet wavelet templates are stored in the on-chip DRAM-based analog array in a row-parallel fashion. A quantized neural recording is shifted into the input shift register. For every shift inner products of a 256-sample window of the input is correlated in analog domain with all wavelet templates

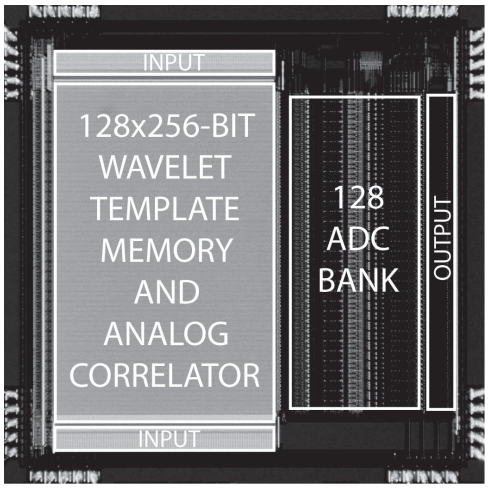

Fig. 8. Micrograph of the wavelet spectral analysis processor. The die measures 3mm x 3mm. A spectrogram of a neural recording is computed in real time using a Morlet wavelet dictionary stored in the on-chip DRAM memory. This is the most computationally intensive step in the seizure prediction algorithm.

stored in the on-chip memory. Correlation is performed in parallel on the entire array. The analog results are quantized by a bank of 128 analog-to-digital converters. The processor dissipates 5.9 mW of power at 6.6 GMACS computational throughput.

IV. Experimental Results

The functionality of the neural recording interface and wavelet spectral analysis processor has been validated in real-time seizure monitoring and spectral analysis experiments. Figure 9 (a) shows a seizure recorded in vitro from a mouse intact hippocampus on one channel of the neural recording interface. Figure 9 (b) depicts the time-frequency map computed by the wavelet spectral analysis processor. The time-frequency map is subsequently fed to an artificial neural network as needed to implement a real-time seizure-predicting brain implant shown in Figure 1.

V. Conclusions

We have presented a neural recording and spectral analysis integrated microsystem, an instrumentational and computational core of an envisioned miniature implantable brain implant for automated epileptic seizure therapy. The microsystem combines two functional blocks: the neural recording interface and the spectral analysis processor. The two blocks have been prototyped and experimentally validated in real-time epileptic seizure monitoring and spectral analysis, as necessary for subsequent automated seizure prediction.

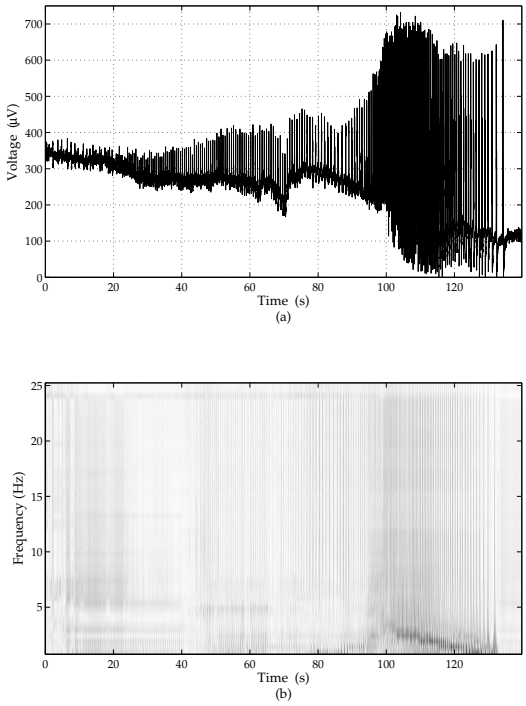

Fig. 9. Seizure monitoring and spectral analysis experimental results: *(a)*, recording of an epileptic seizure in an intact hippocampus of a mouse performed on one channel of the integrated neural interface; *(b)*, a time-frequency map (spectrogram) computed on the wavelet spectral analysis processor.

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