In Vitro Epileptic Seizure Prediction Microsystem

J. Aziz, R. Karakiewicz, R. Genov
Department of Electrical
and Computer Engineering
University of Toronto
Toronto, ON M5S 3G4, Canada
Email: roman@eecg.utoronto.ca

A. W. L. Chiu, B. L. Bardakjian
Institute of Biomaterials
and Biomedical Engineering
Department of Electrical
and Computer Engineering
University of Toronto
Toronto, ON M5S 3G4, Canada
Email: berj@cbl.utoronto.ca

M. Derchansky, P. L. Carlen
Krembil Neuroscience Center,
Toronto Western Hospital,
Departments of Physiology and Medicine,
University of Toronto
Toronto, ON M5T 2S8, Canada
Email: carlen@uhnres.utoronto.ca

***Abstract*— The architecture and VLSI implementation of an epileptic seizure prediction microsystem are presented. The microsystem comprises a neural recording interface and a seizure prediction processor. The two functional blocks have been prototyped in a 0.35 μm CMOS technology and experimentally characterized. The integrated microsystem is validated in predicting the onsets of seizures off line in an in vitro epilepsy model of recurrent spontaneous seizures in the hippocampus of mice.**

I. Introduction

Existing methods of treating epilepsy are of limited benefit or are not effective in all patients [1]. Automated seizure prediction and subsequent prevention is a new promising strategy for epilepsy treatment in patients who do not respond to conventional therapies [2].

The evolution of a seizure involves preictal (*i.e.*, prior to seizure) transitional state that dynamically differs from the interictal (*i.e.*, between seizures) and ictal (*i.e.*, during seizure) states [3]. The implications of this distinction in the states is that there is a possibility for seizure detection or prediction and subsequent preventive intervention. Previous studies reported implantable systems which detect a seizure as it takes place and stimulate to stop it, with only between zero [4] and 17 percent [5] of treated patients rendered seizure-free. The control of dynamic systems to keep them away from the stable manifold once they are firmly established is a laborious and challenging task. Consequently, the ultimate prerequisite for any control algorithm is the ability to predict the onset of undesirable dynamics, not to detect it retrospectively. Hence, the real-time prediction of state transitions becomes the key to successful control strategy. Additionally, multi-site seizure monitoring and stimulation promises to be more effective way to control seizures than few-electrode approaches [4], [5].

We present the design and experimental validation of an envisioned implantable technology that senses, adaptively learns and classifies the abnormal brain activity of seizures before they take place, at multiple sites in the brain. Figure 1 illustrates a block diagram of the autonomous seizure prediction and prevention microsystem. The feedforward signal path predicts a seizure. The feedback path activates a therapeutic intervention upon a positive prediction. The intervention can be in the form of an electrical stimulation [6], or a chemical anticonvulsant injection [7]. In this paper we focus on a miniature implementation of the feedforward path for *in vitro* seizure prediction.

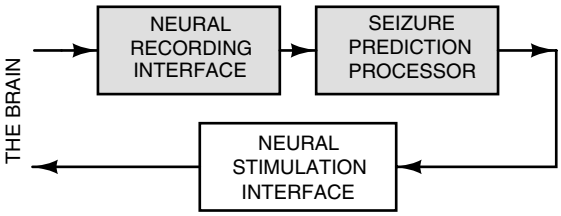

Fig. 1. Seizure prediction and prevention microsystem architecture.

The rest of the paper is organized as follows. Section II presents the VLSI implementation of the neural recording interface with on-chip 3D electrodes. Section III details the functionality of the seizure prediction processor. Section IV contains the experimental results validating each functional block of the seizure prediction microsystem.

II. Neural Recording Interface

A. VLSI Architecture

The neural recording interface acquires voltages on 256 independent channels simultaneously [8]. The signal acquisition circuits are arranged in a 16×16 array as shown in Figure 2.

Each channel is implemented as a two-stage continuous time voltage amplifier as depicted in Figure 3. Electrochemical effects occurring at the electrode-tissue interface cause random DC voltage offsets that are several orders of magnitude larger than the neural signal. Such large amplitude would cause the amplifiers to saturate. Thus, a high-pass filter (HPF) is required to remove the DC offsets without affecting the neural signal. The HPF sub-Hz cut-off frequency is controlled by high-resistance sub-threshold biased MOS transistors [9]. Leakage-induced DC drift is removed by periodic resetting of the amplifier in to the unity gain configuration for a short period of time [10]. A low-pass filter (LPF) is required to filter out any circuit noise outside the band of interest. The LPF is implemented by limiting the bandwidth of the first stage and is controlled by varying the bias current of the transconductance

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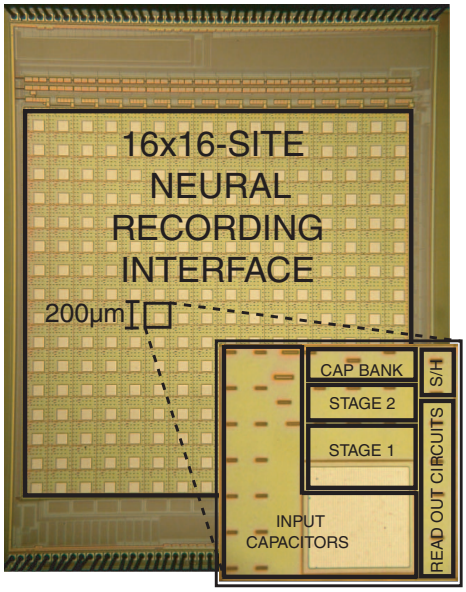

Fig. 2. Micrograph of the neural recording interface. The die fabricated in a 0.35 μm CMOS technology measures 4.5mm $\times$ 3.5mm.

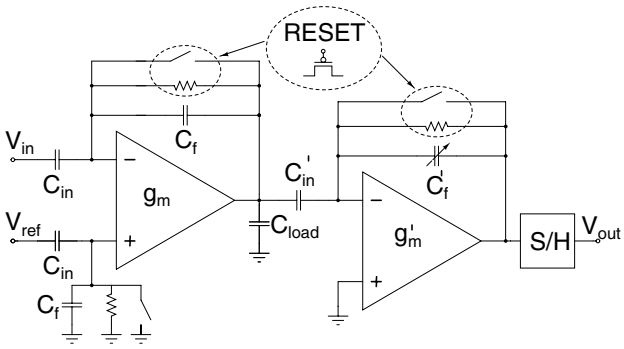

Fig. 3. Recording channel block diagram.

amplifier. The channel gain is programmable and is set by a configurable bank of capacitors in the feedback of the second stage. Each channel in the array contains a sample-and-hold (S/H) circuit as necessary for truly simultaneous multi-channel recording. Array readout is implemented in a serial fashion as controlled by row and column address decoders. One reference electrode is shared by all channels.

B. Low-Power Low-Noise Neural Amplifier

The telescopic operational transconductance amplifier (OTA) shown in Figure 4 is employed in the first stage. Its low output voltage swing is sufficient as two amplification stages are utilized. This yields a factor of five reduction in power dissipation compared to the design in [1] for the same noise. This is due to fewer DC branches and fewer noise sources in the signal path.

Transistor sizing and biasing conditions are crucial for achieving a low-noise performance while dissipating little power. The noise level of $7\mu V$ over 5kHz bandwidth is chosen

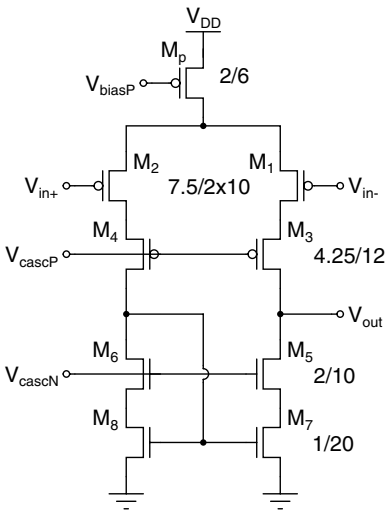

Fig. 4. Telescopic OTA of the first stage.

as an acceptable tradeoff for a channel layout pitch of 200 μm and a bias current of 1.4 μA.

The second stage requires a larger output dynamic range. A wide-swing current mirror OTA topology is employed. As its noise contribution is insignificant compared to that of the first stage, the power dissipation of the second stage can be significantly reduced. The details of this design are given in [1].

C. On-chip Electrode Integration

For *in vitro* experiments on mice hippocampus, a Utah electrode array (UEA) has been bonded to the surface of the neural recording interface die. As the $400\mu m$ UEA electrode pitch is twice the recording channel cell pitch, a set of 8x8 electrodes were bonded for a total of 64 recording sites. A low-cost flip-chip bonding method is adapted. Golden stud bumps are bonded onto the die, coined and covered with conductive epoxy. The electrode array is placed onto the stud bumps. The epoxy is thermally cured. The microsystem is placed into a fluidic chamber as shown in Figure 5. The inlet and outlet tubes allow for the circulation of artificial cerebrospinal fluid (ACSF) during recording from live tissue placed into the chamber as necessary to preserve its vitality.

The experimental characteristics of the neural recording interface are reported in Table II-C.

III. Seizure Prediction Processor

The wavelet artificial neural network (WANN) seizure prediction algorithm described in [2] requires extensive computing resources in order to operate in real time with a high detection rate. The main computational burden, by far, is performing wavelet decomposition of the neural recording signal, which is necessary to train and run the artificial neural network (ANN). This computational throughput is beyond the capabilities of a desktop computer with a Pentium processor, particularly when more than one recording channels are used.

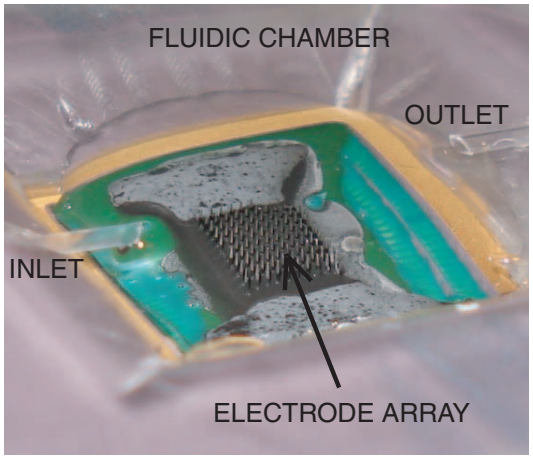

Fig. 5. Neural recording integrated interface in a fluidic chamber.

TABLE I
NEURAL RECORDING INTERFACE EXPERIMENTAL CHARACTERISTICS

Programmable Gain	48dB - 68dB
Total Input Referred Noise	$7\mu V_{rms}$
THD@4.4mV_{pp} (worst case)	0.7%
LPF Cut-off Frequency	500Hz - 5kHz
HPF Cut-off Frequency	0.01Hz - 70Hz
Max Sampling Rate	10ksps
Power Dissipation per channel	$15\mu W$/channel
Total Power Dissipation	5.04mW
Electrode	Pt tips, 1500μm long

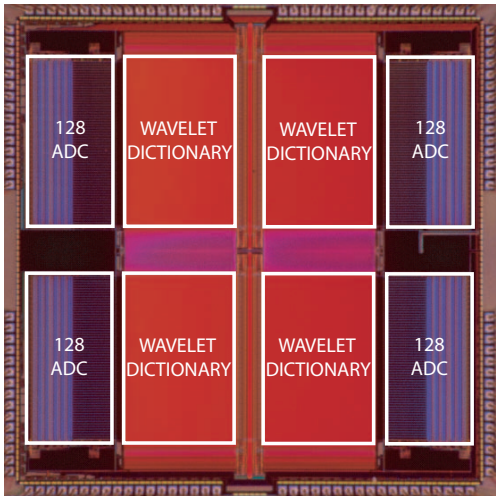

Fig. 6. Micrograph of the wavelet spectral analysis processor. The die fabricated in a 0.35 μm CMOS technology measures 4mm $\times$ 4mm.

TABLE II
ON-CHIP WAVELET TRANSFORM PARAMETERS

Computing frequency	50Hz
Wavelet coefficient resolution	4-bits
Memory dimensions	128 rows $\times$ 1024 columns
Wavelet frequency bins	32 bins
Maximum wavelet frequency	90.8Hz

The wavelet spectral analysis processor shown in Figure 6 is a densely integrated massively parallel energy efficient mixed-signal VLSI processor [11], [12]. It delivers over 175 billion binary operations per second for every milliwatt of power. Implemented in a 0.35 μm CMOS integration technology, the processor yields 1.8 billion operations per second [13]. Such computational efficiency and integration density are several orders of magnitude higher than those available from existing digital processors. This represents an energy-efficient and cost-effective solution for implementations of very computationally intensive learning algorithms, such as epileptic seizure prediction algorithms in real time, particularly on an implantable platform.

Morlet wavelet templates are stored in the on-chip DRAM-based analog array in a row-parallel fashion. Input data is presented serially into the input shift register. For every shift a 1024-sample window of the input is correlated with all wavelet templates stored in the on-chip memory in analog domain. Correlation is performed in parallel on the entire array. The computed inner products are quantized by four banks of 128 analog-to-digital converters each.

The memory dimensions of the wavelet processor dictate the wavelet transform parameters. The number of rows sets the number of wavelets that are stored simultaneously for a given wavelet coefficients resolution. The length of each row and the sampling rate determine the wavelet frequency range. Table III summarizes the characteristics of the wavelet transform for the array size of 128$\times$1024 bits. A larger-scale integrated implementation can relax these limits and may further improve the seizure prediction rate.

The output of the processor represents the time-frequency map of the acquired signal [1]. A ANN is then trained on the time-frequency maps. The tasks of ANN training and classification are of low computational complexity and are performed in software.

IV. EXPERIMENTAL VALIDATION

In order to validate the functionality of the seizure prediction microsystem, the two functional blocks, the neural recording interface, and the seizure prediction processor, both depicted in Figure 1, were experimentally characterized off line.

To validate the neural recording interface functionality, an intact hippocampus of a mouse was inserted onto the electrode array for in vitro recording. Low Mg^{+2} was injected in the ACSF stream to induce seizure like events, which were then recorded through the on-chip UEA, quantized by off-chip ADCs and transferred to a PC for visualization through a custom developed user interface. Figure 7 shows an example of a waveform recorded on the chip through one of the array electrodes.

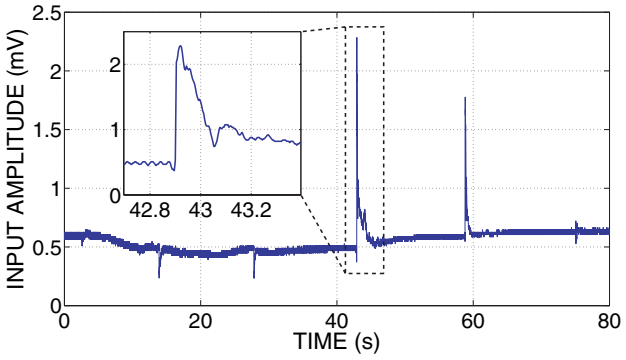

Fig. 7. An experimental recording from an intact hippocampus of a mouse through an on-chip UEA electrode. Seizure-like events were induced chemically by low Mg^{2+}.

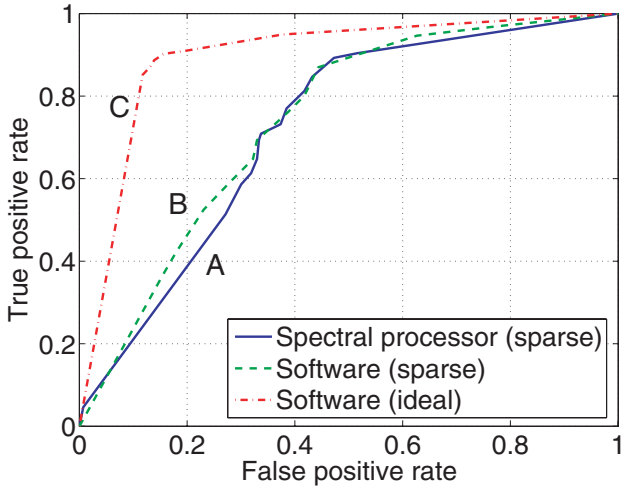

Fig. 8. A comparison of the ROC curves for the classified data obtained from the wavelet processor and a Matlab model.

To demonstrate the seizure prediction efficacy, a set of time-frequency maps of a pre-recorded seizure data set was computed on the wavelet analysis processor. Each map was then selectively sampled and fed to a software-based ANN in order to classify brain activity states in real time. A comparative experiment was performed on the seizure prediction processor and its software model in Matlab. The Morlet wavelet transform of biological recordings was computed on both systems and the outputs were treated as inputs to a software version of the ANN off line. The corresponding Receiver Operating Characteristic (ROC) curves are shown in Figure 8. Curves A and B correspond to the wavelet analysis chip and its software emulation respectively, both in the case when recorded data is sparsely subsampled as limited by the slow PC interface in the testing setup. In this case, a sliding window with 128ms time shift is employed. Curve C corresponds to the ideal case implemented in software when no I/O data rate limitations are present. The sliding window time shift in this case is 1ms. These results fully validate the utility of the wavelet analysis chip as without PC I/O bandwidth limitation the prediction performance is expected to match well that described by curve C.

V. Conclusion

We have presented an architecture and VLSI implementation of an automated epileptic seizure prediction microsystem. The microsystem is composed of a recording neural interface for acquiring neural activity and a wavelet transform processor for real-time spectral analysis. Both components have been prototyped and their functionality experimentally validated. A ANN was trained on the wavelet transformed brain activity data in software to predict seizures in a timely manner. A comparative experiment demonstrates the effectiveness of the microsystem in predicting epileptic seizures.

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References

[1] J. N. Y. Aziz, R. Karakiewicz, R. Genov, B. L. Bardakjian, M. Derchansky, and P. L. Carlen, "Real-time seizure monitoring and spectral analysis microsystem," in *IEEE International Symposium on Circuits and Systems*. IEEE, 21–24 May 2006, pp. 2133–2136.

[2] A. Chiu, S. Daniel, H. Khosravani, P. Carlen, and B. Bardakjian, "Prediction of seizure onset in an in vitro hippocampal slice model of epilepsy using gaussian-based and wavelet-based artificial neural networks," *Ann Biomed Eng*, vol. 33, no. 6, pp. 798–810, June 2005.

[3] L. Iasemidis and J. Sackellares, "Chaos theory and epilepsy," pp. 118–126, 1996.

[4] K. N. Fountas, J. R. Smith, A. M. Murro, Y. D. Park, P. D. Jenkins, and D. Greene, "Closed-loop stimulation implantable system for the management of focal, medically refractory epilepsy: Implantation technique and preliminary results," in *Annual Meeting of the American Epilepsy Society*, 2005.

[5] J. M. Plitsky, R. Estellar, A. M. Murro, J. Smith, P. Ray, Y. D. Park, and M. J. Morrell, "Effects of electrical stimulation paradigm on seizure frequency in medically intractable partial seizure patients with a cranially implanted responsive cortical neurostimulator," in *Annual Meeting of the American Epilepsy Society*, 2005.

[6] H. Khosravani, P. L. Carlen, and J. L. P. Velazquez, "The control of seizure-like activity in the rat hippocampal slice," *Biophysical Journal*, vol. 84, no. 1, pp. 687–695, January 2003.

[7] S. S. Jahromi, K. Wentlandt, S. Piran, and P. L. Carlen, "Anticonvulsant actions of gap junctional blockers in an in vitro seizure model," *Journal of Neurophysiology*, vol. 88, no. 4, pp. 1893–1902, October 2002.

[8] J. Aziz, R. Genov, M. Derchansky, B. Bardakjian, and P. Carlen, "256-channel neural recording microsystem with on-chip 3D electrodes," in *IEEE International Conference Solid-State Circuits Digest of Technical Papers*, 2007.

[9] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording app l ications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, June 2003.

[10] F. Heer, S. Hafizovic, W. Franks, A. Blau, C. Ziegler, and A. Hierlemann, "CMOS microelectrode array for bidirectional interaction with neuronal networks," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1620–1629, July 2006.

[11] R. Genov and G. Cauwenberghs, "Kerneltron: Support vector 'machine' in silicon," *IEEE Trans. Neural Networks*, vol. 14, no. 5, pp. 1424–1434, 2002.

[12] ——, "Charge-mode parallel architecture for matrix-vector multiplication," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 10, pp. 930–936, 2001.

[13] R. Karakiewicz, R. Genov, A. Abbas, and G. Cauwenberghs, "175 GMACS/mW charge-mode adiabatic mixed-signal array processor," in *Proc. IEEE Symposium on VLSI Circuits*, June 2006.