A Zero-IF 60GHz Transceiver in 65nm CMOS with > 3.5Gb/s Links

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Abstract—**This paper presents a 1.2V 60GHz zero-IF transceiver fabricated in a 65nm CMOS process with a digital back-end. The chip includes a receiver with 14.7dB gain, a low 5.6dB noise figure, a 60GHz LO distribution tree, a 64GHz static frequency divider, and a direct BPSK modulator operating over the 55-65GHz band at data rates exceeding 3.5Gb/s. The chip consumes 374mW (232mW) from 1.2V (1.0V) and occupies 1.28x0.81mm^2. The transceiver was characterized over temperature up to 85°C and for power supplies down to 1V. A manufacturability study of 60GHz radio circuits is presented with measurements of transistors, the low-noise amplifier, and the receiver on typical and fast process splits. The transceiver performance is demonstrated using a 3.5Gb/s 2-meter wireline/wireless transmit-receive link over the 55-64 GHz range.**

I. INTRODUCTION

Some of the first mass-consumer products operating in the mm-wave spectrum are likely to be targeted at the emerging 60GHz-radio market. These products take advantage of the 7GHz of unlicensed spectrum available from 57 to 64GHz to provide data-rates that far exceed those of alternative standards such as 802.11n or Ultra Wide-Band. Multi-Gb/s wireless point-to-point transmission is possible over short-ranges using basic modulation techniques.

Unlike earlier 60GHz radio chip-sets reported in SiGe BiCMOS [1] or CMOS [2]–[9], this paper presents the first fundamental frequency, zero-IF 60GHz wireless transceiver. It employs the simplest architecture, as needed in rapid file-transfer applications, utilizing direct BPSK modulation at 60GHz, a fundamental frequency static divider, and which does not require image rejection or ADCs in the receiver. The transmitter data input accepts baseband NRZ data at rates beyond 4Gb/s. Measurement results over temperature, power supply, and process corners are presented.

II. TRANSCEIVER ARCHITECTURE

A block diagram of the direct modulation, zero-IF radio transceiver is presented in Fig 1. With the exception of a fundamental frequency voltage-controlled oscillator, this chip integrates all of the critical 60-GHz blocks, including an LNA, mixer, direct modulation BPSK transmitter, fundamental frequency static divider, and 60-GHz LO tree. Since, due to time constraints, no IF amplifier was included, all the receive-path gain is at 60 GHz. Baseband NRZ data is provided from off-chip to the transmitter and is recovered at the IF output of the receiver, without any digital signal processing or analog-to-digital conversion.

III. CIRCUIT BUILDING BLOCKS

All circuits are differential, except the LNA, and were designed using the constant current density biasing technique described in [10] which renders them immune to V_T and bias current variation. Furthermore, by employing transformer-coupling and AC-folded
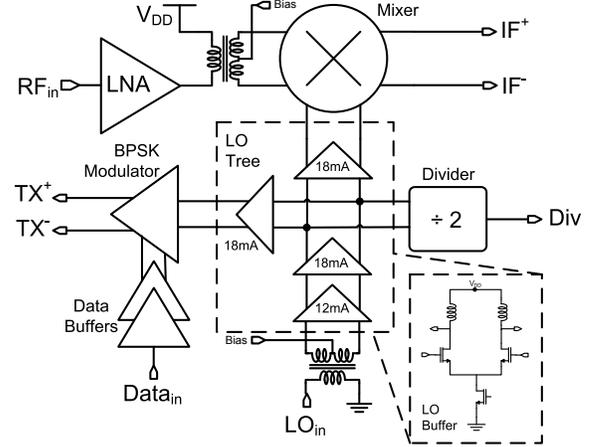

Fig. 1. 60GHz direct modulation BPSK transceiver architecture.

cascode topologies in all blocks, no more than a single high-speed transistor is ever stacked above a current source. This guarantees operation from 1.2 or 1.0V supplies, with the largest possible V_{DS}, which maximizes the power gain and minimizes the noise figure of the transistor. Unlike in a conventional cascode, in an AC-folded cascode, the V_{DS} of the common-source transistor is insensitive to V_T variations of the common-gate transistor. All of these techniques combine to allow the circuits presented here to be operable in LP, GP, or HS flavors of a 65nm CMOS manufacturing process. The penalty for using AC-folded cascodes is a doubling of current consumption compared to the traditional cascode, which is only partially compensated by the reduction in power supply voltage.

A. Low-Noise Amplifier

The single-ended LNA schematic is shown in Fig 2. It consists of three cascaded CS-CG stages, with the transistor sizes increasing from stage to stage. The input stage is noise and impedance
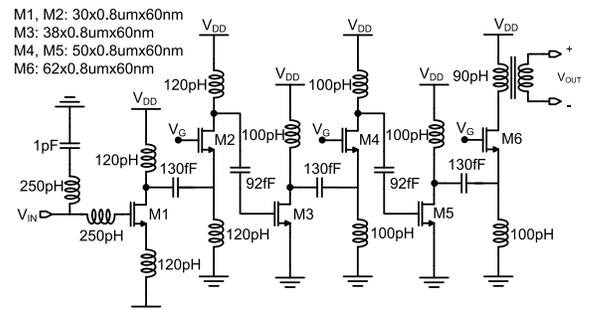

Fig. 2. 1.2V, 3-stage cascaded CS-CG, 60GHz low-noise amplifier schematic.
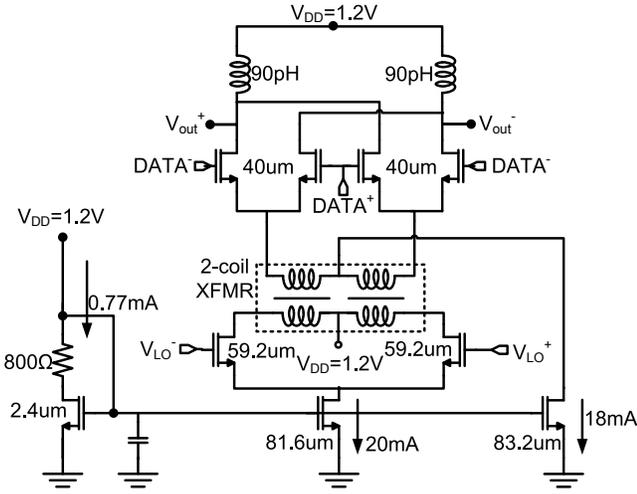
Fig. 3. BPSK modulator schematic.

Fig. 4. Static frequency divider schematic (top), and layout details of the static frequency divider (bottom).

matched to 50Ω and is biased at the receiver minimum noise figure current density of $0.3\text{mA}/\mu\text{m}$ at $V_{DS}=1.2\text{V}$. All transistors feature $0.8\mu\text{m}$ finger width with double-sided gate contacts. The last stage of the LNA is terminated in a transformer which acts as single-ended to differential converter between the LNA and the double-balanced mixer. The LNA, which can also act as a low-noise power amplifier, consumes 80mA (60mA) from a 1.2V (1.0V) power supply and has a measured saturated output power of 7.5dBm (4.6dBm).

B. BPSK Modulator and Mixer

Fig 3 illustrates the BPSK modulator. The LO differential pair at the bottom and the data quad at the top are coupled through a transformer that allows the maximization of the V_{DS} across each transistor as well as the independent biasing of the two sides of the circuit. The data-path is formed from a cascade of three current-scaled CML buffers with a 7GHz bandwidth.

The mixer topology is identical to that of the BPSK modulator and is scalable to 140 GHz [11]. The mixer output is matched to 50Ω and drives the signal directly off chip.

C. Static Frequency Divider

The schematic of the 60GHz static frequency divider is shown in Fig 4 (top). It employs a new topology that features a single differential pair at the clock input which drives the two latches through two transformers. Eliminating one of the two clock differential pairs results in reduced area and power consumption. The transformers were realized with two vertically stacked coils with inputs and outputs aligned along a diagonal line of symmetry. Fig 4 (bottom) illustrates the layout detail including the first of three CML buffers at the divider output.

D. Tuned Clock Tree

The 53-65GHz off-chip LO signal is distributed to the critical circuit blocks using a tuned LO distribution tree designed to have 25% bandwidth. The latter consists of cascaded differential buffers with inductive loads and a fanout of three, as shown in Fig 1, with both 12mA and 18mA buffers employed.

E. Tuned mm-Wave Switch

While not included in the aforementioned transceiver, a stand-alone 50-70GHz series-shunt switch as in Fig 5a was manufactured on the same dies and characterized separately. S-parameter

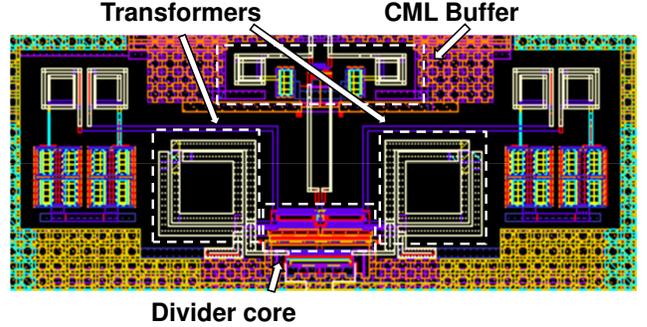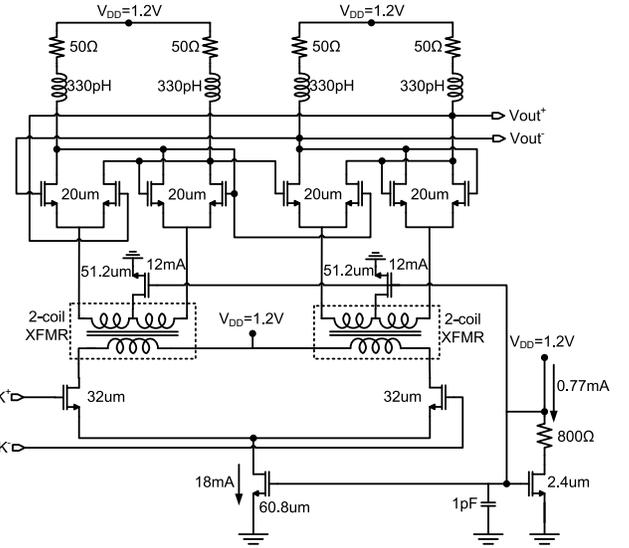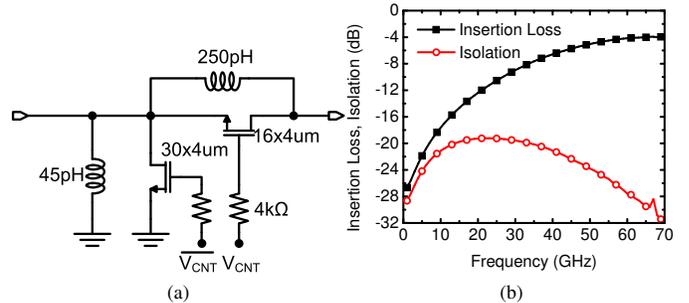Fig. 5. Schematic (a) and measured insertion loss and isolation (b) of series-shunt switch.

measurements on the stand-alone mm-wave switch in Fig 5b show a nominal insertion loss of 3.9dB and an isolation of 28dB at 60GHz.

IV. IMPLEMENTATION AND MEASUREMENTS

The transceiver was fabricated in a 65nm CMOS process with a 7-metal digital back-end and MIM capacitors. For a 80x60nmx1μm NFET device with double-sided gate contacts, peak f_{MAX} and f_T values of 320GHz and 220GHz were measured at current densities of approximately 0.3 and 0.4 mA/μm respectively.

A micro-photograph of the transceiver is shown in Fig 6. It occupies 1.28x0.81mm^2. The LO and RF signals are distributed along μ-strip lines formed in metal 7 over a shunted metal 1

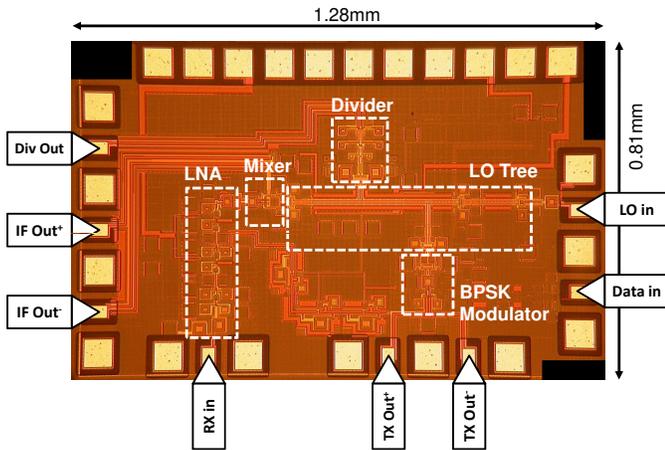Fig. 6. Die photograph of the transceiver. The total die area is 1.28x0.81mm^2.
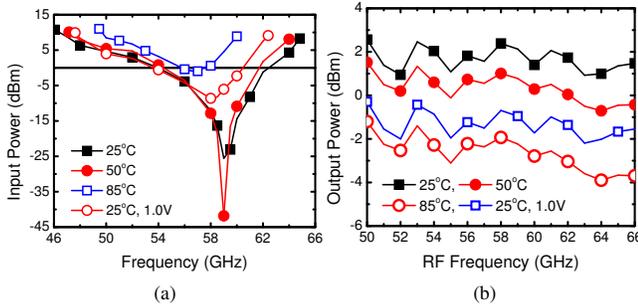

Fig. 7. Measured (a) divider and LO-tree sensitivity, and (b) transmitter output power all over temperature.

and metal 2 ground plane. A side-wall consisting of all metals shunted together forms a Faraday cage-like structure around each transmission line and between circuit blocks, improving isolation.

The static frequency divider sensitivity was measured in the transceiver, including the LO distribution network. The self-oscillation frequency is 59.2GHz at room-temperature with a 1.2V supply. As illustrated in Fig 7a, the divider operates over a frequency range of 46-65GHz at 1.2V, and 47-62GHz at 1.0V.

Measured total integrated power at the output of the transmitter is plotted in Fig 7b versus frequency. Measurements are shown over temperature up to 85^oC, with peak output power above +2.4dBm at 25^oC and 58GHz.

The manufacturability of the 60GHz transceiver was studied by measuring transistors, the low-noise amplifier, and the stand-alone
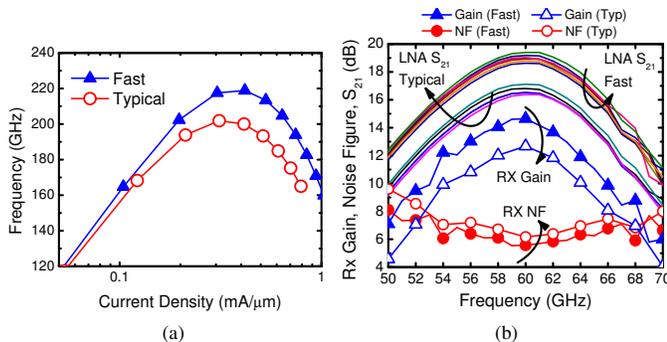

Fig. 8. Measured (a) f_T, and (b) RX gain, noise figure, and LNA S_{21} over fast and typical process corners.
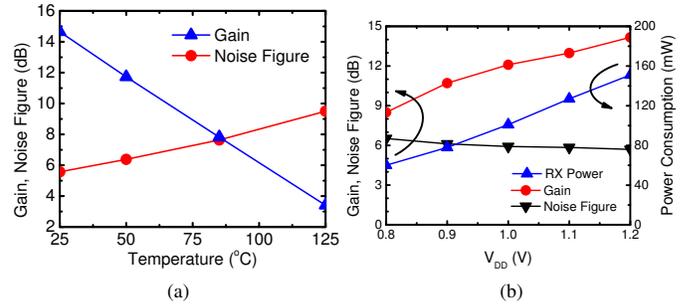

Fig. 9. Measured receiver gain and noise figure over (a) operating temperature, and (b) power supply.
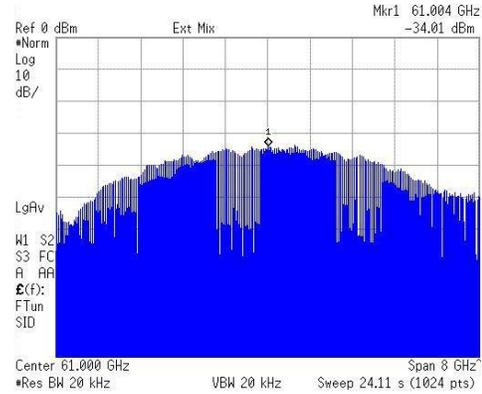

Fig. 10. 3.5Gb/s PRBS transmitter spectrum at 61GHz LO.

receiver over fast and typical process corner lots. Compared to the standalone RX breakout measurements, the receiver gain in the transceiver was degraded by 3dB because of insufficient LO power at the mixer LO port. The LO-tree fanout in the transceiver is 3, whereas it is only 1 in the RX breakout. Performance results for both versions are summarized in Table 1 at the end of this paper.

Results in Fig 8a indicate a 10% drop in peak f_T from the fast to typical corner splits. It should be noted that although there is significant V_T variation across corners, the measured peak f_T current density is essentially constant. LNA s-parameter measurements are plotted in Fig 8b, along with receiver gain and noise figure, all for the typical and fast corners. The LNA displays a peak gain of 19.2dB at 60GHz and a 3dB bandwidth extending from 54GHz to 66GHz. A peak receiver conversion gain of 14.7dB and a 50Ω noise figure of 5.6dB are noted, both occuring at 60GHz. The DSB noise figure remains below 6dB over an RF bandwidth of 58 to 63GHz. The receiver measurements indicate that the impact of process variation on the receiver can be attributed solely to transistor g_m and f_T degradation due to an increase in gate length. Note that the peak gain frequency of the LNA and of the receiver and the minimum noise figure frequency do not shift with process variation.

Measurements of the receiver over temperature in Fig 9a show an approximate 7dB gain degradation and 2dB noise increase at 85^oC. Fig 9b illustrates that the gain and noise figure do not seriously degrade as V_{DD} is reduced to 1.0V, with a gain drop of 2.5dB, and a noise figure increase of only 0.3dB. The gain degradation over temperature and supply can be easily compensated with a VGA at IF. The measured input return loss of the receiver is less than -10dB, and the input compression point is -22dBm.

Finally, a transmit-receive link was demonstrated in the 55-64GHz range by employing one transceiver chip in transmit-mode

TABLE I

PERFORMANCE COMPARISON FOR 60GHz TRANSCEIVER/RECEIVER CHIP-SETS. BRACKETS SHOW MEASURED RESULTS FROM 1.0V.

| Ref.	Gain (dB)	NF (dB)	IP_{1dB} (dBm)	S_{11} (dB)	TX Power (dBm)	Modulation, Data Rate	V_{DD} (V)	P_{DC} (mW)	Chip(s) Area (mm^2)	Process and Integration
[1]	72	5.5-6.5	-36	-15	17.0	MSK 2.0Gb/s	2.7, 4.0	996	12.2	0.13 SiGe, TX, RX, 20GHz PLL, IQ mod/demod
[2]	16-21	5.5-7	-21	-10	n/a	n/a	1.2-1.5	60	0.3	90nm, LNA, mixer, IF buffer, off-chip LO
[5]	51	9	-30	-15	8.4	16-QAM 15Gb/s	1.8	362	6.5	90nm, TX, RX, PLL, IQ mod/demod
[6]	55.5	6.2	-26	-10	n/a	n/a	1.0	24	1.6	90nm, LNA, mixer, VGA, buffer, off-chip LO
[7]	18.3-22	5.7-8.8	-27.5	-	n/a	n/a	1.2	36	0.2	90nm, LNA, 30GHz LO, RF mixer, IF mixer
[8]	19.7	11.7	-17	-	6.0	QPSK 2.6Gb/s	0.7, 1.0	339	4.5	90nm, TX, RX, IQ mod/demod, off-chip LO
This work (RX)	14.7 (12.1)	5.6 (5.7)	-22	-10	n/a	n/a	1.2 (1.0)	151 (101)	0.5	65nm, single-chip RX, off-chip LO
This work (TXRX)	11.3 (8.9)	5.6 (5.8)	-22	-10	2.4 (-0.7)	BPSK 3.5Gb/s+	1.2 (1.0)	374 (232)	1.0	65nm, single-chip TXRX, LO tree, divider, off-chip LO
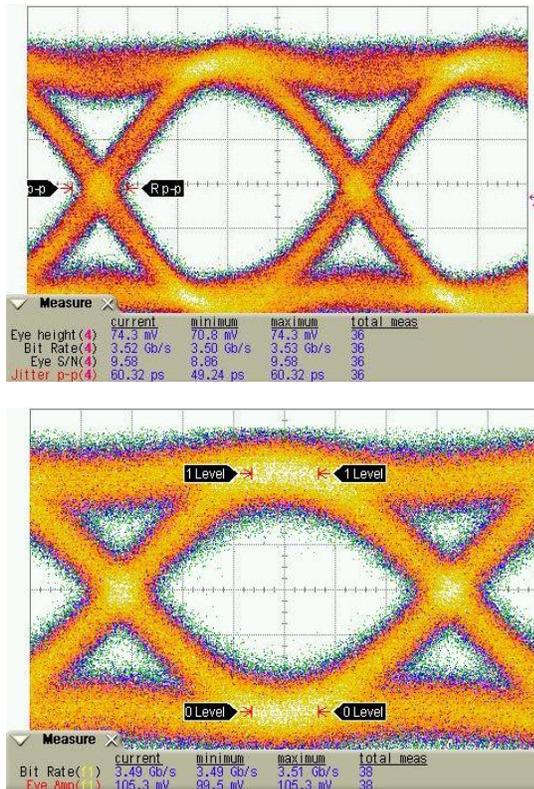
Fig. 11.   3.5Gb/s PRBS eye diagram at the output of the receiver for wireline (top) and wireless (bottom) setups.

on a probe station, and another transceiver chip in receive-mode on a second probe station, approximately 2 meters away. Both wired and wireless demonstrations were conducted, with high-speed signal probes and 67GHz cables connecting to either horn antennas with 25dBi gain, or 2 meters of cable. Both channels are estimated to have approximately 35-40dB of loss at 60GHz. An external amplifier with 30dB gain and 4GHz bandwidth was connected between the IF output of the receiver and a sampling oscilloscope. The transmitter output spectrum is shown in Fig 10 for a 3.5Gb/s 2^7 - 1 PRBS data signal. In Fig 11, the wired (top) and wireless (bottom) received eye diagrams at the receiver IF output are shown. The bandwidth of the external IF amplifier

limited the data rate experiments to 5Gb/s. These transceiver link experiments demonstrate for the first time that a simple zero-IF radio architecture, without ADCs and IQ mixer, can be realized in CMOS at 60 GHz.

V. CONCLUSION

A 1.2V 60GHz zero-IF transceiver has been implemented in a 65nm CMOS technology occupying only 1.28x0.81mm^2. Employing direct BPSK modulation, a 60GHz LO distribution tree, a fundamental frequency static divider, and zero-IF down-conversion, this transceiver represents the simplest architecture appropriate for high-frequency, high-bandwidth data-transfer applications. A 2-meter wireline/wireless transmit-receive demonstration between two probe stations acts as a proof-of-concept, achieving data-transfer rates in excess of 3.5Gb/s over the 55-64GHz range.

ACKNOWLEDGMENTS

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