

65-nm CMOS, W-band Receivers for Imaging Applications

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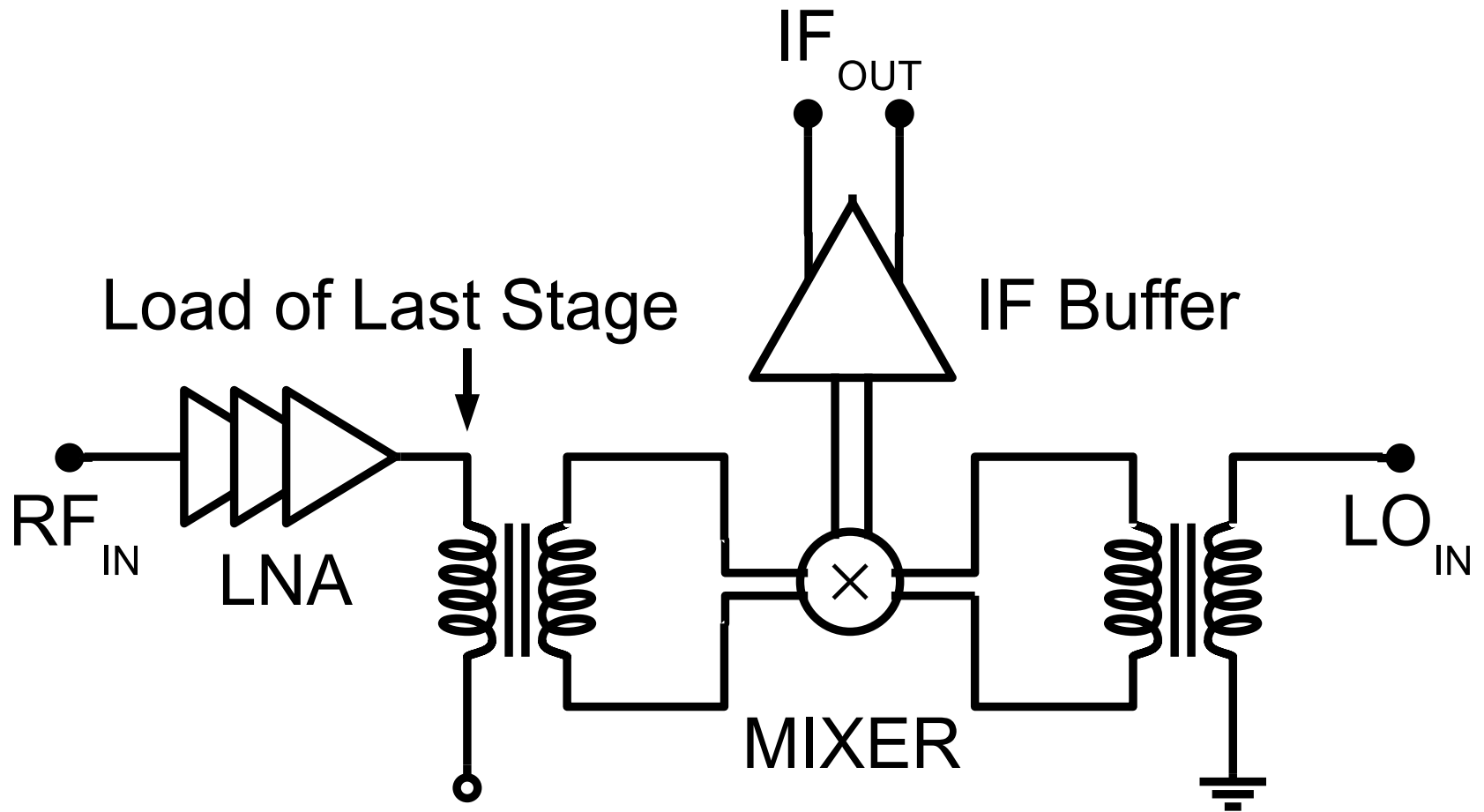
Table of Content

- Motivation
- Circuit Schematics
- Fabrication
- Measurement Results
- Conclusion

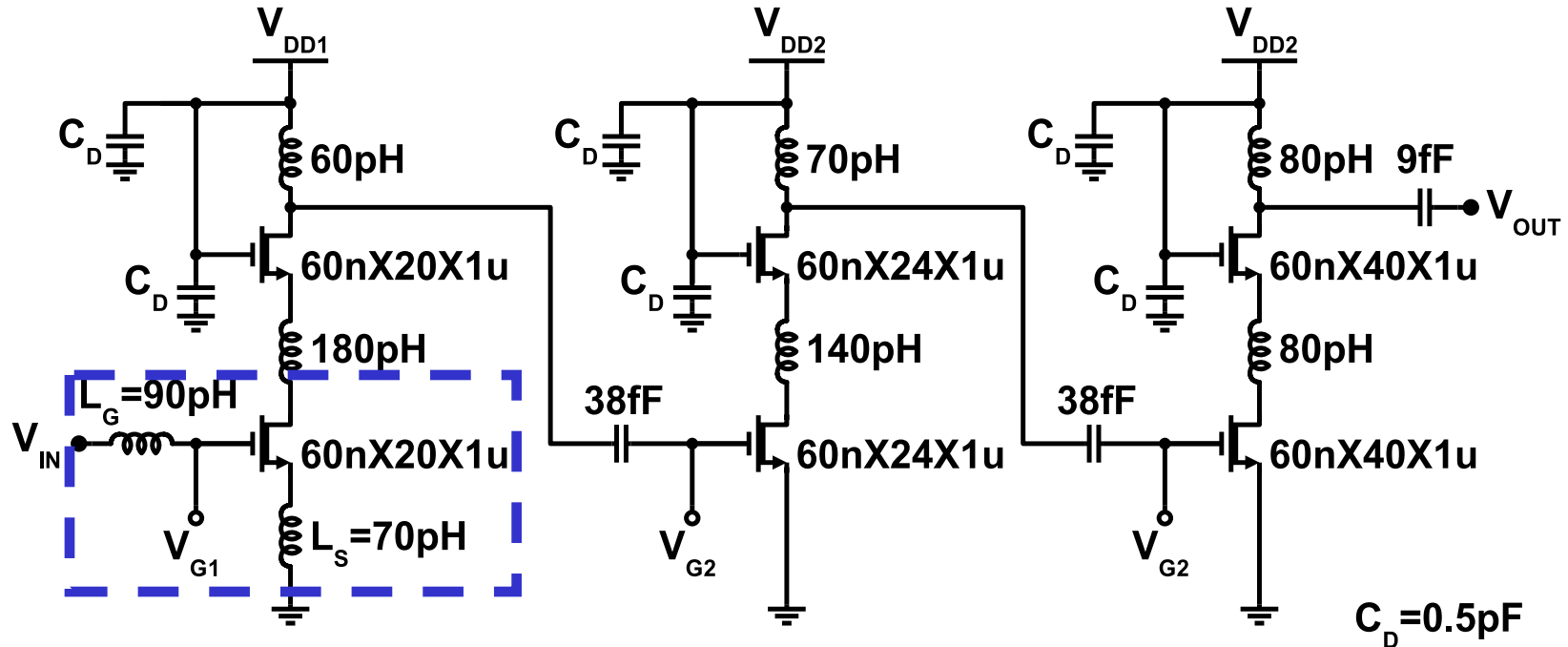
Motivation

- Investigation of W-band receivers in 65-nm GP CMOS
 - CMOS might provide alternatives to III-V and SiGe technology in imaging arrays:
 - Broadband (multi-GHz)
 - Low power
 - Low noise
 - Small area
 - Comparison of two LNA feedback topologies
 - Series-series feedback with inductor
 - Shunt-series feedback with transformer

Receiver Block Diagram

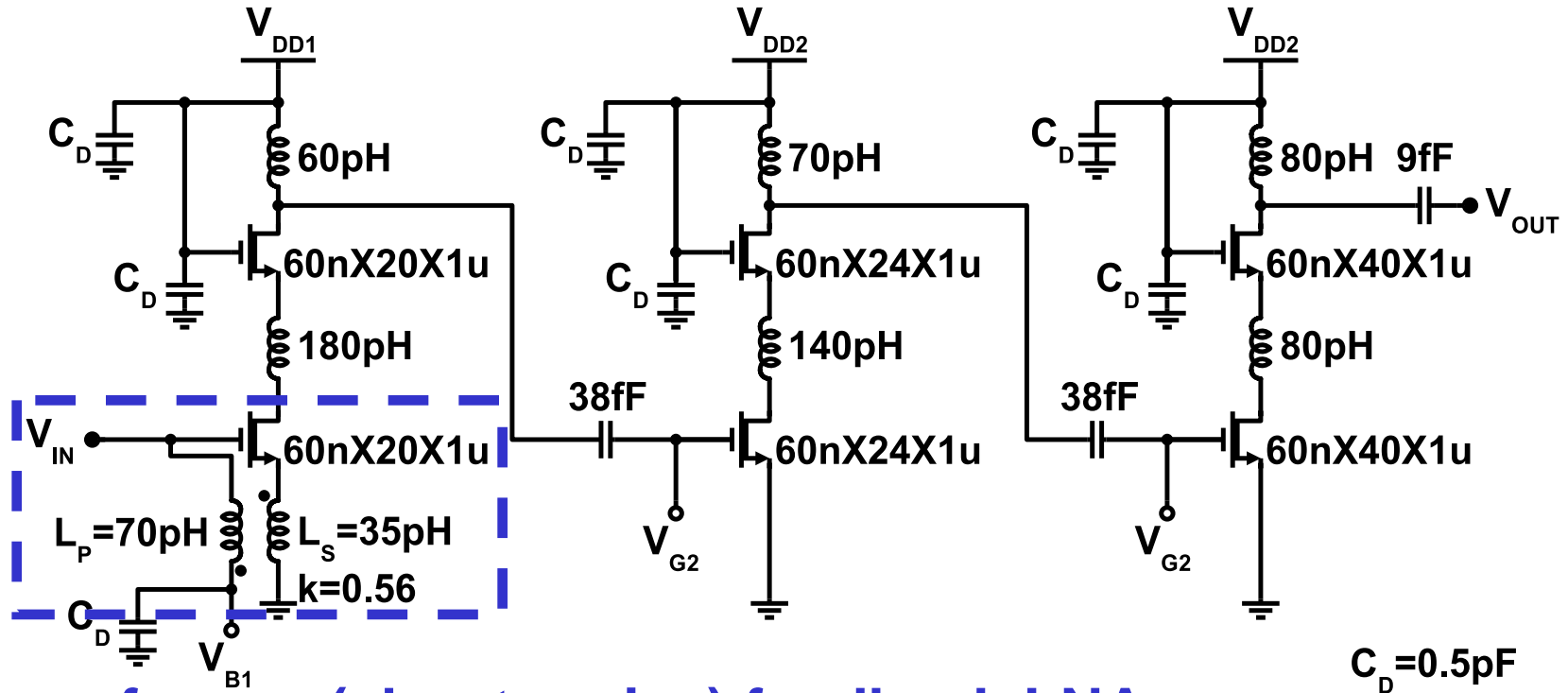


LNA – Schematic



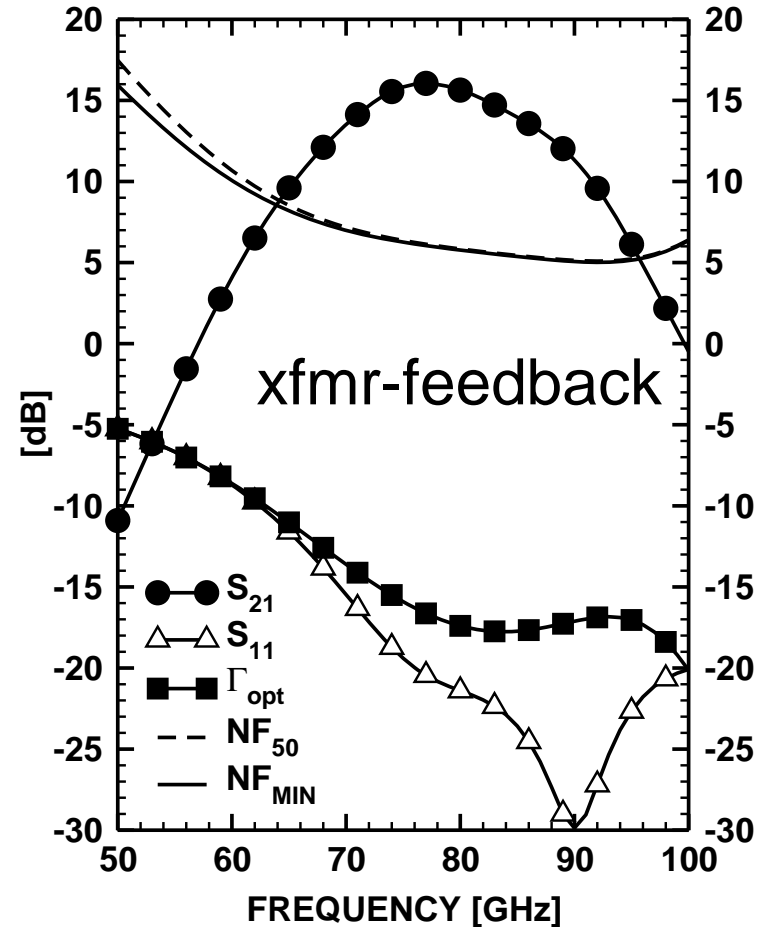
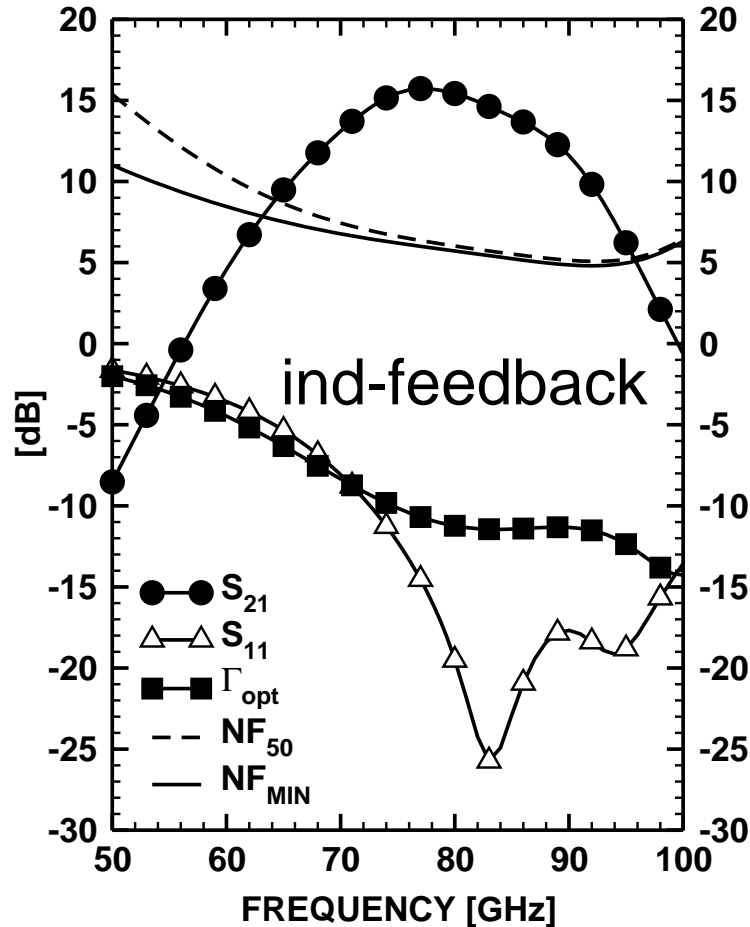
- Inductive (series-series) feedback LNA
- Input matched by L_G and L_S $\Re\{Z_{IN}\} = 2\pi f_T L_S + R_G + R_S$
- Noise impedance matched by transistor sizing and biasing

LNA – Schematic (2)



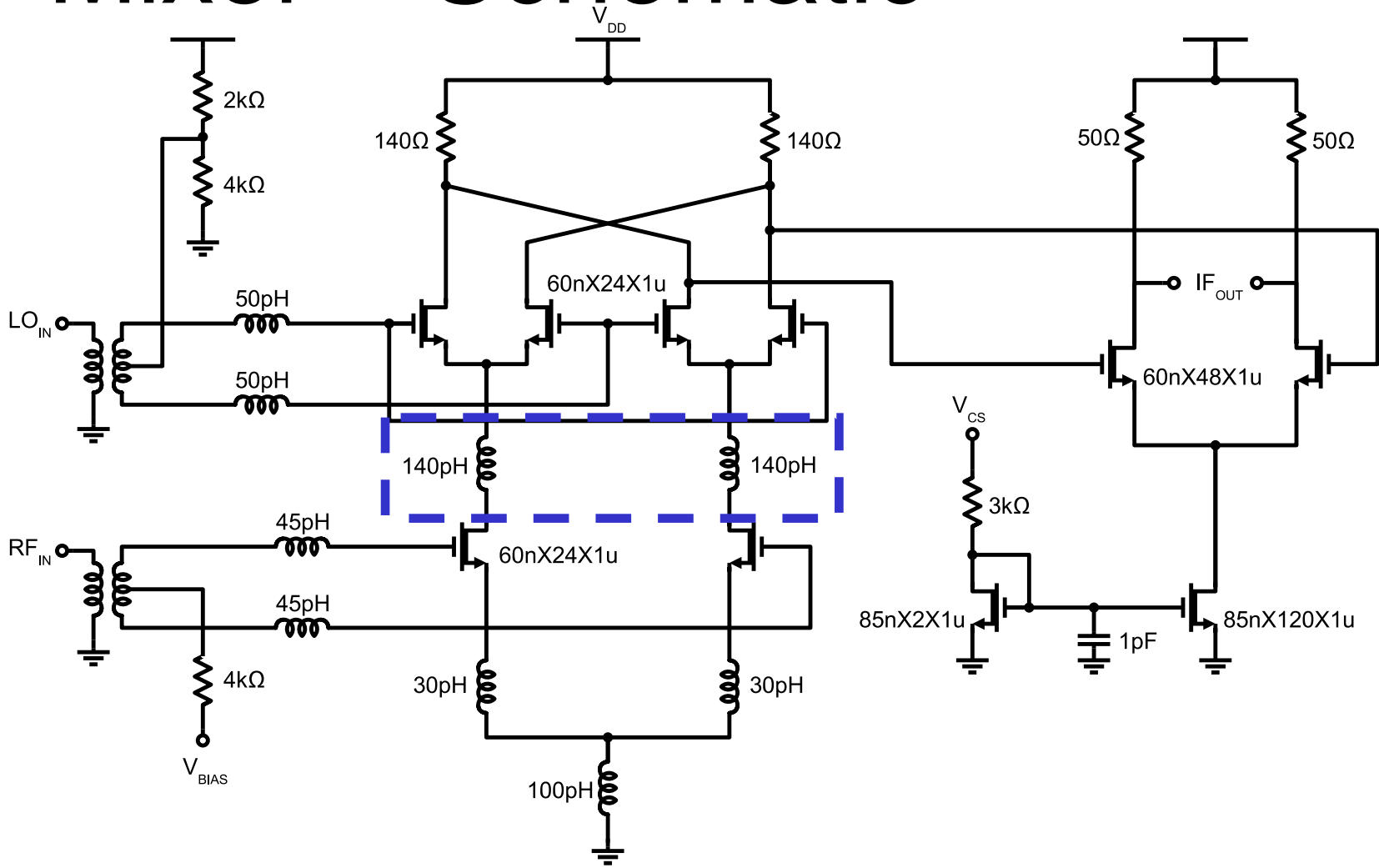
- Transformer (shunt-series) feedback LNA
- Input matched by L_P , L_S and M $\Re\{Z_{IN}\} \approx \frac{L_P}{g_m \cdot M}$, $M = k\sqrt{L_P L_S}$
- Noise impedance matched by transistor sizing and biasing

LNA – Simulation



- $S_{11}, \Gamma_{opt} < -10$ dB from 74-100 GHz for both designs

Mixer – Schematic

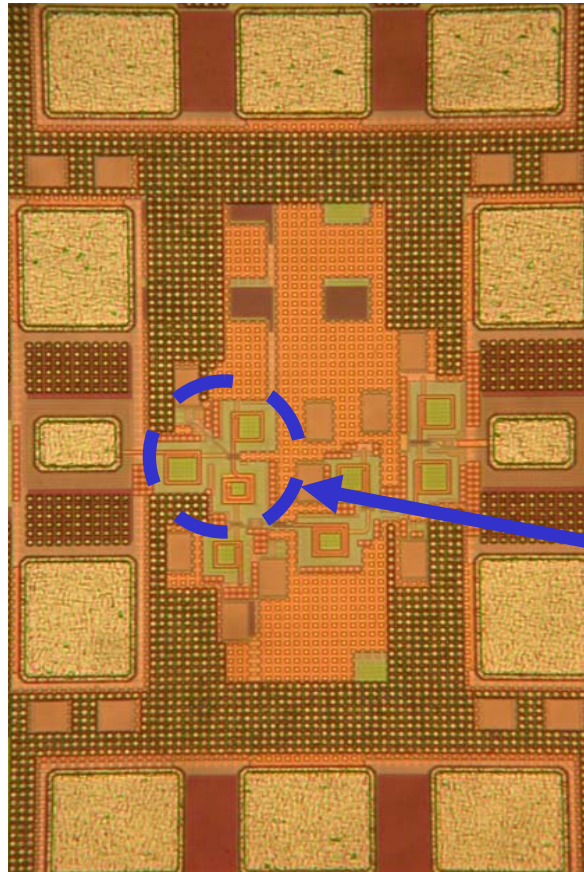


- **Gilbert cell mixer with inductive broad-banding**

Fabrication

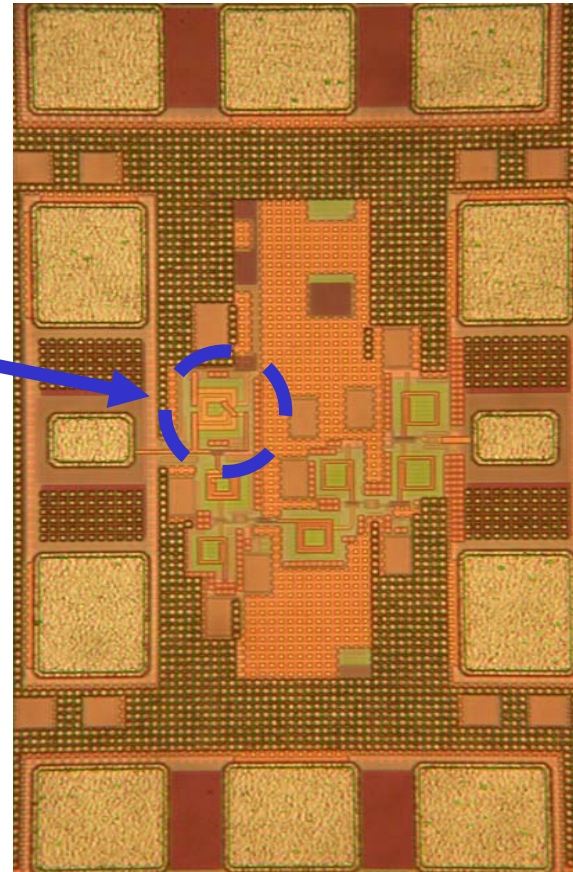
- 65-nm GP/LP digital CMOS process
- 7 metal layers
- GP n-MOSFETs ($80 \times 60 \text{ nm} \times 1 \mu\text{m}$) with gate contacted on one side: $f_T/f_{\text{MAX}} = 170 \text{ GHz}/200 \text{ GHz}$ at $V_{\text{DS}} = 0.7 \text{ V}$
- GP MOSFETs 30% faster than LP MOSFETs and require lower V_{GS} and $V_{\text{DS}} \rightarrow$ lower power
- Gate leakage does not affect mm-wave performance

LNA breakouts – Die Photos



IND-feedback

XFMR

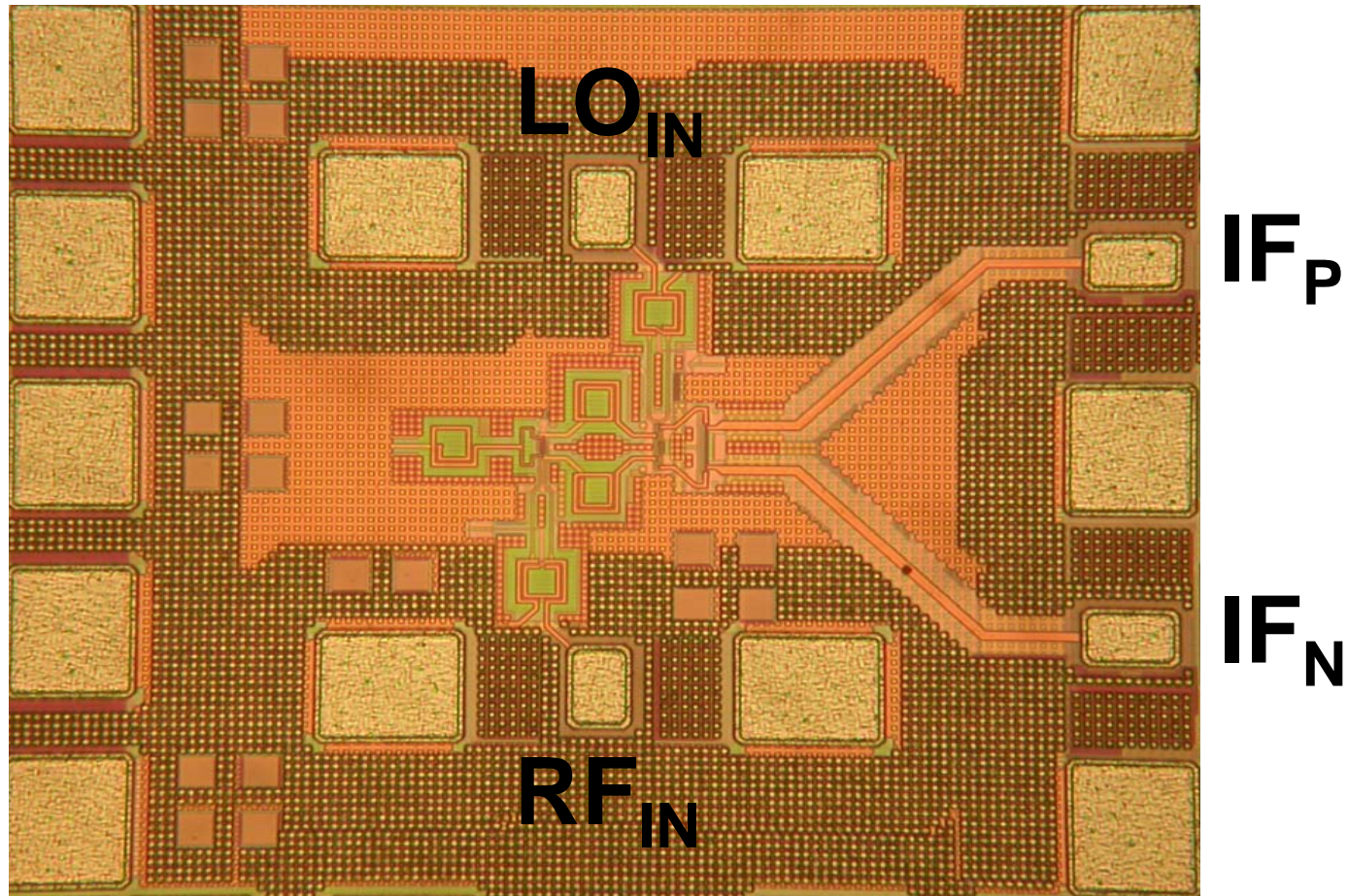


XFMR-feedback

IND

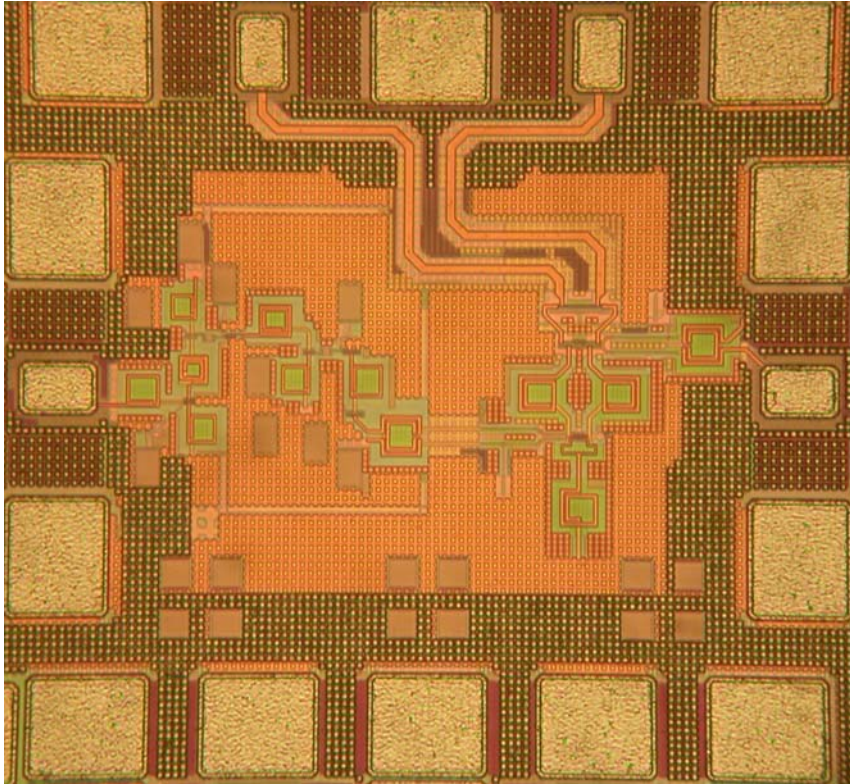
490 um x 300 um (pad) → 120 um x 170 um (core)

Mixer breakout – Die Photo

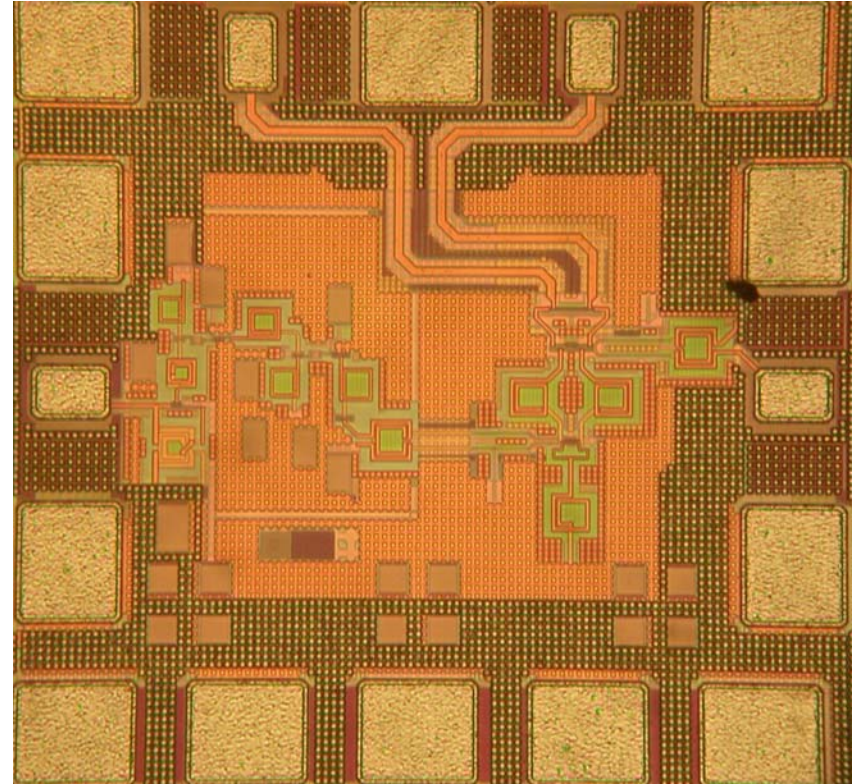


470 μm x 560 μm (pad) \rightarrow 190 μm x 160 μm (core)

Receiver – Die Photos



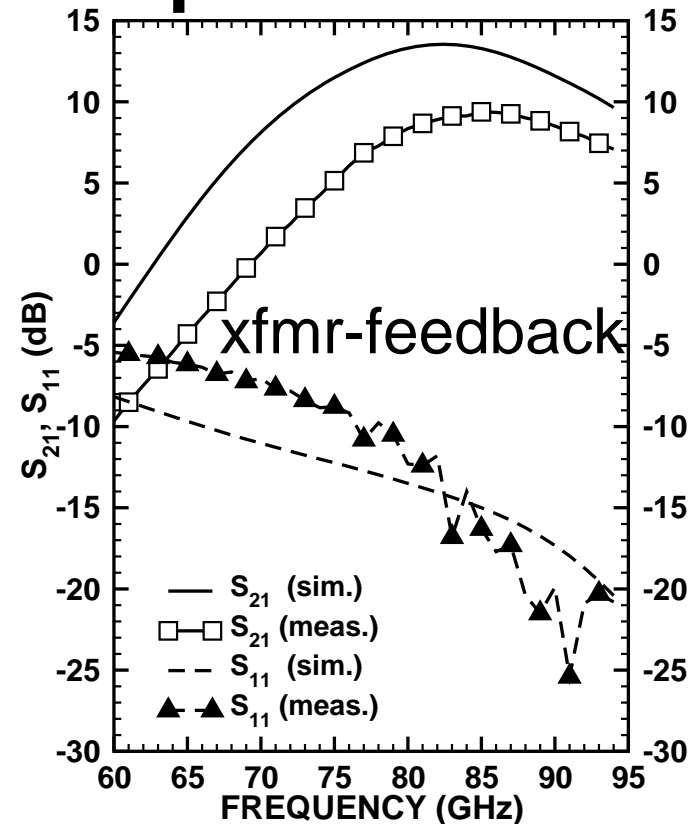
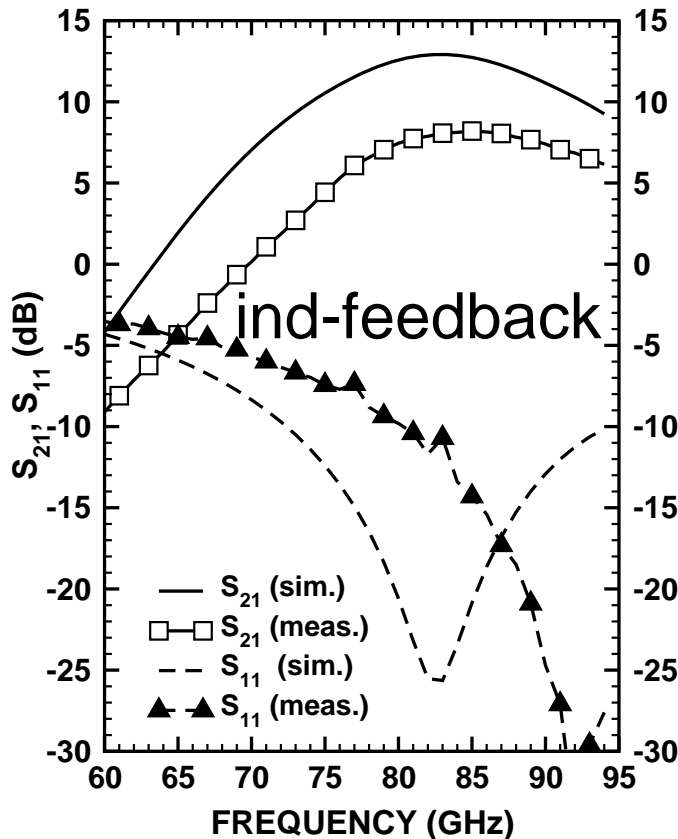
IND-feedback Receiver



XFMR-feedback Receiver

460 um x 500 um (pad) → 160 um x 370 um (core)

Meas. LNA – 1st Spin



- Requires 2.2 V V_{DD} for 8 – 9 dB gain
- 4 – 5 dB below simulation

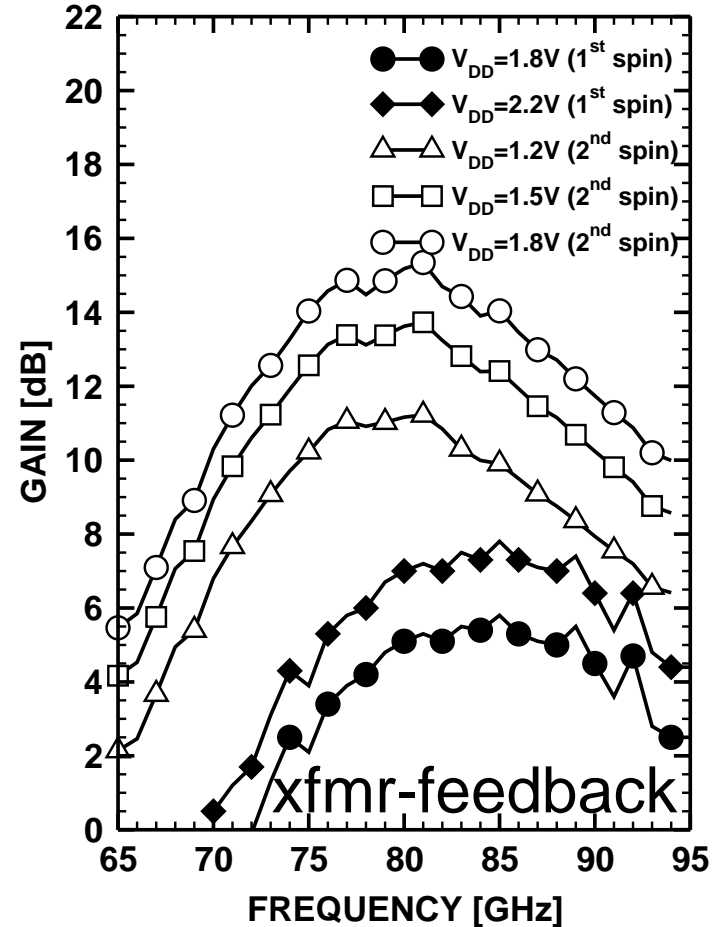
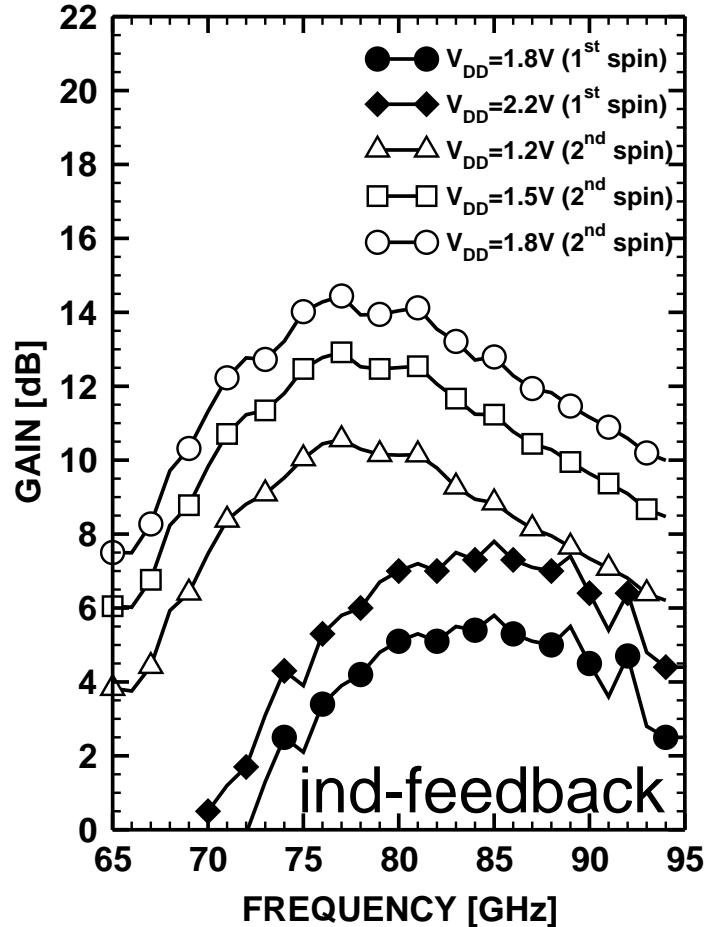
Measurements for 2nd Spin with Modified Layout

Series resistance in ground metallization of LNA was found in the first spin.

A second spin of the design was fabricated with:

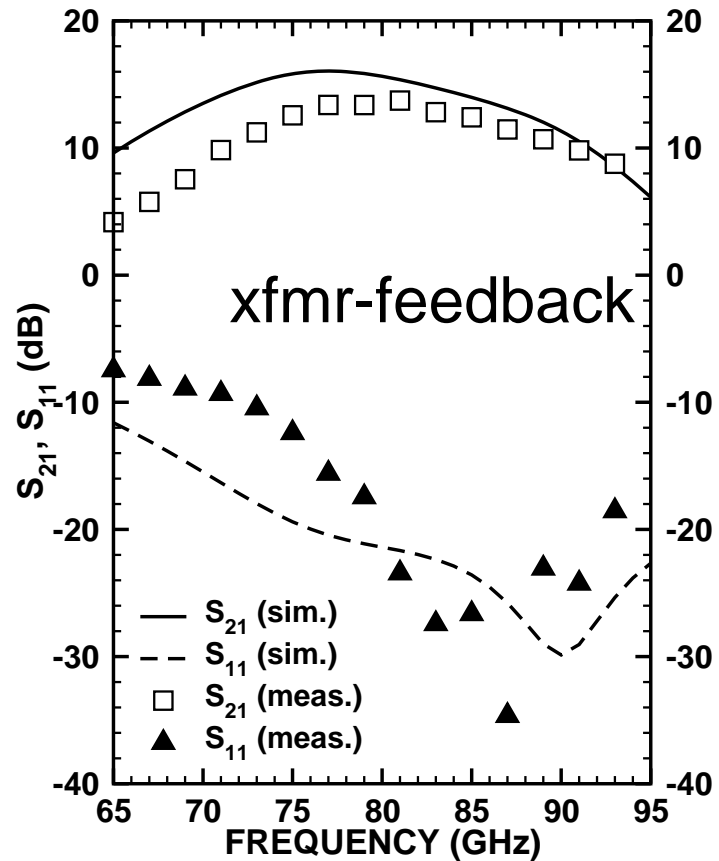
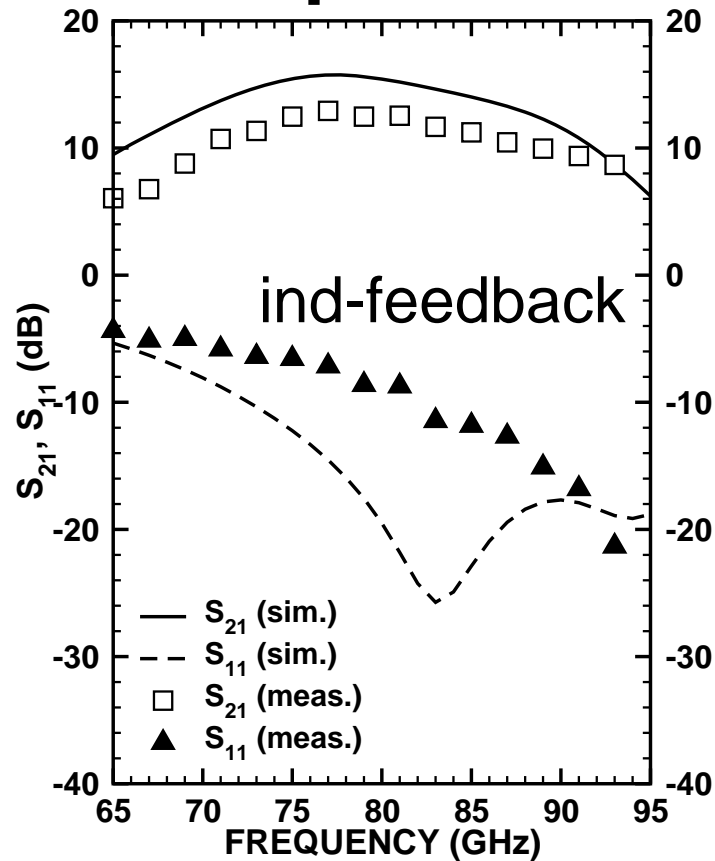
- Wider metal lines in ground mesh at top level
- Increased number of vias (even between M5 and M6)
- LNA inductance values adjusted to match @ 80 GHz

Meas. LNA – 2nd Spin



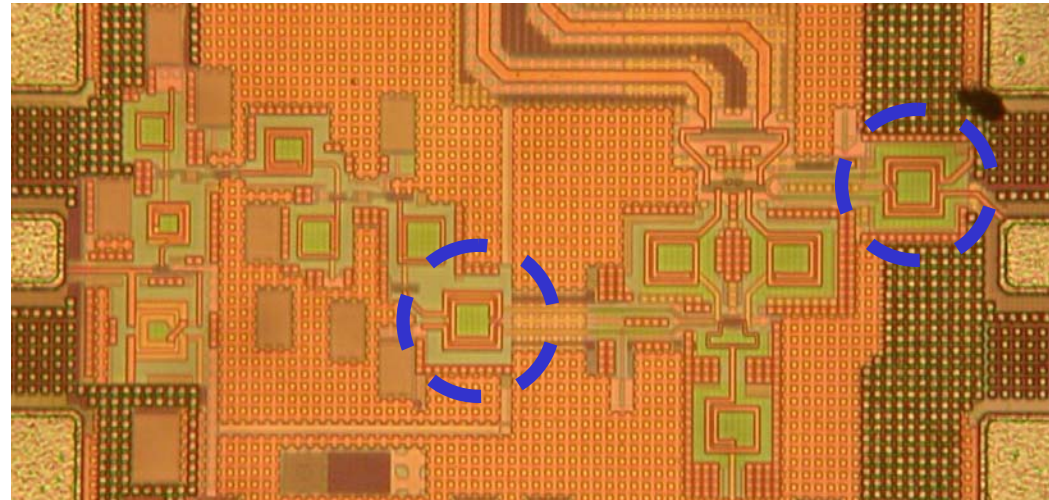
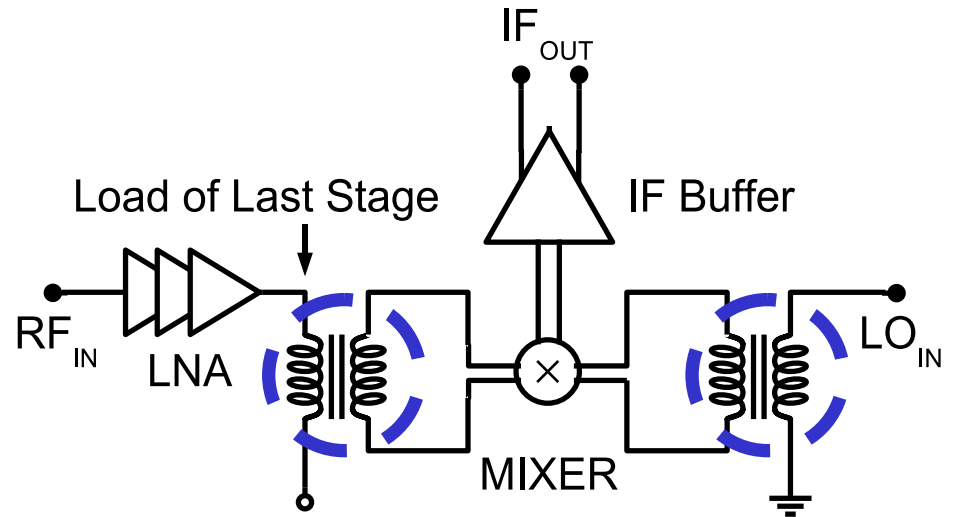
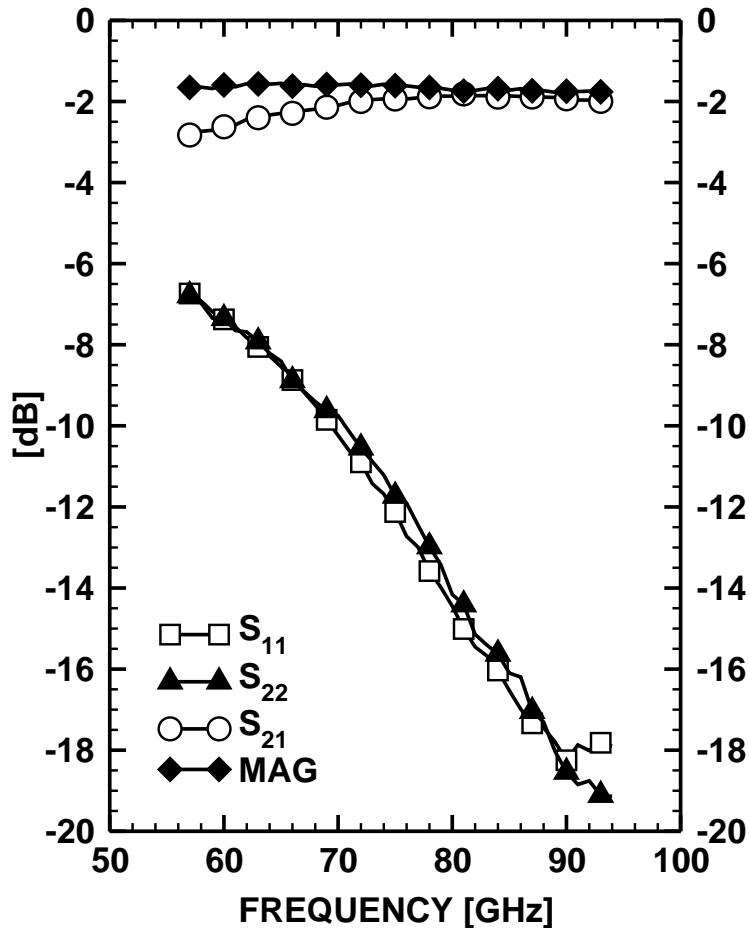
- Measured gain @ 1.5 V V_{DD} = 13 dB

2nd Spin LNA – meas. vs sims.



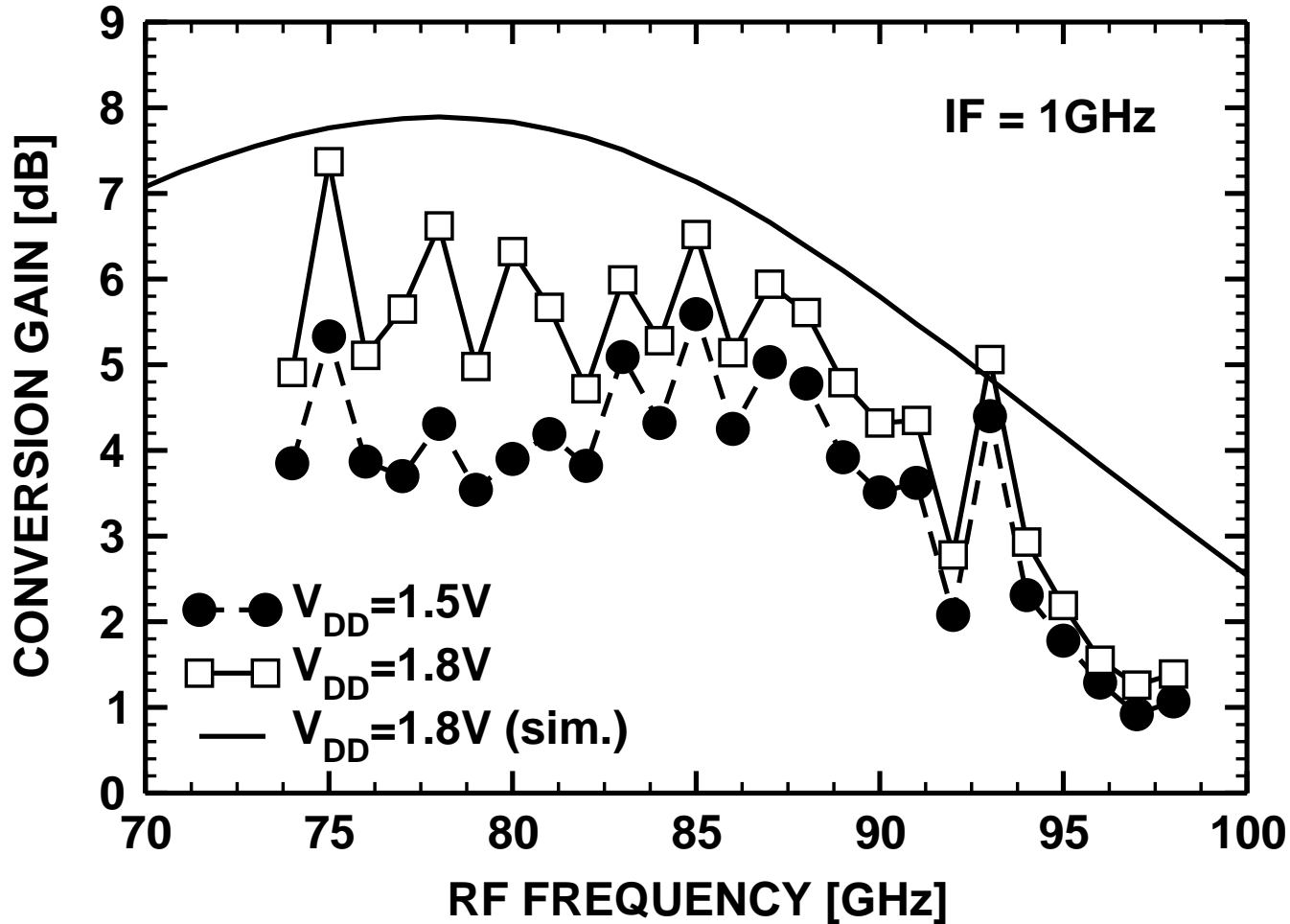
- Meas. gain @ $V_{DD} = 1.5$ V is 1 – 2 dB below sims.
- $S_{11} < -20$ dB from 80 – 90 GHz (xfmr-feedback)

Meas. Transformer S-params.



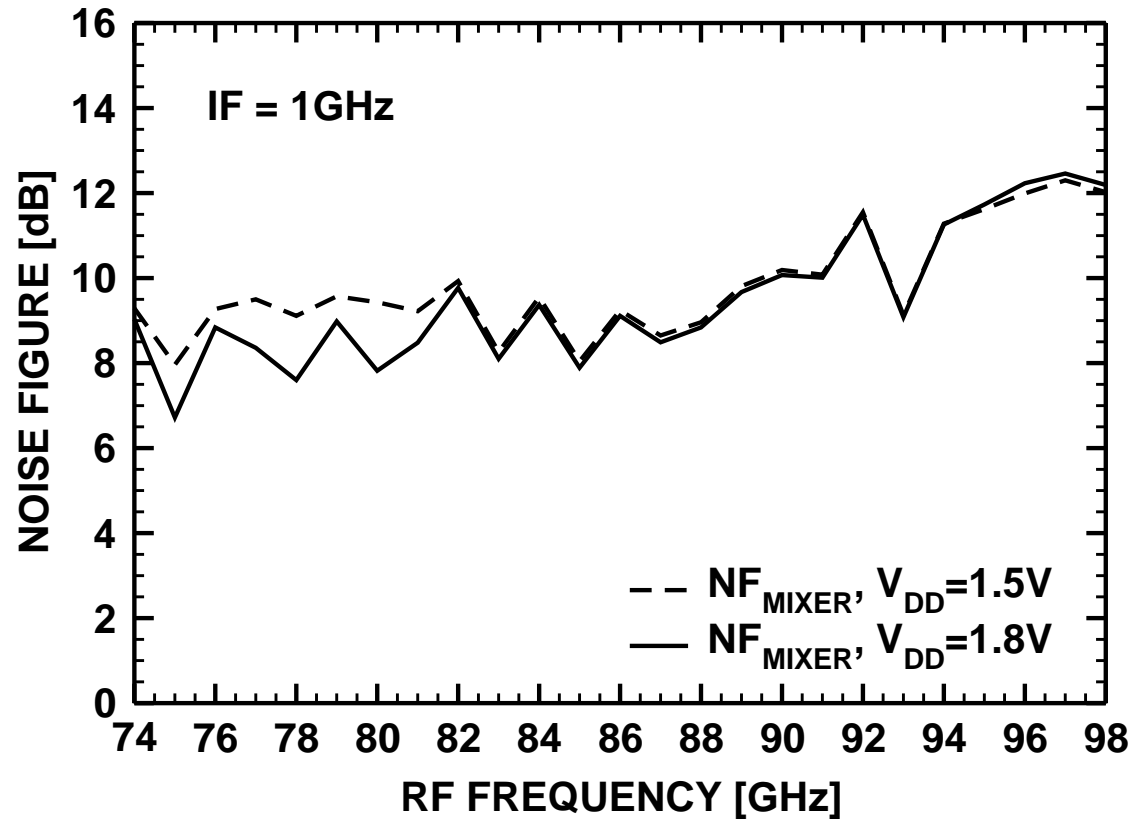
- **MAG (loss) < -2 dB between 75 – 95 GHz**

Meas. Mixer – Conversion Gain



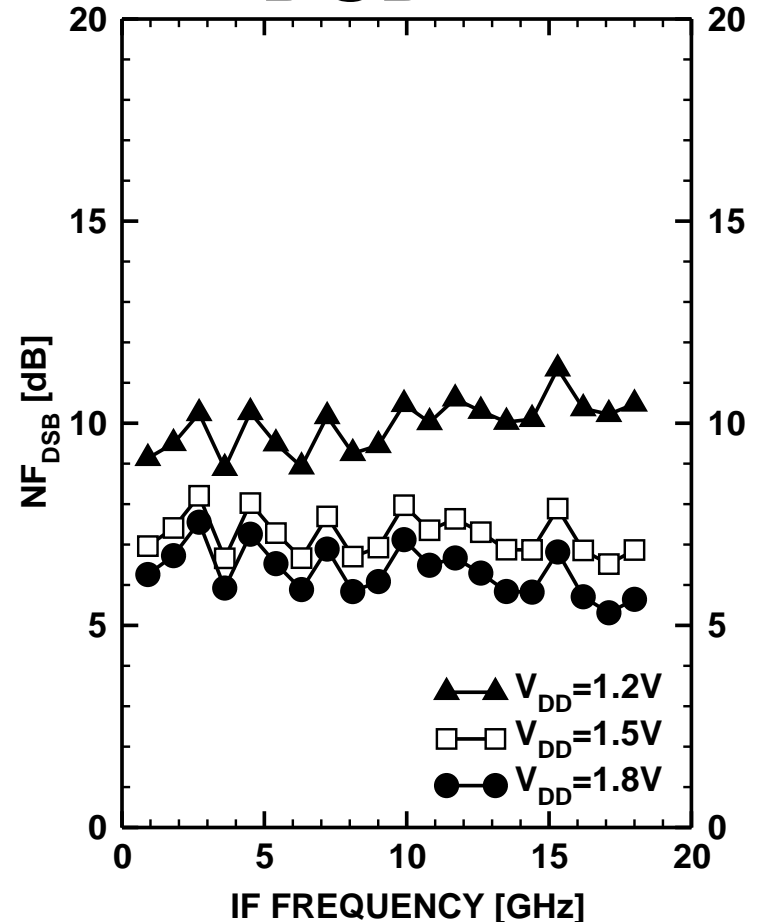
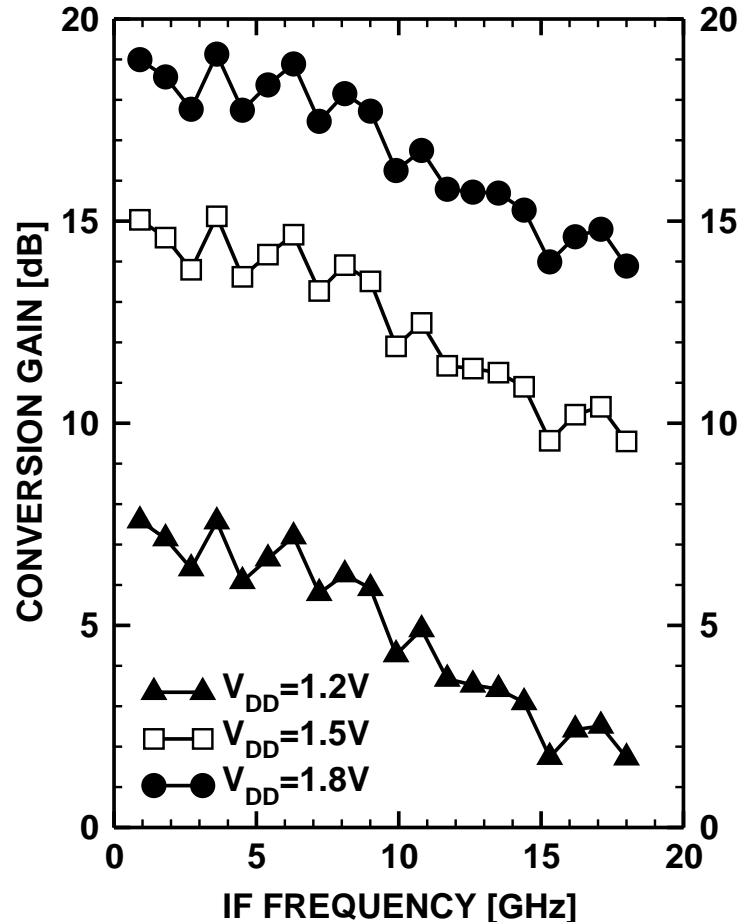
- 1 – 2 dB below simulation

Meas. Mixer – NF_{DSB}



- Includes ~2 dB transformer loss
- Lowest NF_{DSB} mixer at 80 – 90 GHz in silicon

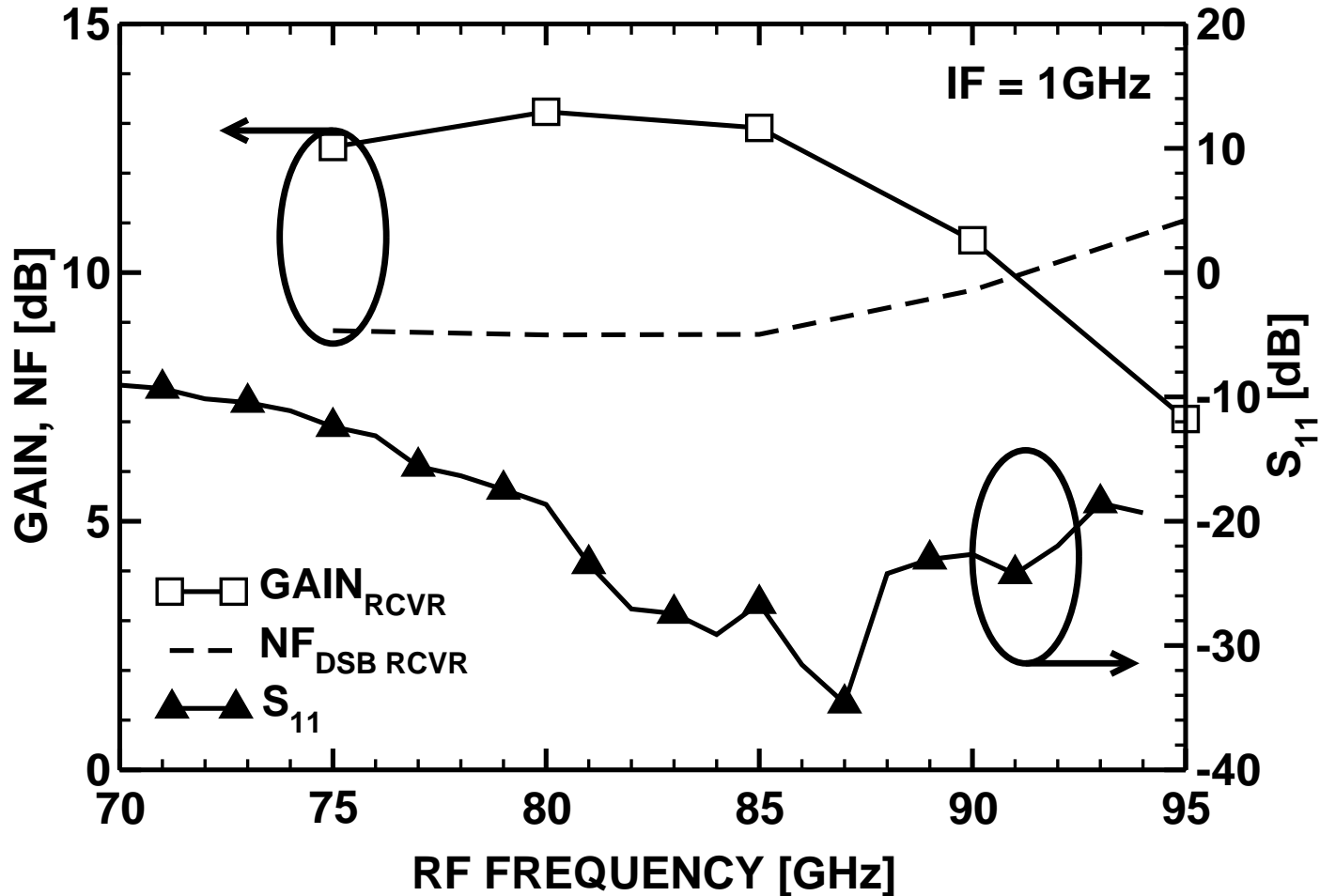
Meas. Rx Gain, NF_{DSB} vs IF



XFMR-feedback RCVR

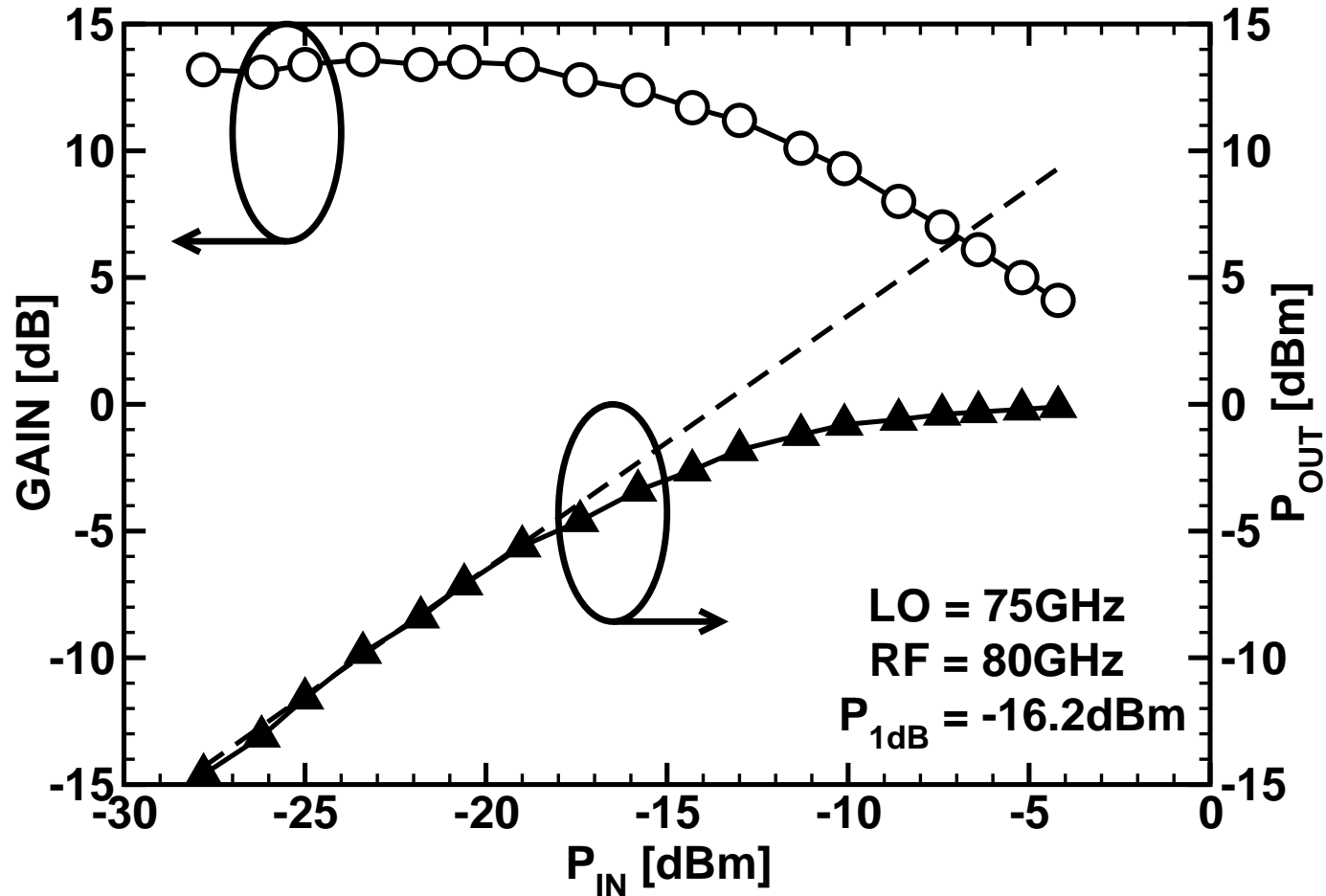
- $NF_{DSB} \sim 7 - 8$ dB, LO @ 89 GHz

Meas. Rx Gain, NF_{DSB} vs RF



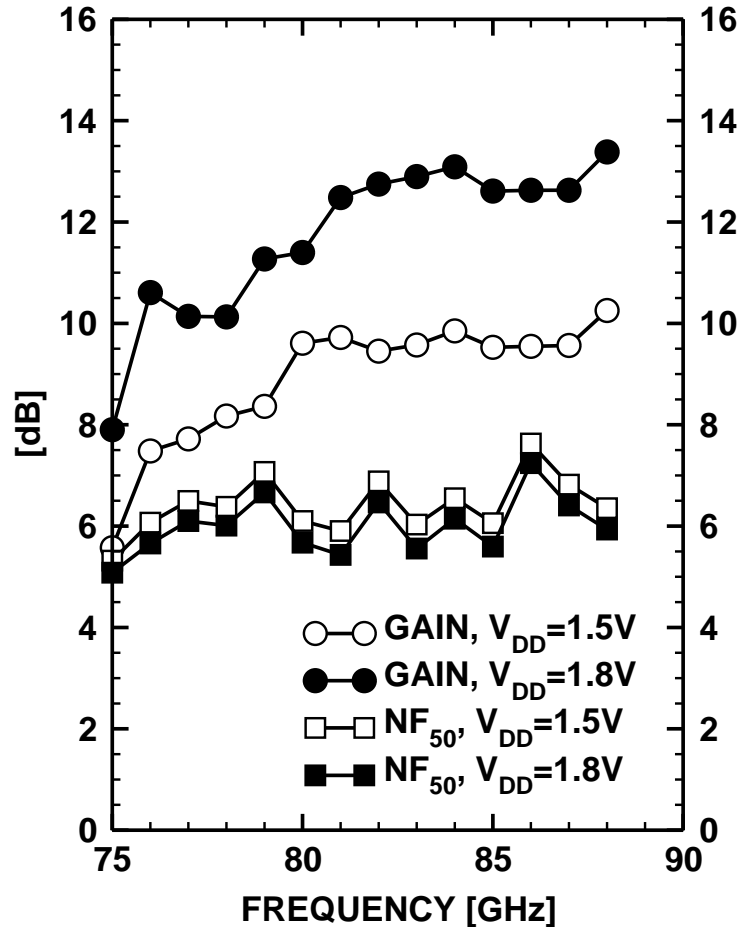
- 3dB-bandwidth: 75 – 91 GHz

Receiver – P_{1dB}



- LO @ 75 GHz due to equipment limitation

Estimated LNA NF



XFMR-feedback LNA

$$G_{LNA} = G_{RCVR} - G_{MIXER}$$

$$F_{LNA} = F_{RCVR} \frac{F_{MIXER}^{-1}}{G_{LNA}}$$

- LNA gain peaks at frequency higher than measured (output pad capacitance removed)
- LNA NF₅₀ ~6 – 7 dB

Summary of Results

1st Spin	V_{DD} [V]	LNA		IF Buffer	Receiver			
		P_{diss} [mW]	Gain [dB]	P_{diss} [mW]	P_{diss} [mW]	Gain [dB]	NF [dB]	S_{11} [dB]
1st Spin	1.8	38	5.8	47	95	11.6	9 – 10	< -10 (80-95+ GHz)
	2.2	57	7.8	75	150	13.5	8 – 9	
2nd Spin	1.2	24	11.1	20	48	6.1	9 – 10	< -10 (74-95+ GHz)
	1.5	34	13.4	30	71	13.6	7 – 8	
	1.8	48	14.9	45	104	17.7	6 – 7	

- **Dramatic increase in performance just with better top-level ground mesh and vias**
- **$\sim 1/2$ of P_{diss} used in IF buffer to drive 50Ω off-chip**

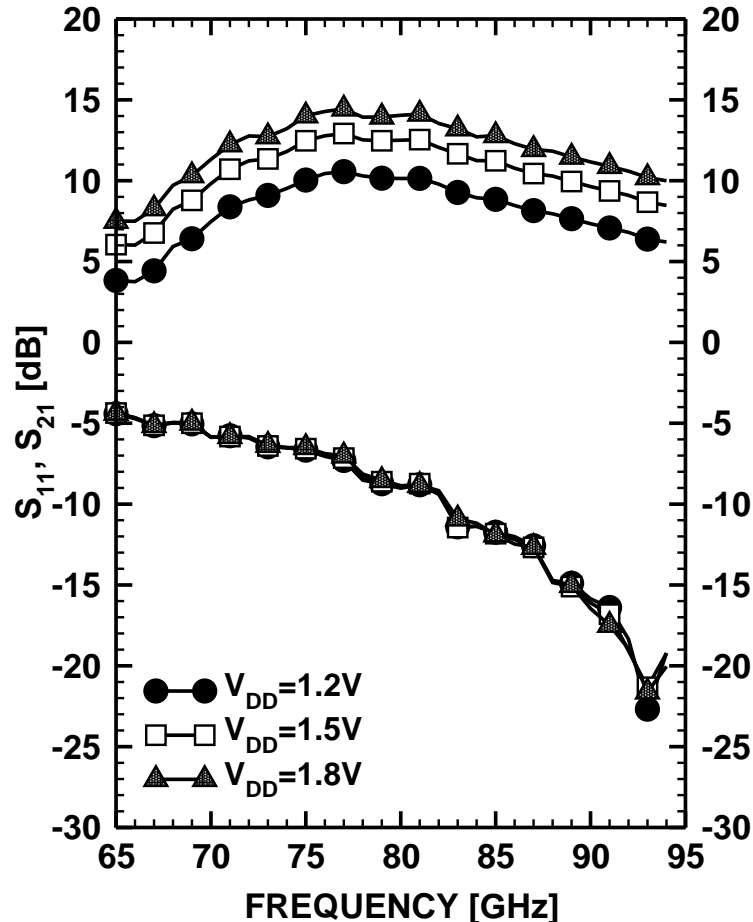
Conclusion

- 74 – 94 GHz receiver with 8 dB NF and 13 dB gain demonstrated in 65 nm GP CMOS technology.
- Inductive-feedback and transformer-feedback LNA topologies presented:
 - Similar performance achieved by different matching procedures
- Layout style significantly affects circuit performance.
- Post-layout simulation at top-level, with ground mesh must be carried out.

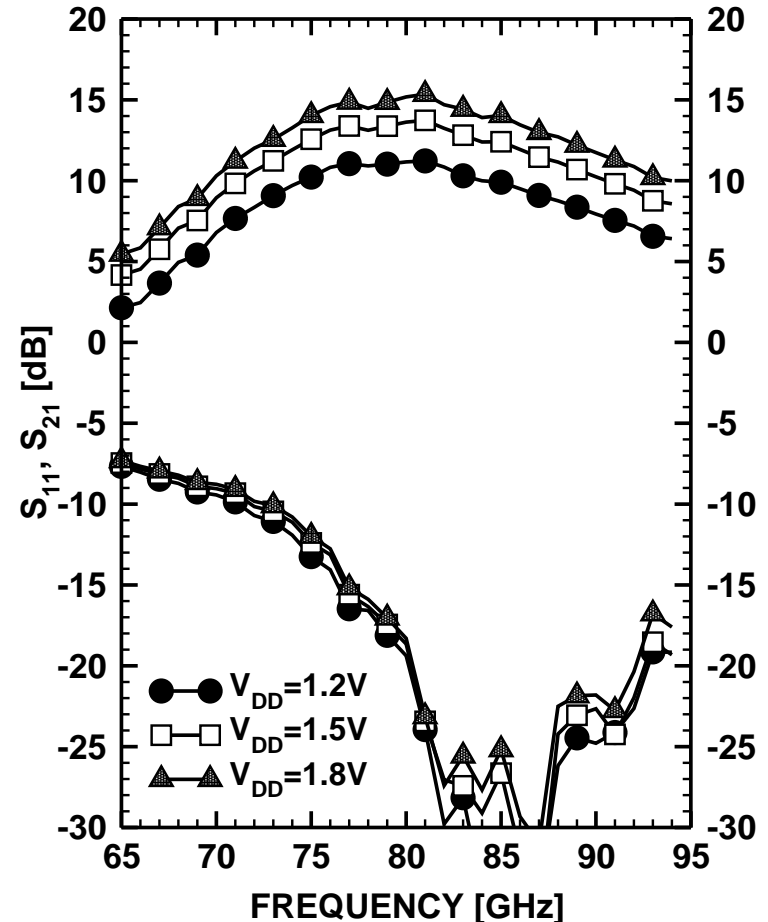
Acknowledgement

- Katya Laskin for measurements on the second-spin
- Alex Tomkins for inductor and transformer measurements
- Jaro Pristupa and CMC for CAD tools
- Bernard Sautreuil of STM for facilitating the technology access
- CITO for funding
- ECTI, NSERC, CFI and OIF for equipment

2nd spin LNA – Meas. Gain



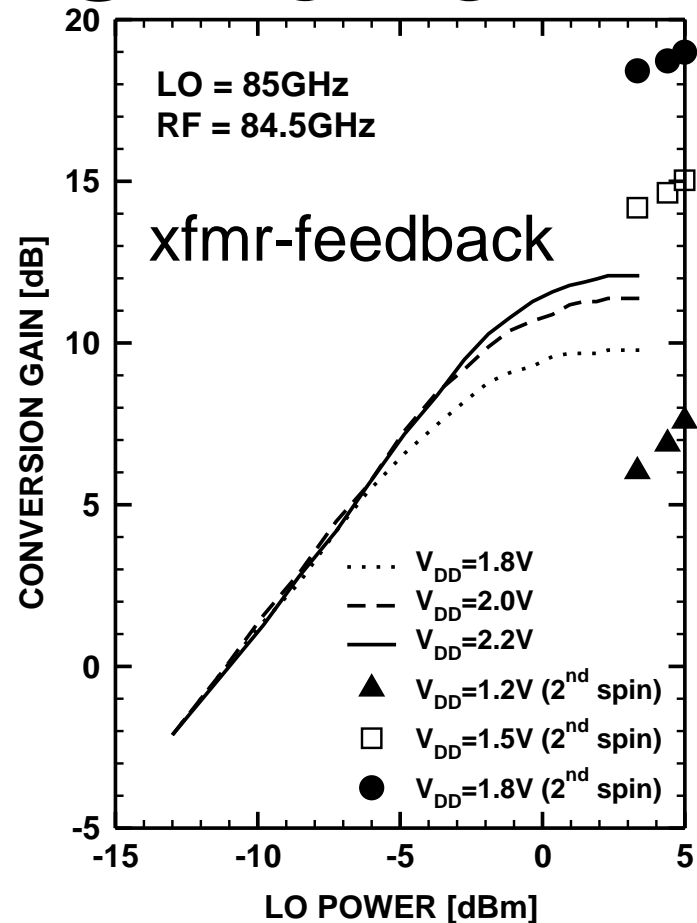
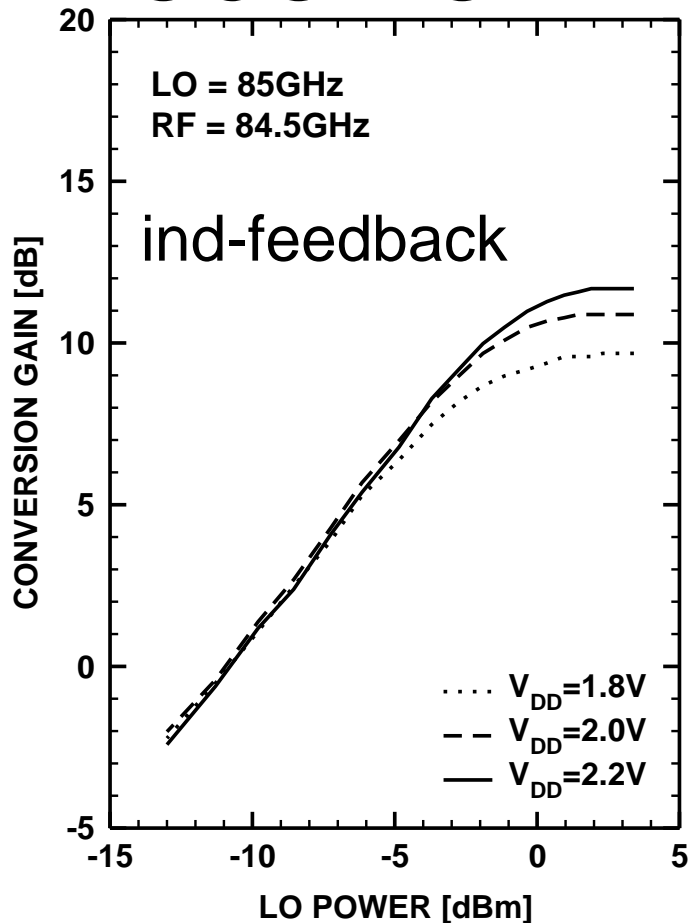
IND-feedback LNA



XFMR-feedback LNA

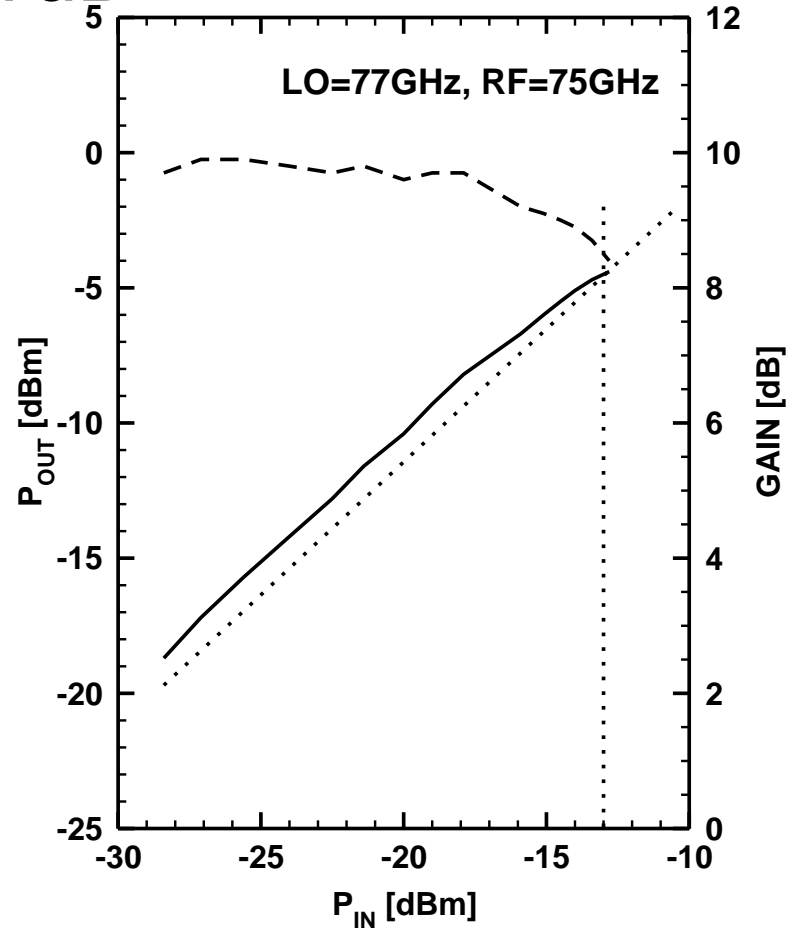
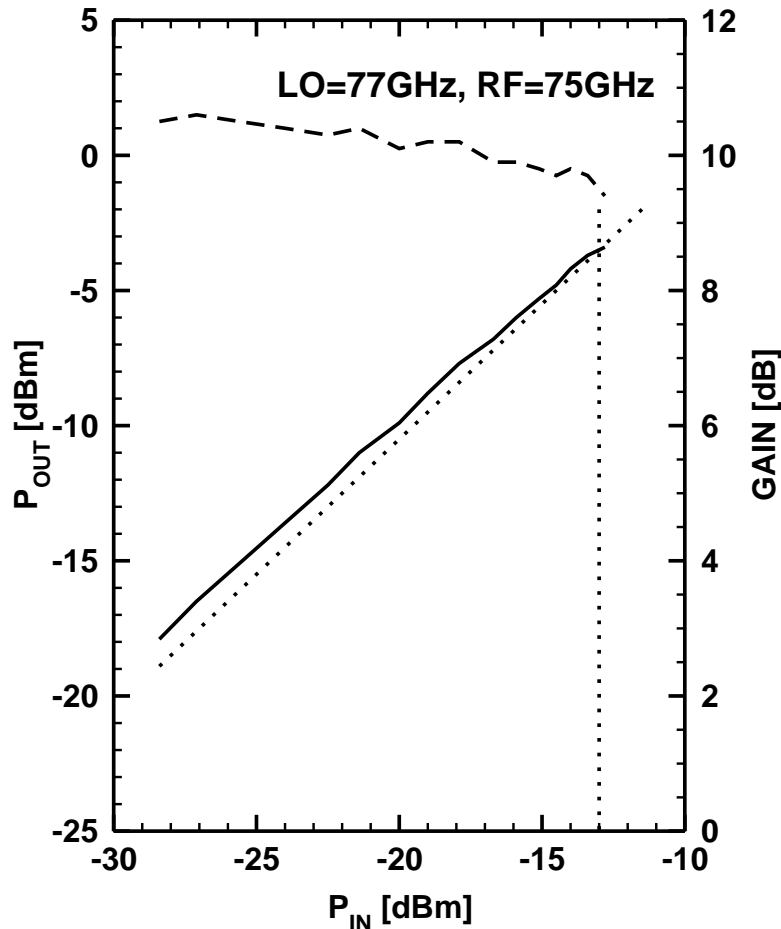
- S_{11} matched at 93 GHz for inductive-feedback LNA (increase L_G)

Receiver – vs LO Power



- Requires 2 – 3 dBm (1st spin) and > 5 dBm (2nd spin) LO power

Receiver – P_{1dB}



IND-feedback Receiver

XFMR-feedback Receiver

- RF at 75 GHz due to equipment limitation

