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Cryogenic Characterization of 22nm FDSOI CMOS Technology for Quantum Computing ICs

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***Abstract*— An approach is proposed to realize large-scale, "high-temperature" and high-fidelity quantum computing ICs based on single- and multiple coupled quantum-dot electron- and hole-spin qubits monolithically integrated with the mm-wave spin manipulation and readout circuitry in commercial CMOS technology. Measurements of minimum-size 6nmx20nmx80nm Si-channel n-MOSFETs (electron-spin qubit), SiGe-channel p-MOSFETs (hole-spin qubit), and double quantum-dot complementary qubits reveal strong quantum effects in the subthreshold region at 2 K, characteristic of resonant tunneling in a quantum dot. S-parameter measurements of a transimpedance amplifier (TIA) for spin readout show improved performance from 300 K to 2 K. Finally, the qubit-with-TIA circuit has 50Ω output impedance, 78dBΩ transimpedance gain with unity-gain bandwidth of 70 GHz and consumes 3.1 mW.**

***Index Terms*— CMOS, cryogenics, monolithic integrated circuits, quantum information processing, radio frequency, semiconductor quantum dots, silicon, silicon-on-insulator**

I. INTRODUCTION

SILICON-based electron-spin [1-3] and hole-spin [4-5] coupled quantum-dot (QD) qubits [6] have attracted a lot of interest recently due to their potential for integration in commercial CMOS technology. However, to date, because of the low confinement and coupling energies (e.g. ΔE, in the tens of μeV range, comparable to the thermal noise level, k_BT, at 100 mK) their operation has been restricted to temperatures below 100 mK. Moreover, since cryogenic systems cannot remove more than a few mW of thermal power at 100 mK, and the experimental laboratory technologies in which these qubits have been realized do not allow for fabrication of spin manipulation and readout circuitry, the latter reside on a separate chip, at 4 K or higher temperature [7]. The lack of monolithic integration further degrades readout fidelity and computing speed because the atto-Farad capacitance, high-impedance qubit needs to drive 50Ω and 100x larger capacitance interconnect off-chip. A qubit with higher confinement and coupling energies, with spin resonance in the upper mm-wave region, will allow for higher temperature operation, alleviating these problems and enabling large-scale monolithic quantum computing processors. For example, a qubit operating at 4 K would require mode splitting energies of 0.25 meV which corresponds to a spin resonance frequency of 60 GHz. The goal of this paper is to study the feasibility of high-temperature (high-T) Si and SiGe electron/hole-spin qubits and qubit integrated circuits (ICs) in commercial 22nm FDSOI CMOS technology [8] and to explore their scalability through simulation to 2nm dimensions, when the coupling energy, ΔE, becomes comparable to thermal noise at 77-300 K. For the first time we report (i) integration of qubits and electronics on the same die, (ii) strained SiGe hole-spin and strained Si electron-spin FDSOI qubits on the same die, and (iii) propose a monolithic processor architecture which allows for short, 10-20ps spin control pulses and high Rabi frequencies, f_{Rabi}, to compensate for short spin phase coherence lifetime. We also demonstrate that, at 2 K, MOSFETs and cascodes can be operated as QDs in the subthreshold region while behaving as classical MOSFETs and cascodes in the saturation region, suitable for qubits and mm-wave mixed-signal processing circuits, respectively.

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II. FDSOI N- AND P-TYPE QUBITS

As sketched in Fig. 1(a), the qubits are realized using series-stacked Si n-MOSFET and SiGe p-MOSFET minimum size cascodes with multiple gates. QDs are formed in the thin (~6 nm) undoped semiconductor film below each top gate, while the tunneling barrier (and, therefore, electron or hole entanglement and exchange interaction between QDs) is controlled by the back gate formed in the Si substrate below the 20nm buried oxide (BOX) [8] or by top gates. The physical gate length and width are L = 20 nm and W_f = 80 nm, respectively, while the gate pitch is approximately 100 nm. A top-level layout view of the fabricated n-qubit is provided in Fig. 1(b), where the two active gates and the three dummy gates on each side of the qubit are drawn in red. A blocking mask (in blue) is placed between the two gates of the coupled double-QD qubit to prevent ion implantation and contact formation in the undoped channel. Fig. 2(a) shows the TCAD-simulated conduction band profiles and energy levels along the z-direction, perpendicular to the gate-channel interface.

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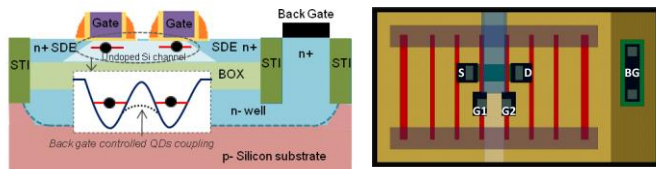

Fig. 1. n-MOSFET cascode as two coupled quantum dot qubits (a) vertical cross-section (b) 20nmx80nm double-QD qubit top-view layout

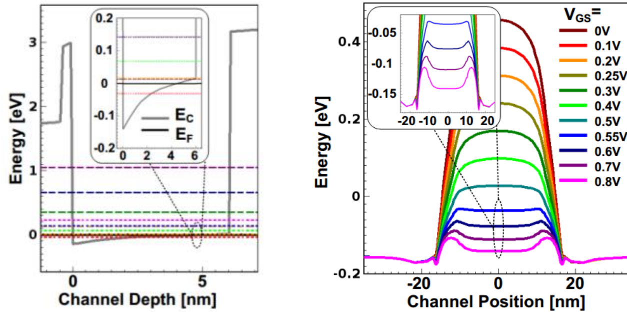

Fig. 2. Simulated n-MOSFET conduction band profile (a) along the z-direction (eigen-energy levels also shown) and (b) along the x-direction (for V_{GS} = 0 to 0.8V and backgate voltage V_{BG} = 0V).

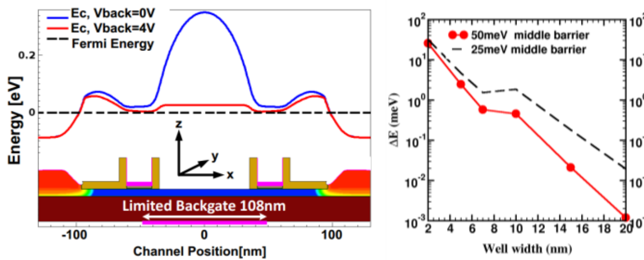

Fig. 3. Coupled-QD simulations of (a) conduction band profile along the channel illustrating barrier height control from a back-gate placed only below the spacer between the two top gates and (b) the coupling energy as a function of double-QD well and barrier width.

The simulated conduction band profile at 77 K along the n-MOSFET channel (x-direction) is reproduced in Fig. 2(b) for various V_{GS} values and V_{DS} of 1 mV. It appears that the gate-source and gate-drain spacers are sufficient to form 10meV parabolic potential barriers which confine the carriers between source and drain in the x-direction. Confinement along the y- and z-directions is provided by the gate oxide, BOX, and STI, which act as infinite potential barriers. Fig. 3(a) shows the conduction band and Fermi-level profiles in the double-QD qubit at 300 K, illustrating how the height of the potential barrier between the two QDs could be controlled by a n-well placed selectively only below the barrier region. Simulations of coupled QD scaling in future technology nodes are reproduced in Fig. 3(b) indicating that $\Delta E > 30$ meV will be possible at 2nm minimum feature size. This suggests that room-temperature operation may become feasible in the next 15 years.

III. Cryogenic Measurements

Transistors, qubits, TIAs, and qubit-with-TIA circuits were fabricated in a production 22nm FDSOI technology [8]. On-die dc and S-parameter measurements were carried out at 300 K and at 2 K with a Lake Shore CPX VLT system. As can be observed in Fig. 4, interesting features appear in the transfer characteristics of single-finger minimum-size 20nmx80nm MOSFETs at 2 K, which are not present at 300 K [8]. Current

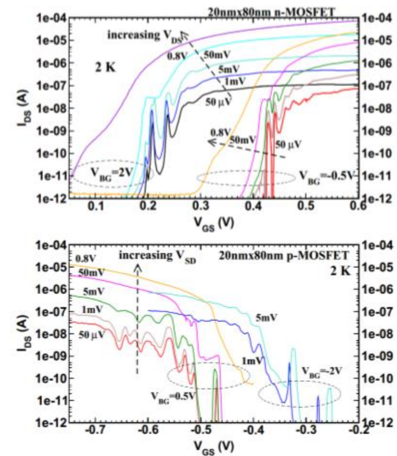

Fig. 4. Measured MOSFET transfer characteristics vs. back-gate voltage and V_{DS} at 2 K for (a) n-MOSFET and (b) p-MOSFET.

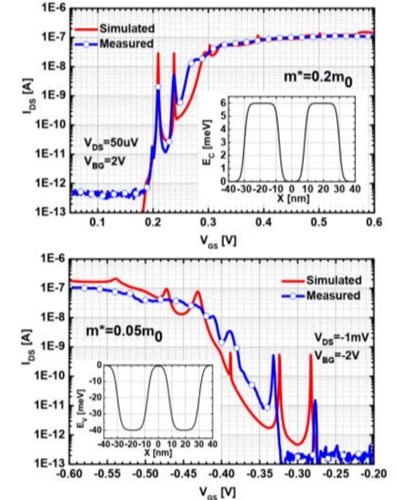

Fig. 5. 1x20nmx80nm measured vs simulated transfer characteristics at 2 K for assumed conduction/valence band profile and effective mass shown in the inset for the (a) n-MOSFET and (b) p-MOSFET.

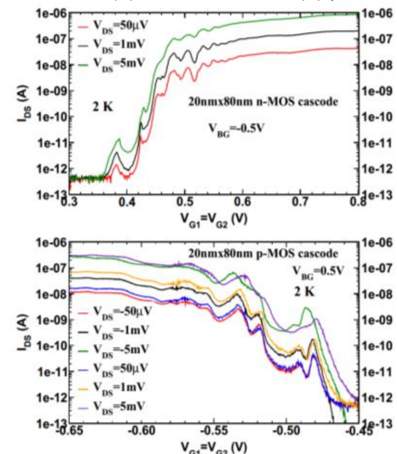

Fig. 6. Measured double-QD transfer characteristics vs. V_{DS} at V_{BG}=±0.5 V and 2 K for (a) n- double-QD and (b) p- double-QD.

oscillations with large peak-to-trough ratios appear at V_{DS} < 50 mV in both n- and p-MOSFETs. The oscillatory behavior is the signature of electron/hole resonant tunneling through the discrete energy levels of the QD. The separation between adjacent peaks, ΔV_{GS}, depends on the energy level separation in the channel QD and is inversely proportional to the effective mass and the capacitance between the top gate and

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the charge centroid in the channel, C_{gs}+C_{gd}. The latter can be tuned from the back gate [9], increasing ΔV_{GS} from 13 mV to 28 mV for the n-MOSFET, and from 42 mV to 55 mV for the p-MOSFET, as the charge moves away from the top gate-oxide interface. The larger ΔV_{GS} of the p-MOSFET is due to the smaller hole effective mass and the additional heterojunction barriers in the valence band along the x-direction which are caused by the larger Ge mole fraction in the source/drain regions compared to the 25% Ge in the channel [10]. A larger ΔV_{GS} is desirable to achieve better noise immunity and larger f_{Rabi} when applying the spin control mm-wave signal on the qubit gate. It improves qubit fidelity at higher temperatures and allows for faster quantum processors. Fig. 5 compares the measured and simulated I_{DS} vs. V_{GS} characteristics of the n- and p-MOSFET QDs assuming ballistic transport and the NEGF formulation [11]. The best fit conduction and valence band profiles are shown in the insets with 20nm thick, 6meV and 40meV barriers, respectively. The effective masses were chosen for best fit but are approximately equal to the 0.19m_0 transverse electron mass in Si and within the 0.043m_0 to 0.15m_0 light-hole mass range in SiGe at 4.2 K [12]. The measured transfer characteristics (with V_{G1}=V_{G2}) of the n- and p- coupled double-QD devices are reproduced in Fig. 6, demonstrating tunneling through three barriers and two wells where the p-type device again shows stronger peaks. The V_{G1}=V_{G2} location of the tunneling peaks in the electron and hole-spin double-QD devices remains practically constant for $|V_{DS}|$ < 5 mV. This V_{DS} range is large enough for high-fidelity spin-readout circuit design and operation.

IV. First Monolithic Qubit ICs

A possible implementation of a low power (< 1 W) monolithic quantum processor with over 100 qubits and operation at 2 K or above is sketched in Fig. 7. The electron and/or hole spins are manipulated according to a well-established electric-field spin-resonance scheme [13-14], in dc magnetic fields of 2-6 T, using pulsed and FMCW (for spin-initialization) mm-wave signals in the 60-160 GHz range, applied to the QD gates. Short $\pi/2$ pulses on the order of 20 ps and Rabi frequencies (linearly dependent on the amplitude of the mm-wave signal applied on the qubit gate), as high as 12.5 GHz could be accommodated. Readout is based on the spin-filter (blockade) concept and spin-to-charge conversion, followed by transimpedance amplification. All the circuit building blocks, including a dc-110 GHz amplifier with 100 mW power consumption, suitable for distributing the mm-wave spin manipulation signals to over 100 qubits, have been designed and fabricated in the same 22nm FDSOI technology [9,15]. The main challenge, addressed in this paper, is the design of the readout TIA, whose schematic is shown in Fig. 8, with sufficient gain, bandwidth, and 50Ω output impedance, such that it does not overload the ~60aF output capacitance of the double-QD qubit. Ideally, the ~1nA tunneling peaks in Figs. 4-6 require at least 140 dBΩ of transimpedance gain for the readout TIA output to reach 10 mV of amplitude in a 50Ω load. Part of this gain needs to be implemented off chip to avoid oscillation. The monolithic qubit with TIA in Fig. 8 was optimized for 80dBΩ gain at 2 K, as shown in the

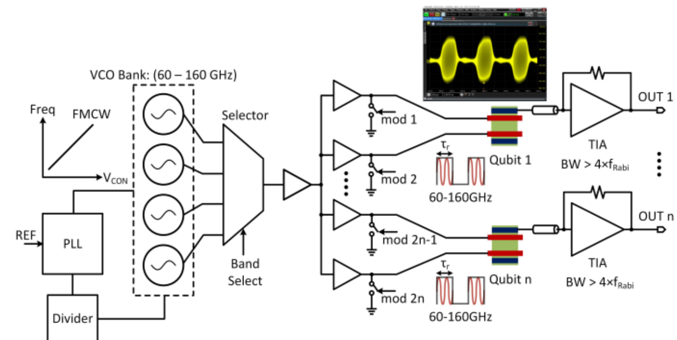

Fig. 7. Proposed monolithic quantum processor.

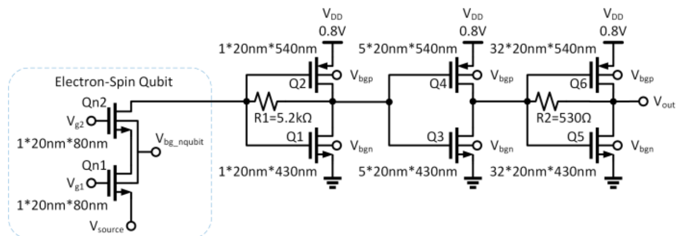

Fig. 8. Schematics of the electron-spin qubit with TIA circuit.

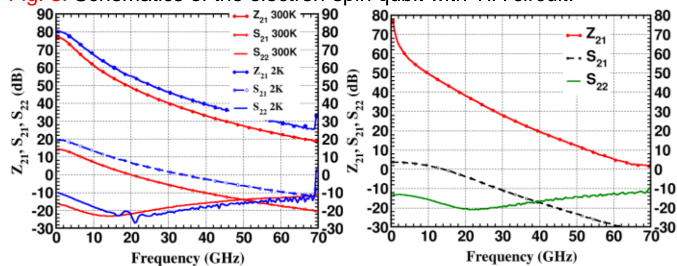

Fig. 9. Measured RF performance for (a) TIA at 300 K and 2 K and (b) n-qubit with TIA readout at 300 K.

measurements of Fig. 9(a). These results and cryogenic measurements of transistors, polysilicon resistors, and MOM capacitors demonstrate that all the components of the production 22nm FDSOI technology operate with even better performance at 2 K than at 300 K, and that monolithic integration of quantum dot qubits and readout circuitry is possible at 2 K. It can be seen in Fig. 9 that the S_{22} of the TIA and qubit-with-TIA remains better than -10 dB up to 70 GHz both at 300 K and 2 K.

V. Conclusion

This paper demonstrates that monolithic integration of qubits and high-fidelity readout circuitry is possible at 2 K in production 22nm FDSOI CMOS technology. Higher temperature operation will be possible if the transistor minimum feature size continues to be scaled. The p-type SiGe quantum dot qubits exhibit a ΔV_{GS} of 55 mV, twice larger than that of the n-type Si qubits, indicating higher energy level separation. A large ΔV_{GS} simplifies spin control electronics and is desirable for high-fidelity, high-f_{Rabi} quantum processors suitable for higher temperature operation.

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