From 1 Tbs per Carrier to 1 THz

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European Microwave Conference
Outline

- Introduction
- Examples of Tbs Wireless and Photonics Systems
- Segmented Power DAC Architectures
- Conclusions
We are addicted ...
What’s in a cloud?

- wireless links
- optical fiber links
- data centers
Why 100+Gb/s wireless?

- Near field communications

- Short-range reconfigurable wireless data transmission in the data center

- Board-to-board
Need >10x improvement in efficiency, bandwidth

Need digital techniques at over 100 Gbaud

Need centre frequencies above 200 GHz
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State-of-the-Art mm-Wave Radio/Fiberoptics TX

- Versatile
- Transparent to modulation scheme
- Linear
- Inefficient!

M. Nagatani
240-GHz, 1.1km Wireless Link

240 GHz IQ Rx/Tx MMIC
35 nm GaAs mHEMT

12 GBd QPSK
EVM 22.7%

35 Gbit/s BPSK BER < 6×10^-8

Courtesy of Ingmar Kalfass, Universität Stuttgart
100 Gb/s with Optical Tx & Electronic Rx

Photonic mm-wave heterodyne transmitter

Wireless transmission at 237.5 GHz over 20 m

Electronic mm-wave receiver with active MMIC

König et.al. OFC2013

Courtesy of Ingmar Kalfass, Universität Stuttgart
Trends in Optical Communications

Courtesy of Koichi Murata, NTT

60Gs/sec InP DACs
How Can We Get to 1 Tb/s per Carrier?

- **Fiber:** Dual-polarization, 16-QAM at 125 Gbaud
  - 8 data lanes at 125 Gb/s
  - Need phase equalization in receiver
  - Need 8 bit 125-GS/sec DACs
  - Need OSNR > 20 dB, optical amplifiers

- **Wireless:** 256-QAM at 125 Gbaud
  - 8 data lanes at 125 Gb/s
  - Need amplitude and phase equalization in receiver
  - Need 12 bit 125-GS/sec DACs
  - Need SNR > 26 dB
Doubling DAC, ADC sampling rate by mixing

2x64 GS/sec = 128 GS/sec

Ciena, CSICS 2013
Flexible Coherent Fiberoptic Transceiver

16-QAM 4x128 Gbaud = 1.024 Tb/s
THz ICs for Optical WDM Recovery in the Electrical Domain

**Bandwidth of optical fiber:** ~5 THz  \hspace{1cm} **Bandwidth of modern ICs:** ~800GHz

*With THz transistors, and with optical single-sideband mixing, one electrical IC can receive 1.6 THz of optical spectrum: 64 WDM channels*

*H-C Park et al (UCSB), ECOC 2013, Sept. 23-27*

**WDM receiver using THz ICs:**
*after optical mixing, optical WDM channels become DC-800 GHz subcarriers*

**Courtesy of Mark Rodwell, UCSB**

Sorin Voinigescu, October 7, 2013
Silicon active components

- III-V Laser
- Ge photodiodes > 100 GHz bandwidth
  - Vertical structure
- Modulators <80 Gb/s
  - Lateral structure

[D. Thompson et al. IEEE Ph.Letts, 2012]
[X. Wu et al., ISSCC 2013]
Electronics-photonics Integration

- Monolithic
  - Back-end of bulk CMOS
  - SOI CMOS
  - SiGe SOI-BiCMOS
- Heterogeneous
- Photonic/electric interposer
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Direct Digital Modulation Transmitters

\[ I-DATA \rightarrow \text{LPF} \rightarrow \sin(\omega_{LO}t) \rightarrow \cos(\omega_{LO}t) \rightarrow \text{PA} \rightarrow f \]

\[ Q-DATA \rightarrow \text{LPF} \rightarrow \sin(\omega_{LO}t) \rightarrow \cos(\omega_{LO}t) \rightarrow \text{PA} \rightarrow f \]

5-50 GS/s \( a_k \) N bits \rightarrow Power DAC \rightarrow \cos(\omega_{LO}t) \rightarrow 64QAM 56 GS/s

300 GHz \( f_{LO} = f_{RF} \) \rightarrow \text{PA} \rightarrow \sin(\omega_{LO}t) \rightarrow 5-50 GS/s \( b_k \) N bits \rightarrow Power DAC
Segmented Power DAC Architectures

- Tuned (<100GHz BW) mm-wave wireless
  - Coarse segmentation at antenna level
  - Fine bits in each antenna element
  - Free-space power combining
  - 50 Gbaud

- Broadband (DC to >100 GHz) fiber
  - Course segmentation at DA cell
  - Fine segmentation in DA cell
  - T-line power combiner
  - 50-110 Gbaud
Segmented Power DAC Architectures (ii)

- Optical
  - Coarse segmentation at modulator electrode level
  - Fine bits in driver element
  - Optical waveguide power combining
  - 5-50 Gbaud

[X. Wu et al., ISSCC 2013]
Broadband Power DAC

Distributed Segmentation: 7 MSBs and 7 LSBs in 8:1 size ratio

- Applications as m-PAM optical modulator driver
- Gb/s radio testing (DC to 60 GHz)

[A. Balteanu et al. IMS 2012]
Distributed DAC Cell

```
LSB_p  LSB_n
  |     |  2mA
  V     |  4mA
  |    60pH
  |  100pH
  |  2mA
  |    8pH
  V  8mA
  V  16mA
  V  28mA
  V  58pH
  V  In_p, In_n
  |    56pH
  |  2mA
  |  4mA
  |  4mA
  |  8mA
  |  16mA
  |  22mA
  |  12mA
  |  21mA
  | EF+ Buffer
  |  7mA
  |  2mA
  |  60pH
  |  100pH
  |  8pH
  |  8pH
  V  Out_p, Out_n
  V  MSB_p, MSB_n

Q5  628 Ω
Q6  4.2 V

Data_n  Q1
       Q2
       Q3
       Q4
Data_p
Clk_p
M1
M2
M3
V_tail

V_bias_gate  500 fF

500 fF

BS30 μm

500 μm

5.1V
```

Sorin Voinigescu, October 7, 2013
Die Photo and Technology

ST 130-nm SiGe BiCMOS process
Measured $P_{out}$ over $2^{14}$ code words
Measured Staircase Response

44GHz

56GHz

60GHz
44-GHz Carrier: 1MSB switching @ 44 Gb/s
Can we quadruple data rate?

130nm SiGe BiCMOS

55nm SiGe BiCMOS
Next Gen: Spar and large signal simulation
108-GHz Clock Quasi-ECL 1.8V Logic
[Y. Fu CSICS 2013]

Data in
Rx Equalizer

Flip-flop

Output driver

Data out

Clock in
Clock buffer

New 1.8V Quasi-CML Family
BiCMOS9MW
1.8V MOS-HBT Quasi-ECL

Sorin Voinigescu, October 7, 2013
108-GHz, 1.8V Lumped Clock-Path

S21 (dB)

Frequency (GHz)
75-Gb/s retimed equalization of a 3-m long cable
Retimed Cable Equalization Demos

40 Gb/s retimed with 40-GHz clock  36 Gb/s retimed with 108-GHz clock
Scaling to 55nm BiCMOS55

- 8x lower power consumption
- higher speed
- 36 fJ/bit

Sorin Voinigescu, October 7, 2013
120-Gb/s 4:2 MUX Retimed Lane Simulation
- Array element
  - Merged DAC with PA
  - Saturated PA
  - 2 bits: for OOK and BPSK modulation at up to 44 GBaud
  - Optional bits in each element
- Adaptable QPSK/m-ary QAM
- Max. PAE at each constellation point
- No back-off needed for linearity
Two solutions for 94-GHz Power DAC

a) 94-GHz 9-bit Stacked Gilbert Cell (S. Shopov, ESSCIRC 2013)
   • >15-Gb/s BPSK modulation performed in last stage
   • >15-Gb/s ASK modulation performed in last stage

b) 94-GHz 2-bit n-MOS-Stack PA (A. Balteanu, CSICS-2013)
   • >44-Gb/s BPSK modulation performed in mixer
   • >44-Gb/s OOK modulation performed in last stage
40+ Gb/s inductively-peaked CMOS logic
94-GHz Gilbert-Cell Based IQ DAC

[S. Shopov et al. ESSCIRC 2013]
94-GHz 9-bit stacked Gilbert cell

\[ I_{DC} = 56.4 \text{ mA}, \quad R_{OPT,diff} = 100\Omega \]
S-par. measurements for all 255 code words
INL-DNL at 90 GHz from S-par. measurements

![Graph showing the comparison between ideal, simulated, and measured INL-DNL at 90 GHz. The graph plots normalized magnitude against digital word, with distinct quadrants highlighting the ideal, simulated, and measured data.]
Large signal $P_{out}$ vs. $P_{in}$ for different frequencies
MSB, 15-Gb/s PRBS ASK/BPSK Spectra
15-Gb/s PRBS OOK Spectra

Ch 1 Pt Avg = 500

Cont. CH 1: Output C° SrcPwrCal° Avg=500

>Ch1: PS Start 77.0000 GHz Stop 103.0000 GHz
94-GHz n-MOS-Stack PA with OOK Modulation

![Circuit Diagram]

![Graph: MAG and S_{21} (dB) vs Frequency (GHz)]
LO Amplifier S-parameters

- $S_{21}$ with BPSK = 0
- $S_{11}$ with BPSK = 0
- $S_{22}$ with BPSK = 0
- $S_{21}$ with BPSK = 1
- $S_{11}$ with BPSK = 1
- $S_{22}$ with BPSK = 1

Frequency (GHz)

$S_{21}$, $S_{11}$, $S_{22}$ (dB)
100/110 GHz: BPSK at 5/10/44Gb/s

b)

\[
P_{\text{out}} \text{ (dBm)}
\]

\[
\begin{align*}
85 & \quad 90 \quad 95 \quad 100 \quad 105 \quad 110 \\
\end{align*}
\]
Conclusions

- Power DAC transmitters with antenna/modulator segmentation
- Convergence of digital with THz techniques
  - 44-Gbaud (88G b/s) 2-bit Power-DAC at 100-110 GHz
  - 15-Gbaud (120 Gb/s) 19 dBm, 18-bit IQ Power DAC
  - 60GS/sec 6V_{pp} 6-bit Distributed Power DAC
- 200+ Gb/s radio at 240 GHz feasible in silicon
- 100-Gb/s electronics for 1Tbs/carrier fiberoptics
- Need progress in modulators and electronic-photonic integration
Credits

- Graduate students
  - Andreea Balteanu
  - Stefan Shopov
  - Yingying Fu
  - Ioannis Sarkas
  - Alex Tomkins
  - Eric Dacquay
  - Ivan Krotnev

- Funding
  - NSERC,
  - OCE,
  - Robert Bosch,
  - DARPA,
  - Ciena,
  - Gennum

- Chip donations
  - STMicroelectronics,
  - DARPA
  - Ciena
240-GHz SiGe HBT Radar Transceiver

Bredendiek et al, IMS 2013
300-GHz SiGe HBT VCO-Doubler Source

S. Voinigescu et al., JSSC 2013

Output Power (dBm)

-25  -20  -15  -10  -5   0
285  290  295  300  305  310  315  320  325

Frequency (GHz)

-60  -55  -50  -45  -40  -35  -30  -25  -20
285  290  295  300  305  310  315  320  325

Phase Noise (dBc/Hz @ 10 MHz)

-105  -100  -95  -90  -85  -80  -75  -70  -65
285  290  295  300  305  310  315  320  325

S. Voinigescu et al., JSSC 2013
InP HBT Integrated Circuits: 600 GHz & Beyond

614 GHz fundamental VCO

M. Seo, TSC / UCSB

340 GHz dynamic frequency divider

M. Seo, UCSB/TSC IMS 2010

585-600 GHz amplifier, > 34 dB gain, 2.8 dBm output

M. Seo, TSC IMS 2013

300 GHz fundamental PLL

M. Seo, TSC IMS 2011

204 GHz static frequency divider (ECL master-slave latch)

Z. Griffith, TSC CSIC 2010

220 GHz 180 mW power amplifier

T. Reed, UCSB Z. Griffith, Teledyne CSICS 2013

Integrated 300/350GHz Receivers: LNA/Mixer/VCO

M. Seo, TSC

600 GHz Integrated Transmitter PLL + Mixer

M. Seo, TSC

Integrated 300/350GHz Receivers: LNA/Mixer/VCO

M. Seo, TSC

600 GHz Integrated Transmitter PLL + Mixer

M. Seo, TSC

Courtesy of Mark Rodwell
220 GHz, 180mW Power Amplifier

Simulations:
320 mW output @ P1dB

Measurements to date:
180 mW @ 220 GHz

T. Reed, UCSB
Z. Griffith, Teledyne
Teledyne 256 nm InP HBT

A 180mW InP HBT Power Amplifier MMIC at 214 GHz
(To be presented, CSICS 2013)

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60-GS/s 6-bit broadband DAC in InP HBT

Technology: InP HBT
Sampling rate: 60 GS/s
Resolution: 6 bit
Analog bandwidth: > 30 GHz
INL/DNL: < 0.5 LSB
SFDR: ~ 30 dB up to 30 GHz
Power Cons.: 1.8 W

M. Nagatani et al. CSICS 2011

Measured Performance

DNL/INL

4-level signal output (for 16-QAM)

50 Gbaud (50 GS/s)
100 mV/div 5 ps/div

60 Gbaud (60 GS/s)
100 mV/div 5 ps/div

DNL: -0.13 / +0.43 LSB
INL: -0.19 / +0.31 LSB

Courtesy of Koichi Murata, NTT
Example: Binary-Weighted Optical DAC

[X. Wu et al, ISSCC 2013]
Optical 16-PAM Eye Diagram

Simulated eye for Enhanced binary code weighted PAM-16
100-GHz Ge PIN Photodiodes on SOI

LETI

40 Gbit/s
94-GHz BPSK Modulator