INVITED PAPER

Silicon Millimeter-Wave, Terahertz, and High-Speed Fiber-Optic Device and Benchmark Circuit Scaling Through the 2030 ITRS Horizon

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ABSTRACT | This paper reviews the technology requirements of future 100–300-GHz millimeter-wave (mm-wave) systems-on-chip (SOI) for high data rate wireless and sensor applications, as well as for 100–300-GBaud fiber-optic communication systems. Measurements of state-of-the-art silicon metal–oxide–semiconductor field-effect transistors (MOSFETs), SiGe heterojunction bipolar transistors (HBTs), and of a variety of HBT-HBT and MOS-HBT cascodes are presented from dc to 325 GHz. The challenges facing mm-wave MOSFET and SiGe HBT device and benchmark circuit scaling toward 2–3-nm gate length and beyond 2-THz transistor f_{MAX} are discussed for the first time based on technology computer-aided design (TCAD) and atomistic simulations. Finally, simulations of the scaling of the SiGe HBT analog and mixed-signal mm-wave benchmark circuit performance across future technology nodes predict that PAs with 45% power added efficiency (PAE) at 220 GHz, track and hold amplifiers (THAs) with over 140-GHz bandwidth, and transimpedance amplifiers (TIAs) with 250-GHz bandwidth and less than 5-dB noise figure will become feasible by 2030. Comparison of simulations and measurements for representative benchmark circuits such as TIAs, THAs, linear modulator drivers, digital-to-analog converters (DACs), and power amplifiers (PAs), fabricated in advanced SiGe BiCMOS and nanoscale SOI complementary metal–oxide–semiconductor (CMOS) technologies, and operating at 120 Gb/s and above 100 GHz, respectively, are presented to support the credibility of the benchmark circuit scaling exercise.

KEYWORDS | Analog-to-digital converter (ADC); benchmark circuit; digital-to-analog converter (DAC); driver; fiber-optic transceiver; fully depleted silicon-on-insulator (FD-SOI); metal–oxide–semiconductor field-effect transistor (MOSFET); millimeter wave (mm-wave); noise figure; PA; partially depleted silicon-on-insulator (PD-SOI); power added efficiency (PAE); radio transceiver; SiGe heterojunction bipolar transistor (HBT); silicon-on-insulator complementary metal–oxide–semiconductor (SOI-CMOS); track and hold amplifier (THA); transimpedance amplifier (TIA); ultrathin body and bulk (UTBB) FD-SOI; VCO

I. INTRODUCTION

During the past seven years we have witnessed the relatively widespread deployment of silicon millimeter-wave (mm-wave) circuits in 77-GHz automotive radar [1], the emergence of silicon mm-wave backhaul transceivers at 57–86 GHz [2], and the tentative introduction of the first consumer 60-GHz wireless high-definition multimedia interface (HDMI) systems [3] which have since found their way in smartphones [4]. Despite failing to meet the expectations of super-high volume, ultralow power, and ultralow cost that would have by now placed silicon 60-GHz transceivers and phased arrays in every smartphone and tablet, the industry appears to be now convinced of the feasibility and merits of silicon technologies at the upper mm-wave

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frequencies. So, what's next? What are the (new) applications? What are the technology requirements for would-be mm-wave products? What are the predictions of transistor and mm-wave benchmark circuit performance for the 2030 International Technology Roadmap for Semiconductors (ITRS) horizon?

Although fifth-generation (5G) networks are likely to operate below 30 GHz, the associated wireless or fiber-optic backhaul will require >100-Gb/s mm-wave integrated circuits (ICs), as illustrated in Fig. 1. The newly introduced silicon mm-wave cellular backhaul transceivers [2], [5] operate in the *V*-and *E*-bands, at data rates below 10 Gb/s. In the future, they may need to move to 140 and 220 GHz for increased bandwidths to accommodate the much higher data rates demanded by future 5G backhaul traffic. The ITRS 2015 radio-frequency and analog/mixed-signal (RF-AMS) tables now charter the predicted high-frequency performance of transistors and of the critical RF blocks at 140 and 220 GHz through 2030, for both silicon and III-V technologies.

Similarly, Internet of Things (IoT) data centers will spearhead the development of 400-Gb/s and 1-Tbs optical fiber links [6] which will also rely heavily on silicon mm-wave and high-speed ICs with bandwidths exceeding 70 GHz [7], and likely 150 GHz by 2030. The complex modulation schemes considered for these fiber-optic links, such as 16-quadrature amplitude modulation (16QAM) and discrete multitone (DMT), will demand 6–8-b mm-wave analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) [8] with aggregate sampling rates into the terahertz (THz) regime.

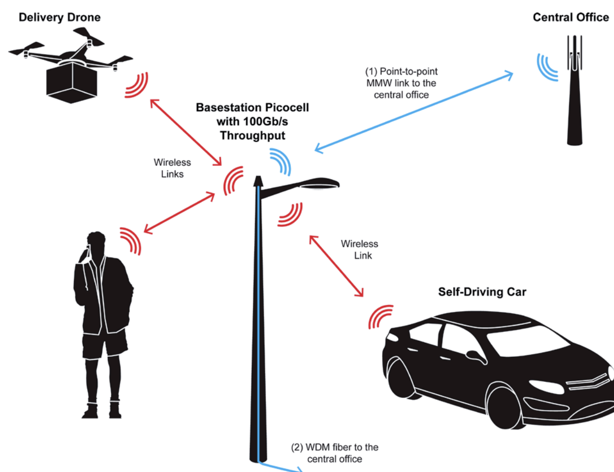


Fig. 1. ***Cartoon of a possible mm-wave backhaul scenario in 5G networks where a mm-wave link at >100 Gb/s will be required between picocells and the central office.***

Autonomous drones and robots, autonomous lawn mowers and snow blowers, as well as a variety of ultrasmall form factor wearable and IoT connected devices, which will require touchless gesture control [9], [10], will benefit from miniature *D*-band (110–170 GHz) [11], [12] and *J*-band (220–325 GHz) [13], [14] distance and velocity sensors with in-package antennas, such as the ones shown in Fig. 3 [11], [12]. High transistor transconductance and power gain

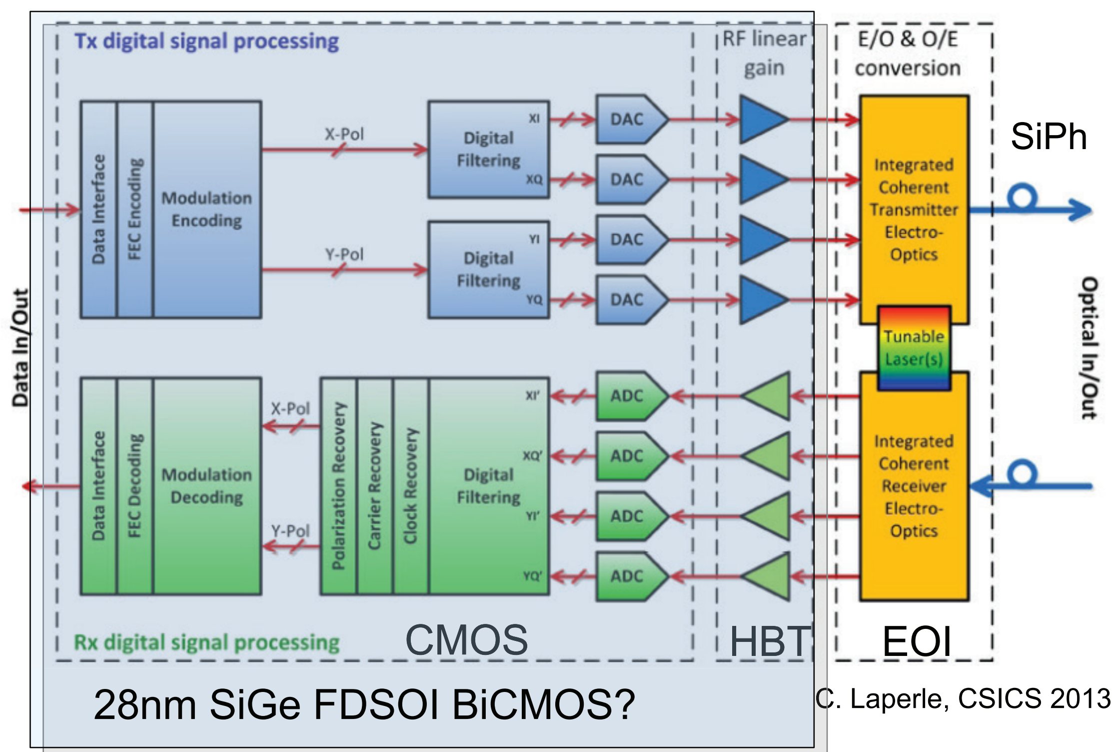


Fig. 2. ***Block diagram of 100/400/1000-Gb/s fiberoptic transceivers [8].***

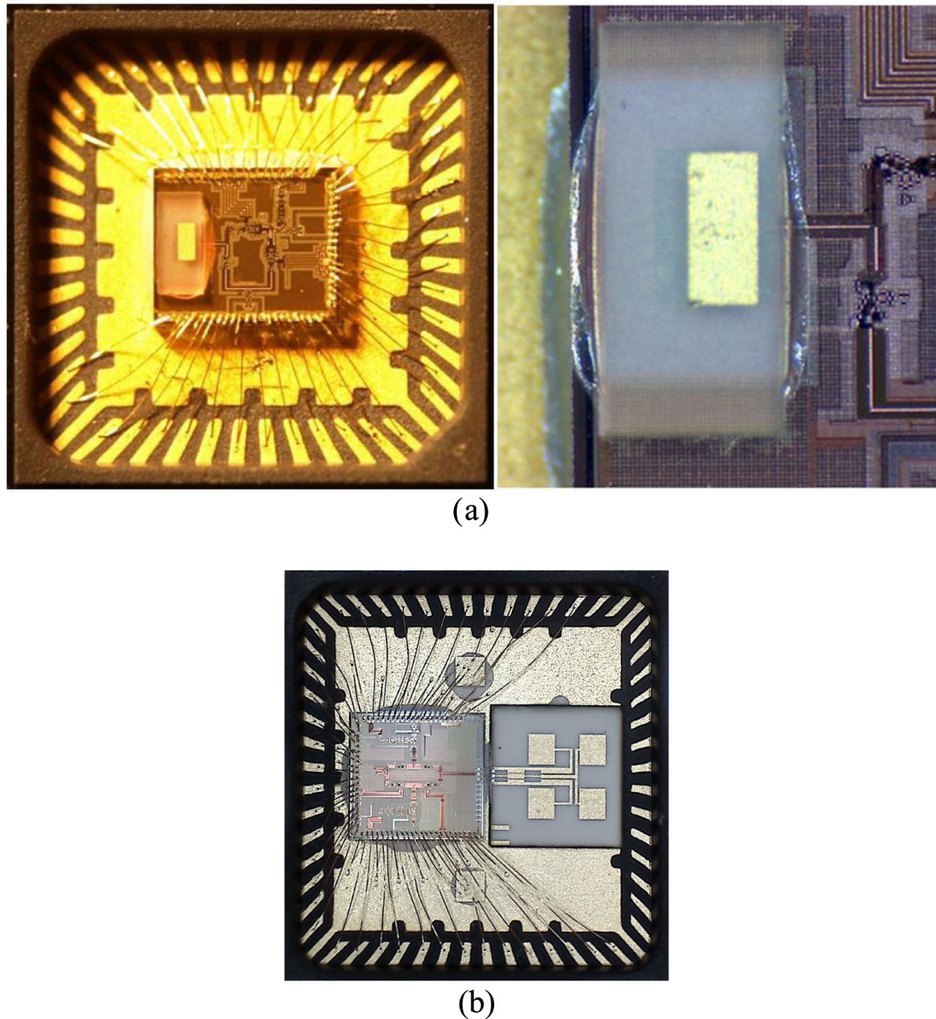


Fig. 3. *Photograph of (a) 120-GHz [11] and (b) 150-GHz [12] SiGe BiCMOS distance and velocity sensors copackaged with above die (a) and in-package ceramic antennas in a 7-mm × 7-mm QFN package (courtesy of Dr. J. Hasch of Robert Bosch GmbH).*

at low bias current, a strength of heterojunction bipolar transistors (HBTs), along with a technology back-end suitable for high-Q (>50) inductors and varactors, will be needed in ultralow power mm-wave sensors and tags connected to the IoT if the ever-increasing energy consumption of the IT sector is to be curbed.

This paper expands on the methodology of the HBT benchmark circuit scaling exercise introduced in [15] and [16], and augments it with new research on the scaling of the high-frequency performance of Si metal–oxide–semiconductor field-effect transistors (MOSFETs) down to 2-nm gate lengths, and on the scaling of SiGe HBT transimpedance amplifiers (TIAs) and track and hold amplifiers (THAs), to provide a global comparative view of the expected evolution of Si complementary metal–oxide–semiconductor (CMOS) and bipolar transistor mm-wave and broadband analog/mixed-signal circuits in future technology nodes. It is organized as follows. Section II discusses the measured high-frequency performance of transistors and cascode topologies in state-of-the-art 55-nm SiGe BiCMOS and 28-nm ultrathin body and bulk (UTBB) fully depleted silicon-on-insulator (FD-SOI) CMOS technologies up to 325 GHz. For the first time, technology computer-aided design (TCAD)- and atomistic-based predictions for the scaling of the transconductance g_m and cutoff frequency f_T of silicon MOSFETs down to 2–3-nm gate lengths is presented in Section III. The architecture of current and future mm-wave radio, sensor, and fiber-optic transceivers is reviewed in Section IV and the critical analog/mixed-signal SiGe HBT and CMOS circuit building blocks are identified and their high-frequency figures of merit are simulated in future technology nodes in Section V.

II. SILICON TECHNOLOGY PERFORMANCE

As transistor dimensions have shrunk, they have continued to become faster and to generate less noise, favoring larger

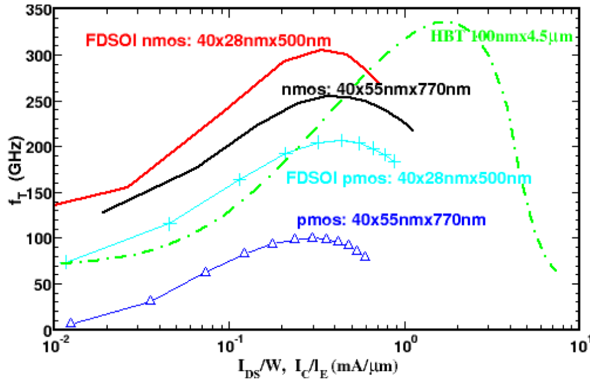


Fig. 4. ***Measured f_T of 55-nm SiGe BiCMOS (HBT, 55-nm p-MOSFET, 55-nm n-MOSFET) and 28-nm UTBB FD-SOI CMOS [15].***

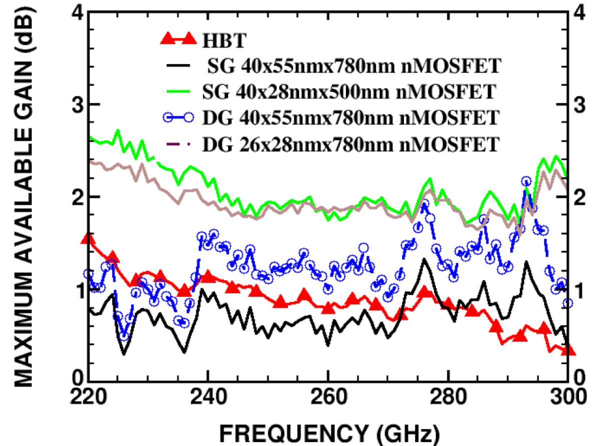


Fig. 6. ***Measured MAG of state-of-the-art SiGe HBTs, single-gate and double-side gate contact 55-nm bulk and 28-nm UTBB FD-SOI MOSFETs [15].***

bandwidth applications for the same or slightly reduced dynamic range. This has been possible because transistor breakdown and supply voltages have decreased only slightly in recent technology nodes. However, source and gate or base and emitter resistances have been difficult to scale and mobility enhancement techniques based on strain engineering and SiGe channels have already run most of their course. Moreover, unlike most other RF and high-speed blocks which have benefited from silicon transistor scaling, RF power amplifier performance, especially in CMOS, has saturated and somewhat been diminished in advanced nodes due to the reduced safe operating voltage range. Voltage-controlled oscillator (VCO) phase noise has also been degraded in deeply scaled MOSFETs due to the reduced voltage swing and high 1/f noise corner.

Measurements of f_T, maximum frequency of oscillation f_{MAX}, and maximum available power gain (MAG) of fully wired (up to the top metal) state-of-the-art 55-nm SiGe BiCMOS [17] and 28-nm UTBB FD-SOI [18] transistors were conducted in the direct current (dc) 325-GHz range and are reproduced in Figs. 4–6. Although f_T and f_{MAX} of both SiGe HBTs and 28-nm n-MOSFETs simultaneously exceed 300 GHz, MAG is lower than 10 dB above 110 GHz and is comparable to that of 55-nm n-MOSFETs. As the physical gate length is shrunk, the f_T and f_{MAX} improvement in fully wired n-MOSFETs is not proportional to the gate length ratio, as constant-field scaling rules for the intrinsic FET predict. Moreover, unless a cascode stage is used, the MAG of state-of-the-art silicon transistors is inadequate for efficient power amplifiers beyond 100 GHz. Nevertheless, as illustrated in Fig. 7, the measured MAG of SiGe-HBT cascodes and of double-gate contact 55-nm MOSFET-HBT cascodes is larger than 10 dB up to 240 GHz. It is therefore not surprising that most SiGe HBT amplifiers reported to date, and which operate above 200 GHz, employ several SiGe-HBT cascode stages [19]. The authors are not aware of published CMOS power amplifiers operating above 200 GHz. The latter topic will be revisited in Section V.

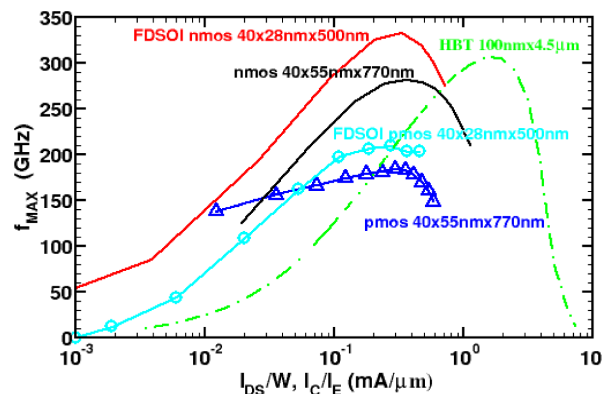


Fig. 5. ***Measured f_{MAX} of 55-nm SiGe BiCMOS (HBT, 55-nm p-MOSFET, 55-nm n-MOSFET) and 28-nm UTBB FD-SOI CMOS [15].***

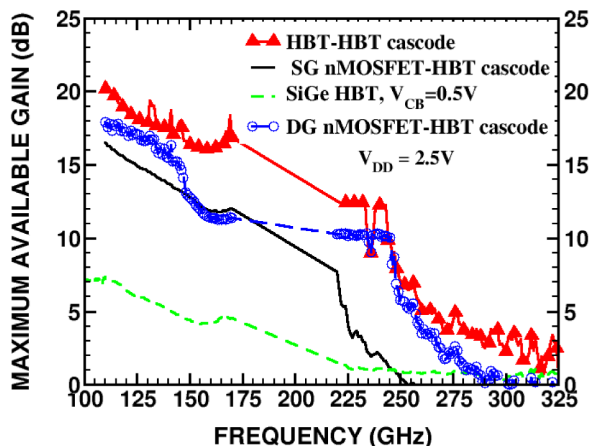


Fig. 7. ***Measured MAG of HBT-HBT and single-gate and double-gate contact MOS-HBT cascodes [15].***

III. HIGH-FREQUENCY PERFORMANCE SCALING OF SILICON TECHNOLOGY

Can MOSFET scaling continue through 2030? Although the exact high-frequency performance of scaled MOSFETs in future technology is difficult to predict using industry state-of-the-art TCAD simulators such as Sentaurus, or even with commercial atomistic simulators such as Atomistix Toolkit where the transistor structure is built atom by atom and simulated using first principles without making assumptions about material transport properties or bandgap, it is possible to determine the ultimate limits of scaling beyond which short channel effects and tunneling seriously impede the transistor action.

Extensive TCAD (using Sentaurus) and atomistic (using Atomistix Toolkit) simulations of 20-, 14-, 10-, 7-, 5-, and 2-nm gate length silicon double-gate MOSFETs (essentially ideal FinFET structures with tall fins) with ideal high-*k* gate dielectric stack, were conducted. Gate-drain and gate-source fringing capacitances, and source and drain contact resistances were added to realistically capture the impact of layout parasitics on the high-frequency performance of the scaled MOSFETs. With the exception of the 2-nm device, all simulated structures follow the material composition, layer dimensions, and contact resistances tabulated in the 2015 ITRS tables. The device with 20-nm physical gate length corresponds to the present 14-nm FinFET node where the physical gate length is approximately 20 nm. Cross sections of the 5- and 2-nm structures are included as inserts in Fig. 8. The n-MOSFET with 5-nm physical gate length has a silicon channel thickness of 1.8 nm and a 2.1-nm-thick gate dielectric stack with an effective relative permittivity of 25. It is expected to enter production in 2030. The 2-nm-long n-MOSFET structure is beyond the current ITRS horizon, and features more aggressively scaled channel thickness and an ideal gate dielectric stack of 1.2 nm (6 Si atoms thick) and 0.5 nm, respectively, in order to suppress short channel effects. To avoid tunneling through the oxide, the ideal 0.5-nm-thick dielectric stack with $\varepsilon_r = 25$ could be realized as a 2-nm-thick physical oxide stack with a relative permittivity of 100. The simulated transfer characteristics shown in Fig. 8 clearly indicate that, despite some subthreshold-slope degradation not captured by the classical TCAD simulator, short channel effects can be controlled even in a double-gate structure with 2-nm physical gate length. Assuming that manufacturing solutions and new high-*k*, large bandgap gate dielectrics are found, such structures will be needed to meet the ITRS milestones beyond 2030. However, as shown in Fig. 9, parasitic source and drain resistance, fringing capacitance, and especially surface scattering [20] pose more urgent barriers to overcome as the physical gate length is reduced below 10 nm. For more reliable predictions, the model in [20] must be validated and calibrated on new sets of mobility measurements of structures with silicon layer thicknesses in the 1–3-nm range. Moreover, atomistic simulations of nanowire MOSFETs predict that, even without surface scattering, the bandgap increase in a silicon nanowire only 3–4 atoms in cross section and the smaller number of free electrons than in a thin silicon fin or sheet, result in a significant degradation of I_{ON}, transconductance, and cutoff frequency. The f_{MAX} has been left out of these predictive simulations because of its strong dependence on gate resistance, layout geometry, and layout parasitics, all of which vary strongly with manufacturing solutions. The latter are too speculative to be predicted today. It should be noted that the TCAD simulator used to generate the g_m and f_T scaling data in Fig. 9 was calibrated by simulating a realistic 28-nm UTBB FD-SOI n-channel MOSFET structure with 24-nm physical gate length, and ensuring that the simulated g_m and f_T match measurements, including those in Figs. 4–7.

It is instructive to compare the high-frequency performance scaling simulations for MOSFETs with those for SiGe HBTs published in [16]. The latter also include f_{MAX} and the minimum noise figure scaling, and cover today's generation of SiGe HBTs with f_T / f_{MAX} = 300/400 GHz and four future technology nodes beyond 2030, when f_T and f_{MAX} are predicted to reach 780 GHz and 2 THz, respectively.

Table 1 compares the n-MOSFET and SiGe HBT high-frequency performance scaling. Because of its coarser lithography (Node 5 features a minimum emitter width of 20 nm) SiGe HBT scaling and manufacturing solutions are easier to predict based on current production 28- and 14-nm CMOS technology. Also, unlike CMOS whose high-frequency performance appears to saturate at an f_T of about 600 GHz and then degrade with further scaling, the high-frequency performance of both SiGe HBTs and InP HBTs continues to improve proportionally to the scaling factor. InP HBT technologies with performance similar to that of the SiGe HBT in Node 2, i.e., with both f_T

Table 1: Comparison of n-MOSFET and SiGe HBT Minimum Physical Feature Size and High-Frequency Performance Scaling

Parameter	Node 1	Node 2	Node 3	Node 4	Node 5
L_G (MOSFET)	20 nm	14 nm	10 nm	7nm	5 nm
W_E (HBT)	115 nm	88 nm	66 nm	44 nm	22 nm
f_T (n-MOS)	334 GHz	436 GHz	609 GHz	423 GHz	210 GHz
f_T (HBT)	282 GHz	395 GHz	502 GHz	642 GHz	778 GHz
f_{MAX} (HBT)	432 GHz	543 GHz	766 GHz	1191 GHz	1985 GHz

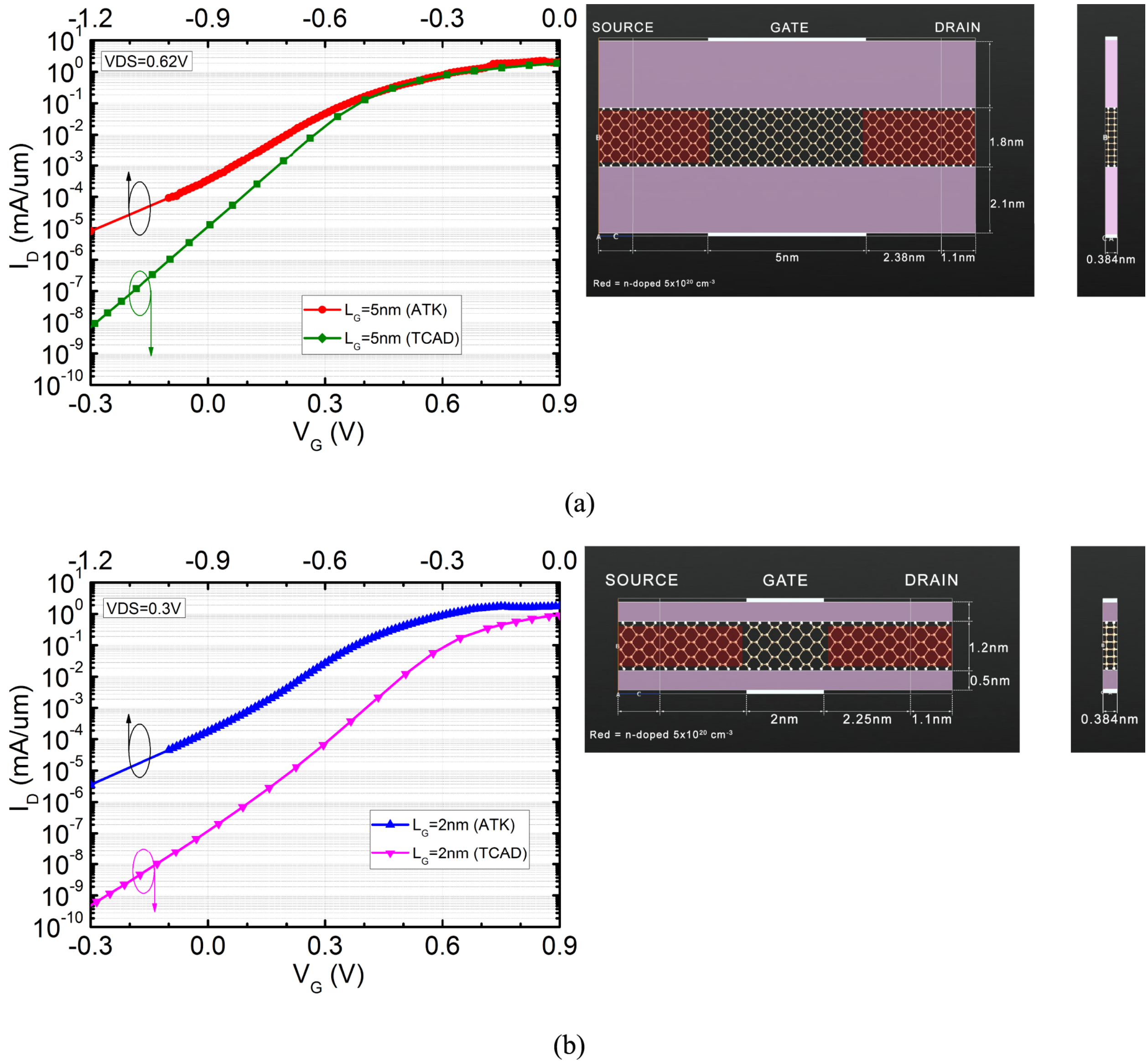


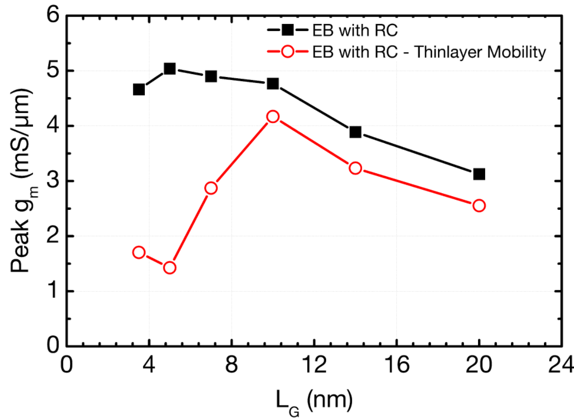
Fig. 8. *Sentaurus (TCAD) versus atomistic (ATK) simulations of the I-V transfer characteristics in the saturation region of (a) 5-nm-long and (b) 2-nm-long double-gate Si MOSFETs with ideal gate dielectric and ideal (scatter-free) channel oxide interface.*

and f_{MAX} larger than 450 GHz, are already prototyping in small volumes at foundries on at least two continents. In general, for similar breakdown voltage, lithography, and vertical structure dimensions, InP HBT performance continues to be one or two technology nodes ahead of SiGe HBT performance, while practically identical circuit topologies can be used to manufacture all benchmark circuits discussed in Section V.

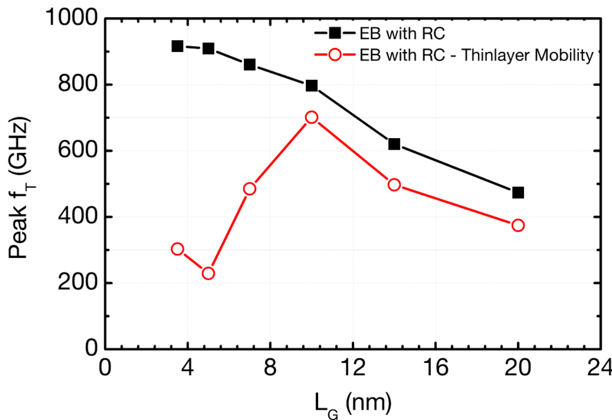
IV. MILLIMETER-WAVE TRANSCEIVER ARCHITECTURES AND BUILDING BLOCKS

Some of the most important goals of the roadmapping exercise are as follows: 1) to identify existing and potential applications that will drive future technology development; 2) to single out representative circuit benchmarks for each of those applications; and 3) to analyze and chart the evolution of their figures of merit (FoMs) across technology nodes. As discussed in the Introduction, among the important applications that will drive mm-wave technology development in the next 15–20 years are mm-wave sensing, mm-wave radio, and fiber-optic systems at 1 Tb/s per carrier and beyond. A variety of commercial silicon mm-wave circuits are used in all of these applications today. They operate in the 30–100-GHz range, and are expected to approach 300 GHz in the future.

Fig. 10 shows the block diagram of a fundamental-frequency multichannel Doppler transceiver architecture that



(a)



(b)

Fig. 9. ***Impact of RC parasitics and surface scattering on (a) transconductance and (b) f_T scaling in idealized double-gate Si MOSFET structures as captured using energy-balance Sentaurus simulations with the surface scattering mobility model from [20]. EB stands for energy balance simulations and RC indicates that resistive and capacitive layout parasitics are included up to and including metal 1.***

is currently used in a variety of distance and velocity sensors for autonomous navigation and industrial sensing at 60 and 77 GHz [1], and which has also been proposed for touchless gesture control [10]. Critical building blocks are the tuned PA, VCO, divider chain, and receive mixers which also act as low-noise amplifiers (LNAs). This architecture and building blocks are expected to be scalable to higher frequencies, likely up to 220 GHz, with improved performance, in future SiGe BiCMOS and CMOS technology nodes. Higher frequency of operation results in lower power consumption in the receive mixers and VCO, and in improved sensor resolution. Power consumption will be the main driver for such systems. If they are to be inserted into wearable devices, power consumption will have to come down by at least a factor of 20 from the current systems which consume over 0.5 W [1], [3], [10]–[14].

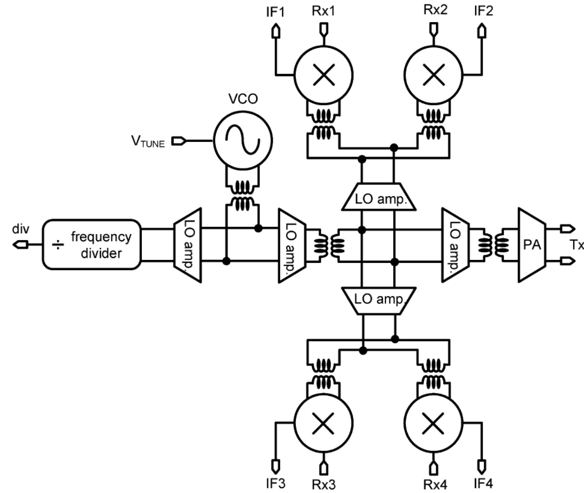


Fig. 10. ***Multichannel Doppler transceiver architecture used for distance, velocity, and touchless gesture control sensors.***

Similarly, Fig. 11 illustrates two transmitter architectures employed in high data rate mm-wave radio transmitters at 60 GHz and above. Here, too, we can identify the VCO and divider chain (not shown), the linear PA, or an RF power DAC, and the linear up-conversion mixer as the critical building blocks whose performance needs to be chartered in future technology nodes.

Finally, Fig. 12 shows several ultrabroadband analog front-end architectures for fiber-optic receivers and transmitters, and for instrumentation ADCs used in real-time oscilloscopes [21]. Fig. 12(a) describes the block diagram of

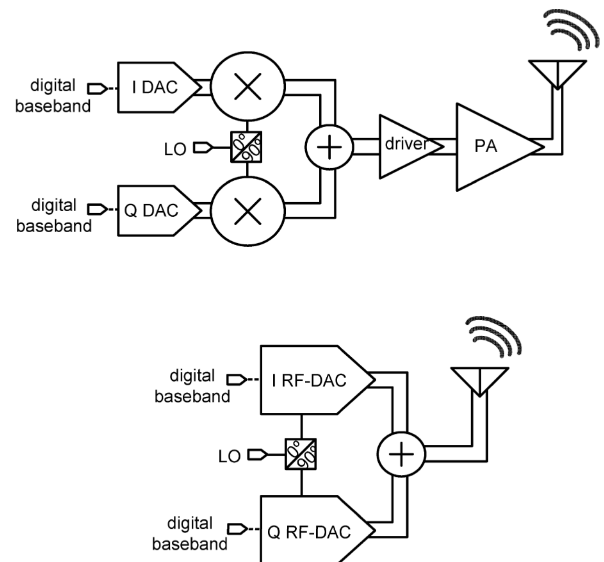


Fig. 11. ***Traditional linear radio transmitter architecture with linear up-converter and linear power amplifier (top) and fully digital RF power DAC radio transmitter architecture (bottom).***

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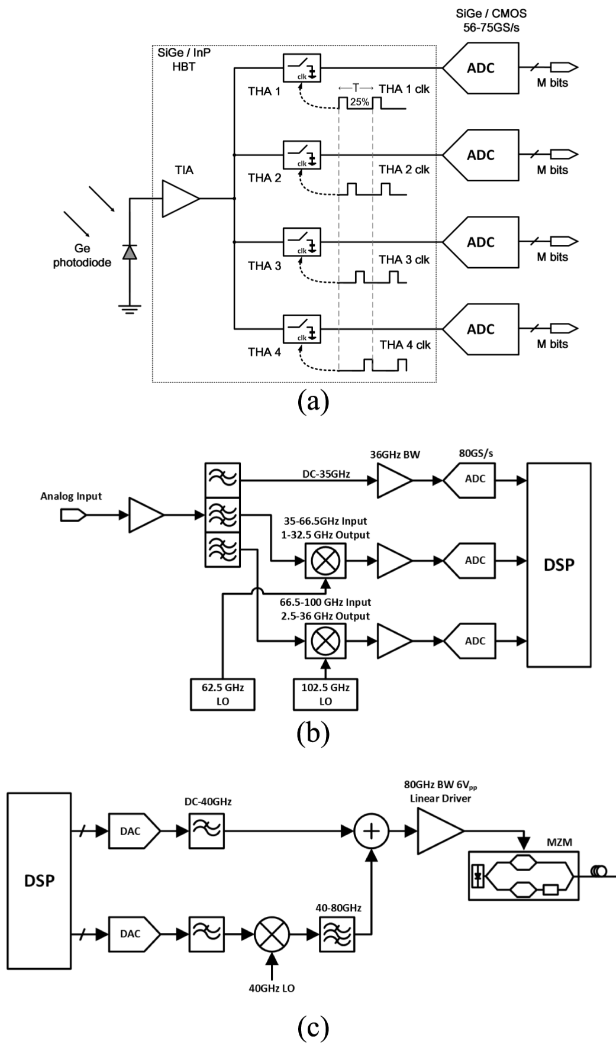


Fig. 12. ***(a) Time-interleaved and (b) frequency-interleaved fiber-optic ADC receiver analog front-ends (inspired by [21]) and (c) frequency-interleaved fiber-optic transmitter [24].***

a possible 128-GBaud fiber-optic receiver that consists of a photodiode, a 90-GHz bandwidth TIA, which in modern systems with QAM and DMT modulation is a very broadband, linear LNA and the >220-GS/s ADC front-end. The latter employs a time-interleaved architecture with four THAs, sampled with nonoverlapping clock signals. Time interleaving along with the THAs allow for the sampling frequency and bandwidth of the receiver to be increased four times compared to the bandwidth of the 56–75-GS/s sub-ADCs. The latter are typically manufactured in the most advanced CMOS nodes [22]. Their bandwidth will be difficult, though apparently possible, to increase in future CMOS nodes [23]. In this architecture, both the TIA and the THA are critical broadband building blocks whose performance needs to be improved and chartered in future technology nodes.

An alternative broadband electronic receiver architecture based on frequency interleaving (also known as mixing) is shown in Fig. 12(b) [21], while the corresponding fiber-optic transmitter architecture is depicted in Fig. 12(c) [24]. In both cases, linear broadband amplifiers are needed, with low noise in the receiver and large output swing in the transmitter. The output amplifier in the transmitter is the broadband equivalent of the linear PA in a tuned radio transceiver and typically requires > $3\,V_{pp}$ output swing per side in order to properly drive an optical modulator.

V. BENCHMARK CIRCUITS

The benchmark circuits identified earlier can be classified as follows: 1) high-speed digital; 2) tuned, used in wireless data transmission, radar, sensing, and imaging systems; and 3) broadband, used in telecom, datacomm, and computercomm systems. The FoM is typically chosen for each type of circuit in order to capture a combination of important performance parameters in a single number. The FoM allows for a quick and simple way to judge and compare different designs of the same benchmark circuit at different frequencies and in different technologies, without stifling design freedom and creativity. More importantly for device technology developers, the FoMs can be linked to certain transistor high-frequency and noise parameters and thus can provide valuable guidance on those features of the technology that need to improve in future nodes and on the target values to be set for them. To the latter end, the benchmark circuits should be simple, preferably single transistor, and should use ideal passive components to unambiguously link circuit performance to transistor performance.

The FoMs of the benchmark circuits are typically defined in such a way so that the highest FoM value marks the best performance. For example, in a tuned LNA, we want to maximize gain and linearity and to minimize noise figure at a given frequency. High gain and low noise become increasingly difficult to achieve at higher frequencies. Therefore, frequency has to somehow factor in the FoM

$$\mathrm{FoM_{LNA}} = \frac{G \cdot \mathrm{IIP3} \cdot f}{(F-1)\cdot P}. \tag{1}$$

Here G is the power gain, IIP3 [W] is the input third-order intercept point, f [Hz] is the frequency, F is the noise factor, and P [W] is the dc power consumed by the LNA.

How does $\mathrm{FoM_{LNA}}$ relate to the transistor high-frequency figures of merit? Knowing that the output third-order intercept point $\mathrm{OIP3} = G \cdot \mathrm{IIP3} <= P$, assuming that the LNA is optimally designed for linearity, and that $G < \mathrm{MAG}$, for a single-stage LNA the ceiling for $\mathrm{FoM_{LNA}}$ can be linked to the transistor $F_{\mathrm{MIN}} - 1$ at the center frequency of the LNA

$$\mathrm{FoM_{LNA}} = \frac{f}{(F_{\mathrm{MIN}}-1)}. \tag{2}$$

Similarly, for a VCO, several FoMs can be defined as

$$\mathrm{FoM_{VCO}} = \left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}\cdot P} \tag{3}$$

$$\mathrm{FoM}_{VCO-T} = \left(\frac{f_0}{\Delta f}\right)^2 \frac{P_{\mathrm{out}} \cdot \mathrm{FTR}}{L\{\Delta f\} \cdot P} = \left(\frac{f_0}{\Delta f}\right)^2 \frac{\eta \cdot \mathrm{FTR}}{L\{\Delta f\}} \quad (4)$$

where P_{out} [W] is the VCO output power, L is the phase noise in a 1-Hz band at offset frequency Δf, $\eta = P_{\mathrm{out}}/P$ is the VCO efficiency, and $\mathrm{FTR} = (F_{\max} - F_{\min})/(F_{\max} + F_{\min})$ is the normalized frequency tuning range of the VCO.

For a single common-emitter or common-source class A or class AB PA, the FoM is given by

$$\mathrm{FoM}_{\mathrm{PA}} = P_{\mathrm{out}} \cdot G \cdot \mathrm{PAE} \cdot f^2 \quad (5)$$

where PAE is the power added efficiency. Again, this figure of merit can be tied to the transistor performance. For example, by assuming that the gain of the PA approaches that of the transistor with $G(f) = \min\{\mathrm{MSG}\ (f), f_{\mathrm{MAX}}^2/f^2\}$ and assuming that the ideal PA can be designed with a PAE of 50%, we can find the following links to the HBT and MOSFET high-frequency performance parameters:

$$\mathrm{FoM}_{\mathrm{PA_HBT}} = \frac{J_{pfT}}{2} \min\left\{V_{\mathrm{DD}} - V_{\mathrm{CEsat}}, \frac{\mathrm{BV}_{\mathrm{CER}}}{2} - V_{\mathrm{CEsat}}\right\} \cdot \min\left\{\mathrm{MSG}, \frac{f_{\mathrm{MAX}}^2}{f^2}\right\} \cdot 0.5 \cdot f^2 \quad (6)$$

$$\mathrm{FoM}_{\mathrm{PA_MOS}} = \frac{I_{\mathrm{ON}}}{4} \min\left\{V_{\mathrm{DD}} - V_{\mathrm{DSAT}}, \frac{\mathrm{BV}_{GD}}{2} - V_{\mathrm{DSAT}}\right\} \cdot \min\left\{\mathrm{MSG}, \frac{f_{\mathrm{MAX}}^2}{f^2}\right\} \cdot 0.5 \cdot f^2 \quad (7)$$

where the optimal large-signal load resistances are given by

$$R_{\mathrm{Lopt_HBT}} = \frac{\min\left\{V_{\mathrm{DD}} - V_{\mathrm{CEsat}}, \frac{\mathrm{BV}_{\mathrm{CER}}}{2} - V_{\mathrm{CEsat}}\right\}}{J_{pFT} \times A_E} \quad (8)$$

$$R_{\mathrm{Lopt_MOS}} = \frac{2 \cdot \min\left\{V_{\mathrm{DD}} - V_{\mathrm{DSAT}}, \frac{\mathrm{BV}_{GD}}{2} - V_{\mathrm{DSAT}}\right\}}{I_{\mathrm{ON}}} \quad (9)$$

and J_{pfT} is the transistor peak f_T current density per emitter area. If the frequency of operation is large enough that the transistor becomes unconditionally stable, then $\mathrm{FoM}_{\mathrm{PA}}$ can be linked to J_{pfT}, the breakdown voltage BV (B_{VCER} for HBTs) and f_{MAX}

$$\mathrm{FoM}_{\mathrm{PA}} = \frac{J_{pfT} \cdot \mathrm{BV} \cdot f_{\mathrm{MAX}}^2}{8}. \quad (10)$$

The last edition of the ITRS charts tuned LNA, tuned PA, VCO, and current-mode-logic (CML) inverter delay across 5 SiGe HBT technology nodes (N1 through N5) through the 2030 ITRS time horizon. Single-transistor tuned LNA, power amplifier, and voltage-controlled oscillator benchmark circuits have been optimized at 60, 94, 140, and 220 GHz in each of the five technology nodes and their performance has been tabulated in the ITRS document and published in [16]. The CML inverter delay scaling is representative of high-speed digital circuits such as the divider chain in the PLL but also of analog/mixed-signal circuits such as the THA and the current steering output stage of DACs.

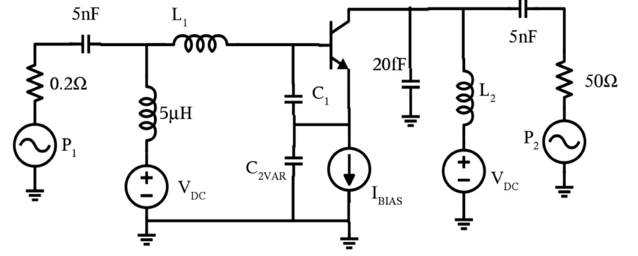


Fig. 13. *AMOS varactor-tuned Colpitts VCO test bench [15].*

High current models (HICUMs) used to design these circuits were extracted for each technology node from realistic TCAD-simulated dc and high-frequency characteristics of scaled SiGe HBTs with realistic doping profiles and contact parasitics [16]. Node 1 reflects SiGe HBT performance already reported by several foundries in the United States and Europe, similar to the one shown in Figs. 4–7. Here we will focus on some of the details of those circuits not published in [16], and review the performance of new SiGe HBT benchmark circuits important for broadband fiber-optic receivers and transmitters. CMOS PA and power DAC performance scaling is also briefly discussed.

The varactor-tuned Colpitts VCO benchmark circuit is shown in Fig. 13. It includes an output pad capacitance of 20 fF and finite tank inductor Q. It directly drives a 50-Ω load, making it easy to calculate the output power and the efficiency unambiguously. Differential versions of this fundamental frequency VCO topology with HBT varactors [25] and, more recently, with low-voltage accumulation mode MOS (AMOS) varactors have already been designed at 140 and 220 GHz, fabricated in a 55-nm SiGe BiCMOS process [17] corresponding to Node 1 in [16], and validated in measurements at frequencies as high as 250 GHz. However, the performance of the manufactured 220-GHz VCO in Node 1 is not sufficient for products yet, with the tuning range smaller than 5% and very sensitive to supply pushing, the output power lower than −4 dBm, and the phase noise higher than −78 dBc/Hz at 1-MHz

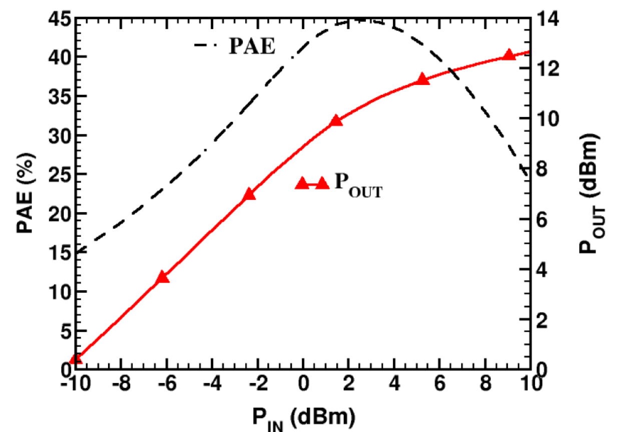


Fig. 14. *Simulated 220-GHz PA performance in SiGe HBT Node 5 with f_T/f_{MAX} of 0.78/2 THz [15].*

offset. In Node 5, the phase noise is predicted to improve to −91 dBc/Hz at 1-MHz offset [16].

The simulated performance of the 220-GHz tuned power amplifier in Node 5 is illustrated in Fig. 14. The circuit consists of a large common-emitter HBT biased for class B operation, with ideal input and output matching networks. A PAE as high as 45% with 7-dB associated gain and 10.6-dBm output power (1.6 mW/μm of emitter length) are expected by 2030.

Although HBTs in the present SiGe BiCMOS technology node have inadequate performance for efficient power amplifiers and low-phase noise oscillators at 220 GHz, a 230–260-GHz VCO-doubler-divider signal source has been reported recently with over 7-dBm output power, 1.5% PAE, and a phase noise of -84 dBc/Hz at 1-MHz offset [26]. For comparison, InP HBT PAs with 22-dBm output power and 1.5% efficiency have been reported at 214 GHz [27].

As we have seen in Section IV, the TIA is an important circuit building block for broadband ADCs, silicon photonics, and fiberoptic applications. In modern fiber-optic systems, the TIA amplifies signals with complex modulation formats. Therefore, it must simultaneously be broadband, low noise, and linear, while consuming as little power as possible and providing large (transimpedance) gain. The linearity specification is typically captured by the total harmonic distortion (THD) and by the maximum linear input current or voltage range, if driven by a 50-Ω source rather than a photodiode. The FoM of the TIA can then be defined as

$$\mathrm{FoM}_{\mathrm{TIA}} = \frac{Z \cdot I_{\mathrm{MAX}} \cdot \mathrm{BW}}{i_n^{\mathrm{rms}} \times P \cdot \mathrm{THD}} \quad (11)$$

where Z [Ω] is the transimpedance gain, I_{MAX} [A] is the maximum input linear current, BW [Hz] is the 3-dB bandwidth, i_n^{rms} [A] is the equivalent input noise current, and P[W] is the dc power consumption.

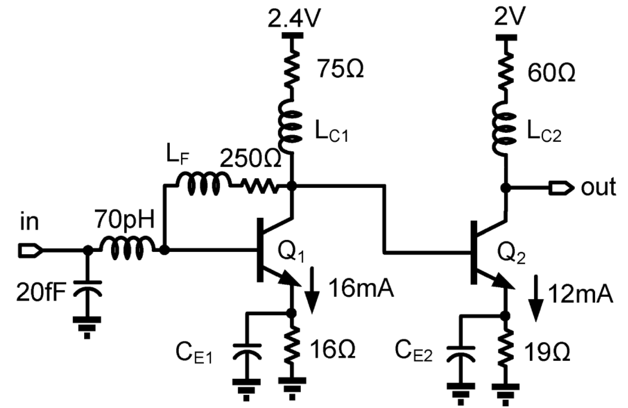
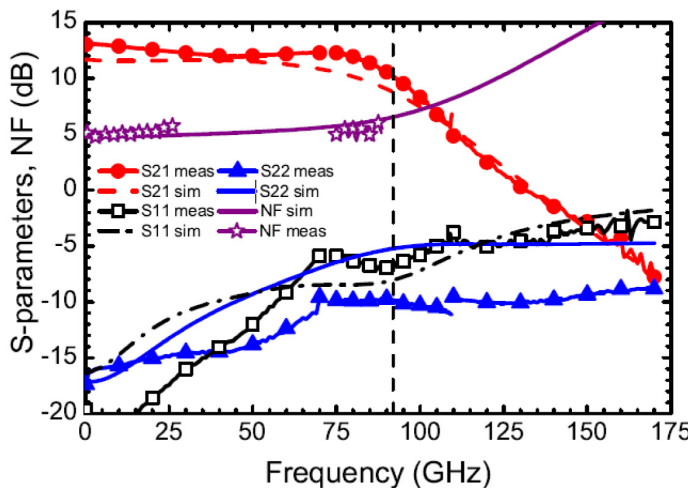


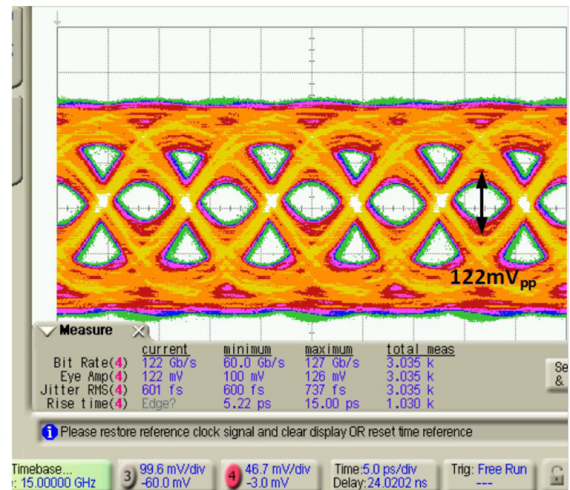
Fig. 15. ***TIA benchmark circuit.***

The TIA benchmark circuit shown in Fig. 15 was designed, fabricated, and tested in the 55-nm SiGe BiCMOS process described earlier, with similar performance as that of Node 1. An input pad (or photodiode) capacitance of 20 fF is also included in the test bench. The circuit was designed to be input matched to 50 Ω, with an input linear range of 300 $\mathrm{mV_{pp}}$, and was biased at the minimum noise figure current density at 90 GHz, which is approximately 1 mA/μm of emitter length. A comparison of the measured and simulated S-parameters and noise figure is reproduced in Fig. 16(a) from [28]. Together with the measured eye diagrams at 120 Gb/s shown in Fig. 16(b), they mark record bandwidth, noise figure, and data rate performance for silicon TIAs.

The TIA benchmark circuit was next optimized and simulated in Nodes 1–5, as illustrated in Fig. 17, retaining the 20-fF input pad/photodiode capacitance, 250-Ω transimpedance feedback resistor, 50-Ω input matching, and 50-Ω output buffer.



(a)



(b)

Fig. 16. ***(a) A comparison of the measured and simulated S-parameters and noise figure of the SiGe TIA benchmark circuit manufactured in Node 1. (b) Measured PRBS-31 eye diagram at 120 Gb/s [28].***

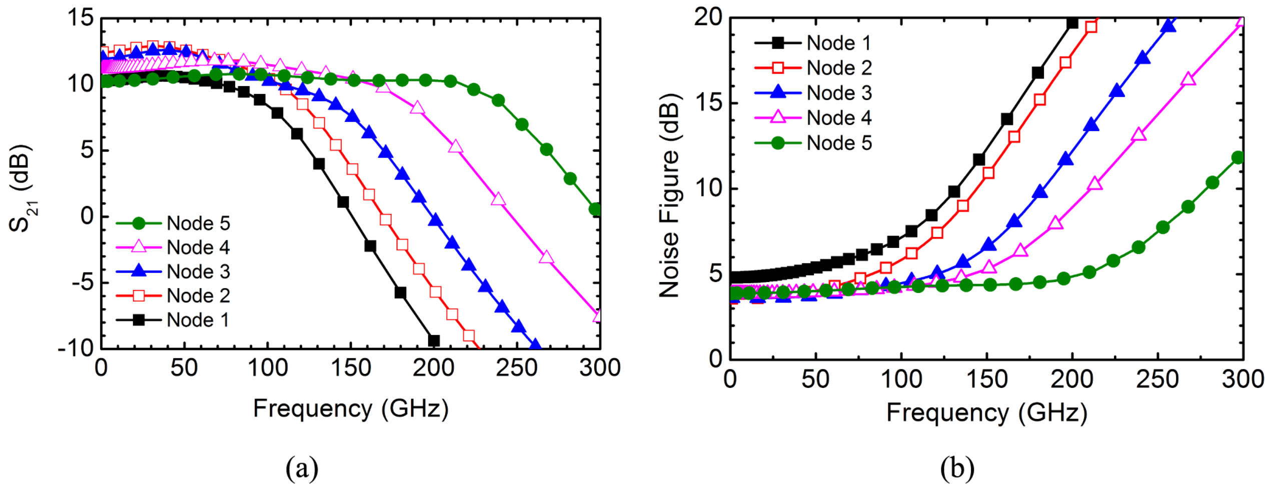


Fig. 17. *Simulated TIA: (a) S_{21}; and (b) 50-Ω noise figure scaling.*

The simulated bandwidth increases from 100 GHz in Node 1 to 250 GHz in Node 5 while the in-band noise figure remains around 3–4 dB in all nodes. The input linear range is 300 mV_{pp} in all cases. The Node 1 component values reflect the fabricated 55-nm SiGe BiCMOS circuit described earlier, while the component values of the Node 2–5 circuits were designed to maintain the same power consumption and gain. The role of the emitter degeneration capacitors is to introduce zeros at medium-to-high frequency, to compensate for the dominant pole and to reduce the noise contribution of the degeneration resistors. The peaking inductors add further zeros to the transfer function at the highest frequency to compensate for the second pole and reduce noise from the transimpedance feedback resistor. As shown in Fig. 18, a bandwidth of 250 GHz with 10-dB gain, and a noise figure smaller than 5 dB are predicted. The power consumption of the TIA stage is 40 mW in Nodes 2–5, and only 26 mW in Node 1. Such performance will be adequate for fiber-optic receivers operating at over 320 GBaud with an energy efficiency better than 110 fJ/b even when simple non-return-to-zero (NRZ) modulation format is employed.

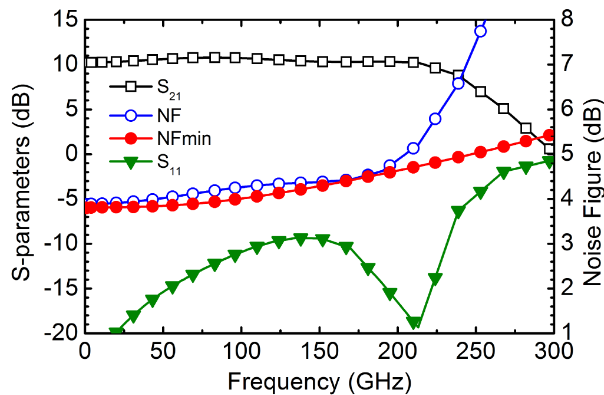


Fig. 18. *Simulated TIA performance in Node 5.*

In broadband instrumentation receivers, a low-noise distributed amplifier (DA) can provide similar noise figure as a TIA with better linearity, more bandwidth, and better input and output matching. Such an example of a dc-coupled distributed amplifier fabricated in the same 55-nm SiGe BiCMOS process is shown in Fig. 19 [29]. By taking advantage of the 55-nm MOSFET-HBT cascode, a bandwidth of 135 GHz was achieved with 9-dB gain, a noise figure lower than 7 dB up to 88 GHz, and 3-dBm input compression point with 100-mW total power consumption. Compared to the TIA, the input linearity is increased by more than 6 dB, the bandwidth is 50% larger, but the power consumption has doubled and the occupied silicon area is much larger. An even larger bandwidth of 170 GHz was reported in a SiGe-HBT-only DA

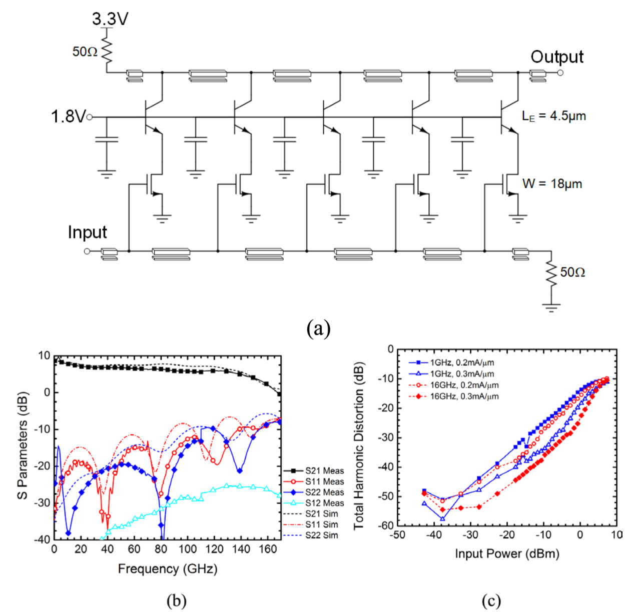


Fig. 19. *Distributed linear LNA in 55-nm SiGe BiCMOS (Node 1): (a) schematic and (b) measured S-parameters; and (c) measured THD [29].*

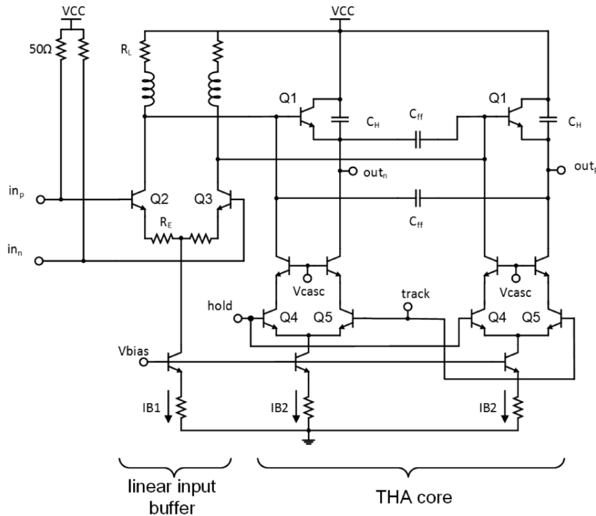


Fig. 20. ***THA benchmark circuit.***

employing a triple-cascode cell with input capacitive division [30]. Unfortunately, series input capacitors make it unusable in dc-coupled fiber-optic receivers because the low-frequency cutoff is 1 GHz. For comparison, InP HEMT DAs with 180-GHz bandwidth were reported as early as 1998 [31].

As discussed in Section IV, for the future generation of ADCs used in fiber-optic systems, a very broadband sampler is needed. While CMOS series switches can provide bandwidths of over 100 GHz, they require rail-to-rail switching signals and CMOS logic which cannot operate with 100-GHz or higher frequency clock signals. A potential solution is a bipolar or BiCMOS CML THA, as shown in Fig. 20, whose performance scales with the HBT f_T and f_{MAX}. This is a truly mixed-signal circuit, where the input differential pair forms a linear amplifier with a gain of 1, followed by a differential switched emitter follower which charges the hold capacitors C_H. To first order, the size and tail current of the emitter followers and the value of the hold capacitors dictate the small-signal bandwidth of the circuit and its linearity, while the bottom CML cascode switches determine the sampling speed. To maximize the tracking mode bandwidth, the size of the switched emitter follower HBT is chosen such that its base emitter capacitance is equal to the total hold capacitance (including the parasitic capacitance at the hold capacitor node). This circuit is popular in both InP HBT and SiGe HBT incarnations. A suitable FoM for the THA must be proportional to the gain G, tracking bandwidth BW, sampling clock frequency f_{clk}, and linearity, described by the spurious-free dynamic range (SFDR) and input compression point (IP1), and inversely proportional to the dc power consumption P of the THA

$$\text{FoM}_{\text{THA}} = \frac{G \cdot \text{IP1} \cdot \text{BW} \cdot \text{SFDR} \cdot f_{\text{clk}}}{P}. \tag{12}$$

With the Node 1 SiGe HBT, it is possible to achieve over 70-GHz bandwidth and sampling clock frequencies in excess of 100 GHz.

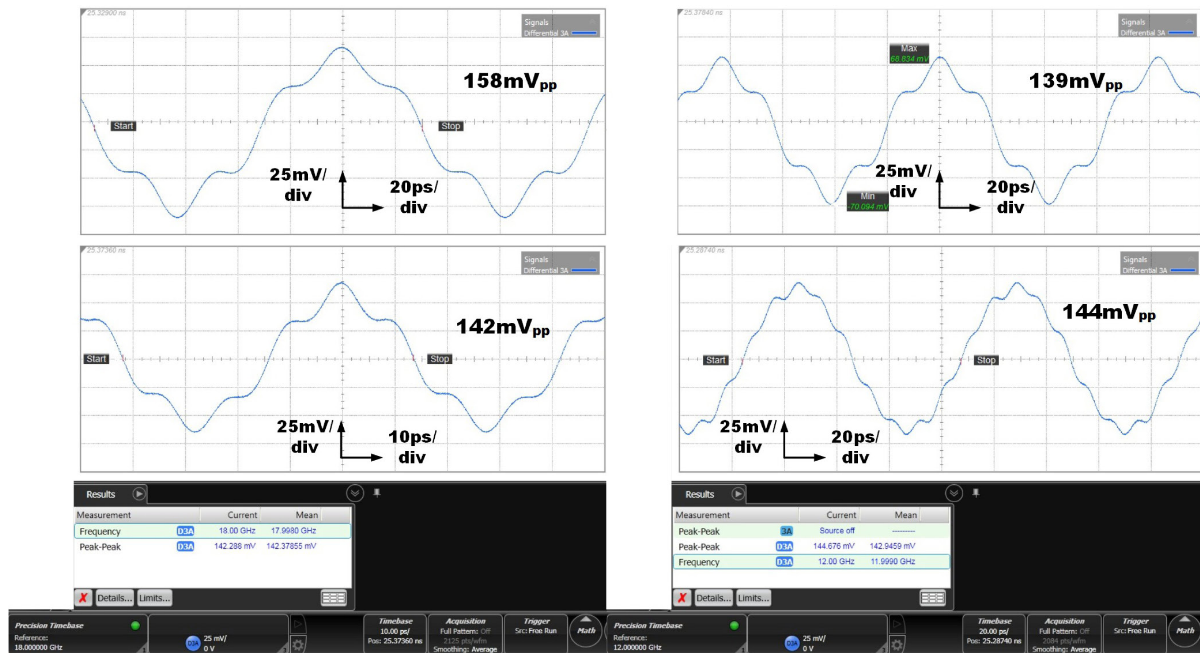


Fig. 21. ***Measured differential output waveforms of a 55-nm SiGe BiCMOS THA manufactured in Node 1 for a single-ended sinusoidal input at 8 GHz sampled at 40 GS/s (top left), 12 GHz sampled at 60 GS/s (top right), 18 GHz sampled at 90 GS/s (bottom left), and 12 GHz sampled at 108 GS/s [32].***

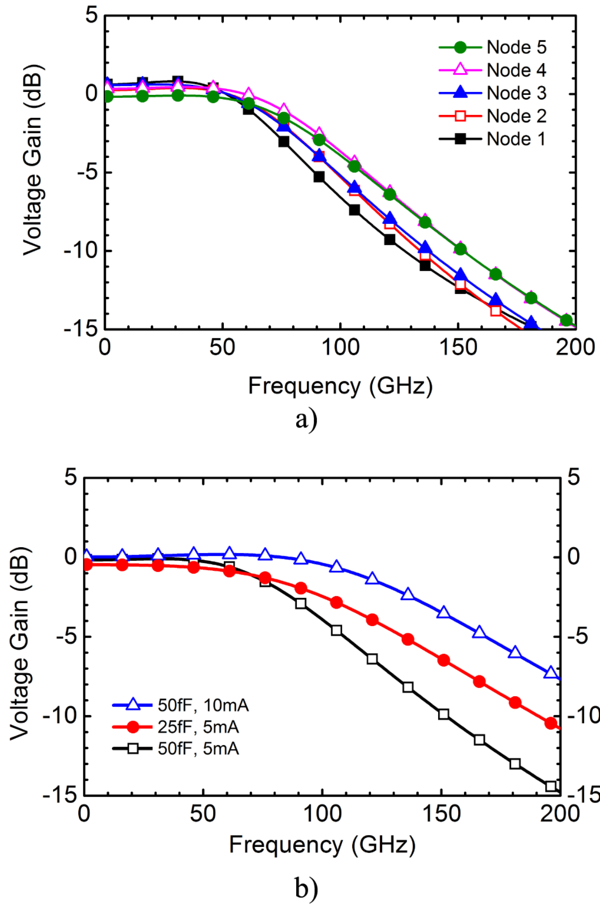


Fig. 22. ***(a) THA small-signal gain and tracking bandwidth as a function of technology node as at constant power consumption and 50-fF hold capacitors. (b) Impact of hold capacitance and THA tail current on tracking bandwidth in Node 5.***

Fig. 21 shows the measured sampled output waveforms from a variant of this topology fabricated in the 55-nm SiGe BiCMOS process. In this version, the bipolar cascode CML switches were replaced by quasi-CML MOS-HBT switches to reduce the power consumption. The circuit has a measured small-signal bandwidth of 40 GHz, SFDR of 49 dB, IP1 of −4 dBm, consumes 87 mW, and operates with record sampling clock frequencies from 40 up to 108 GHz [31].

A THA testbench was created and simulated across the five technology nodes. The input pad capacitance of 20 fF and the hold capacitance of 50 fF were kept constant and the total power consumption of the input buffer and of the THA core was also kept constant at 42 mW. As shown in Fig. 22(a), the bandwidth improves marginally from 70 GHz in Node 1 to 92 GHz in Node 5. However, Fig. 22(b) illustrates for Node 5 that, if the current is doubled or the hold capacitance is halved, the tracking bandwidth is further increased. The preferred solution is to double the tail currents and power consumption to 84 mW while keeping the same hold capacitance of 50 fF to avoid degradation in SFDR. The Node 5 THA tracking bandwidth becomes 140 GHz, and the sampling frequency (125 GHz with 25% duty cycle) is doubled compared to those in Node 1 with similar SNDR and IP1. However, if the tail current of the input buffer and THA core is also doubled to 10 mA in the Node 1 benchmark THA, its tracking bandwidth improves from 70 to 93 GHz. The latter values are sufficiently large for ADCs aimed at 128-GBaud 16QAM fiber-optic receivers required for 1-Tb/s fiber-optic systems.

Just like the tuned power amplifier and tuned power DAC in wireless communication transceivers, the large-swing linear modulator driver and large-swing DAC play the most critical role in a broadband fiber-optic transmitter. The bandwidth, the output (linear) voltage swing, and the linearity of the driver must be maximized while the total power consumption must be reduced. The power gain G must be sufficient to reach the desired output voltage swing with the low input voltages of 200–300 $\mathrm{mV_{pp}}$ expected at the output of a nanoscale CMOS DAC. A possible FoM for linear large-swing drivers then becomes

$$\mathrm{FoM}_{\mathrm{OpticalModDriver}} = \frac{V_{\mathrm{opp}} \cdot \mathrm{BW} \cdot G \cdot \mathrm{IP1}}{P} \tag{13}$$

where V_{opp} [V] is the peak-to-peak output voltage swing provided by the driver into the optical modulator. Most optical modulators require voltage swing in excess of 4 $\mathrm{V_{pp}}$ for proper operation, making it extremely challenging to design a linear large-swing driver with bandwidth larger than 70 GHz in any technology.

For future generations of fiber-optic systems operating at 128 GBaud and beyond, distributed driver topologies, like the one depicted in Fig. 23(a), are likely the best solution. Given the low breakdown voltage of silicon technologies with large enough f_T and f_{MAX} for the required bandwidth, a cascode topology with one or more transistors in the stack must be employed. Such a driver, with 6-$\mathrm{V_{pp}}$ differential output swing, based on the MOS-HBT cascode cell in Fig. 23(b), was fabricated in a 90-nm SiGe BiCMOS technology with a SiGe HBT f_T/f_{MAX} comparable to that of Node 1. A bandwidth of over 80 GHz was achieved with an input compression point of 5 dBm per side and a saturated output power of 18 dBm, as illustrated in Fig. 23(c) and (d). The measured bandwidth is lower than that of the low-noise DA in Fig. 19 because of the much larger transistor sizes and input and output cell capacitances of the DA cell needed to achieve the large output swing.

The same distributed amplifier concept can be applied to a power DAC which can directly drive an optical modulator without the need for linear amplification, thus improving efficiency. This is illustrated in Fig. 24(a) which describes a segmented 6-b power DAC with 7-$\mathrm{V_{pp}}$ differential output swing [29]. In its simplest form, the DAC cell can employ a differential (cascode) pair, as in Fig. 24(b). However, if the cell is realized as multiplexer [Fig. 24(c)], a time-interleaved power DAC is obtained, doubling the sampling rate.

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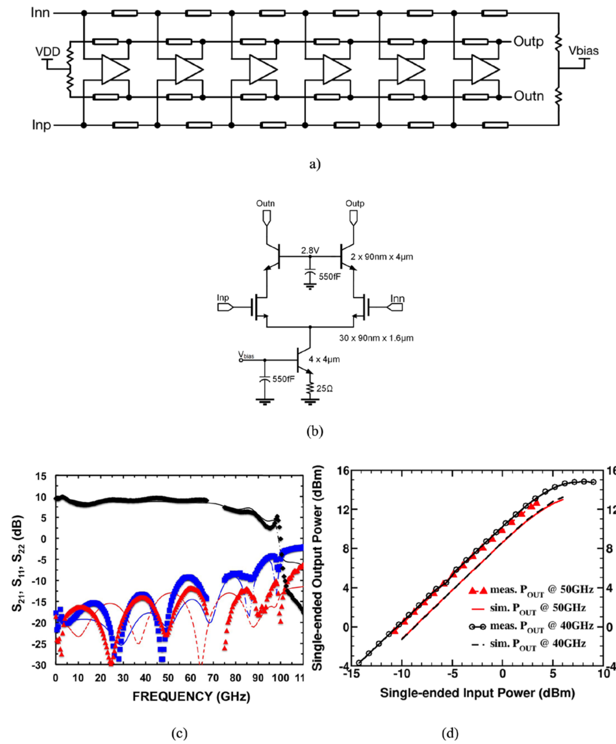

Fig. 23. ***Distributed linear modulator driver amplifier of 90-nm SiGe BiCMOS (Node 1): (a) block diagram; (b) output cell schematic; (c) measured S-parameters; and (d) measured, IP1dB, P1dB, and P_{SAT} [24].***

An output bandwidth of 65 GHz with 7-V_{pp} differential output swing has been measured for this segmented, 6-b power MUX-DAC architecture [29] in the 55-nm SiGe BiCMOS technology described earlier. If ideal lossless transmission lines are assumed, the bandwidth of the distributed amplifier architecture will scale with f_{MAX} and MAG of the cascode stage employed in the DAC cell. Given that the SiGe HBT f_{MAX} is predicted to increase from 400 GHz in Node 1 to 2 THz in Node 5, it is very likely that power DACs with over 200-GHz output bandwidth and > 4 V_{pp} output swing will be realizable in Node 5. A different example of a 100-GS/s time-interleaved distributed DAC architecture was implemented in 32-nm CMOS [33]. However, the measured output bandwidth is smaller than 20 GHz.

Finally, what can we say about CMOS benchmark circuit scaling? Not much, since f_T data alone are not sufficient to predict mm-wave tuned and broadband circuit performance. Without f_{MAX} and all the layout parasitics accurately captured in a compact model, a CMOS benchmark circuit scaling exercise at 140 and 220 GHz becomes futile. Nevertheless, up until now, with very careful MOSFET layout to minimize gate resistance so as not to compromise f_T, it has been possible to simultaneously achieve similar or higher f_{MAX} values. A number of fundamental frequency CMOS oscillators have been published up to 300 GHz, albeit with very poor tuning range, output power, and phase noise performance.

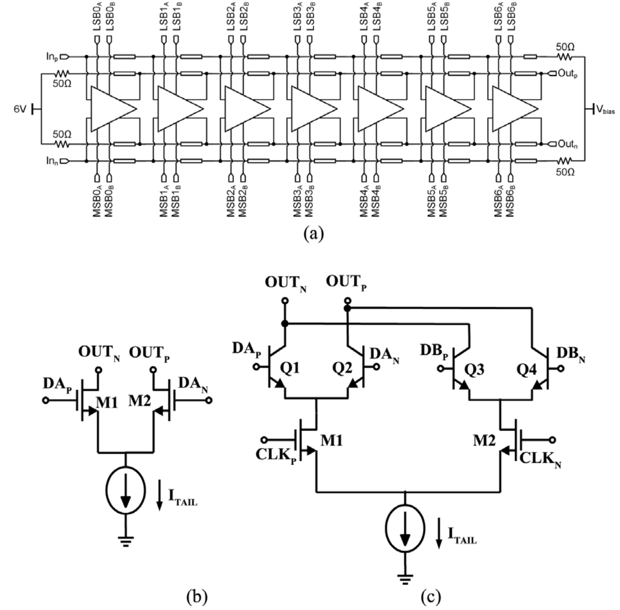

Fig. 24. ***Distributed power DAC: (a) block diagram [29]; (b) current-steering cell; and (c) time-interleaved current steering cell schematic.***

Most published CMOS signal sources which operate above 140 GHz employ n-push [34], [35], [36] or multiplier-based architectures [37] with some form of on-chip or free-space power combining [38], [39] to overcome the output power limitations.

Fig. 25 compares single common-source MOSFET PA benchmark circuit simulations at 140 GHz in 45-nm partially depleted (PD) SOI and 28-nm UTBB FD-SOI technologies. The measured f_T and f_{MAX} of the fully wired 45-nm PD-SOI n-channel MOSFET are approximately 250 GHz [38]. In both cases, fully wired n-channel MOSFETs with single-gate contact (for stability reasons) and all extracted

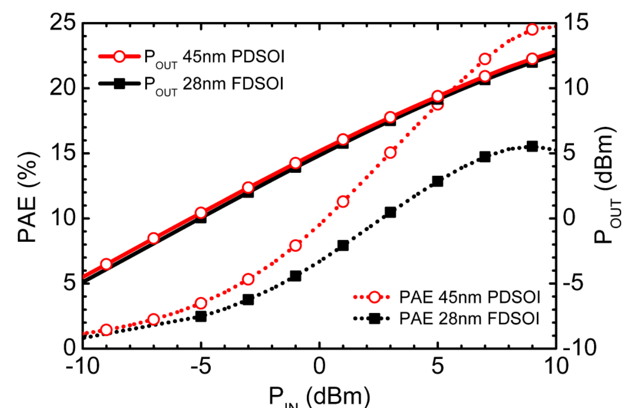

Fig. 25. ***Simulated 208 × 28nm × 780nm FD-SOI (V_{DD} = 1 V) and 96 × 45nm × 770nm PD-SOI (V_{DD} = 1.1 V) class AB (0.2 · I_{ON}) n-MOS PA benchmark performance at 140 GHz.***

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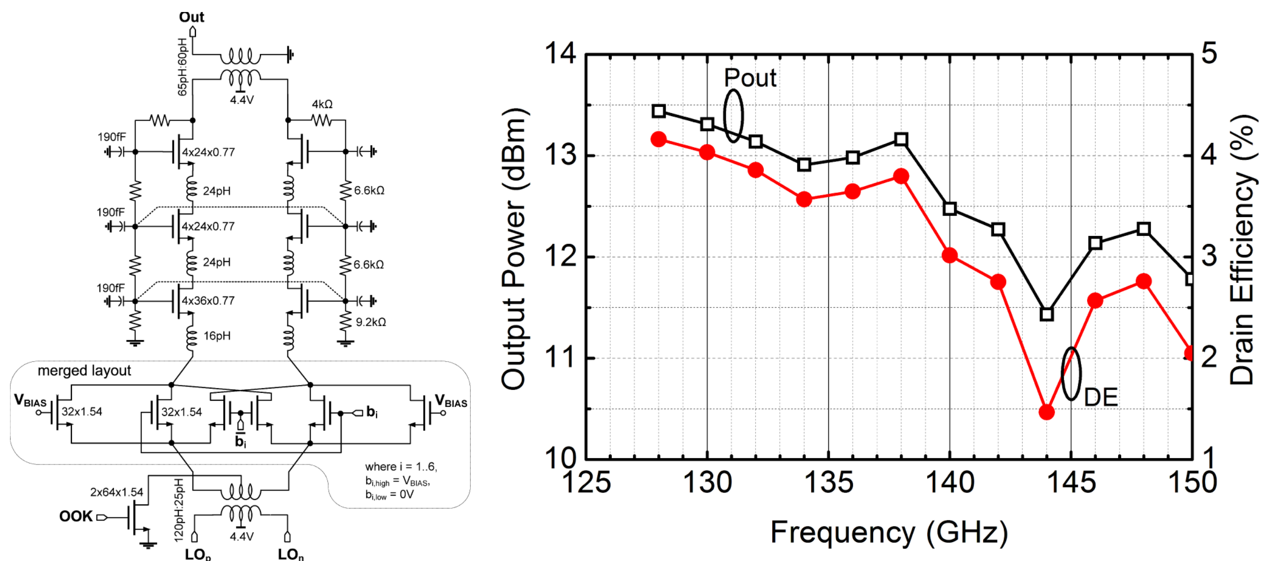

Fig. 26. ***(a) Tuned 45-nm PD-SOI CMOS power DAC output stage schematic; and (b) measured performance at 140 GHz [40].***

RC layout parasitics were included in the simulations. Ideal lossless input and output matching networks were used. Since at 140 GHz the MAG/MSG of these MOSFETs is lower than 7 dB, they were biased in class AB for maximum possible PAE and were sized for an output power of 10 dBm. Other classes of PAs are simply not feasible in state-of-the-art CMOS technology at 140 GHz due to the small power gain. The supply voltage was set to the maximum allowed V_{DS}, 1.1 V in 45-nm PD-SOI and 1 V in 28-nm UTBB FD-SOI. The results in Fig. 25 show a peak PAE of 24.8% for the 45-nm design and only 15% for the 28-nm UTBB FDSOI PA. Although the 28-nm UTBB FD-SOI n-MOSFET has higher f_T, it requires a larger gate width and total current for the same output power because of the smaller drain voltage. The additional layout parasitics and the lower supply end up degrading the efficiency.

Similar to the MOS-HBT and HBT-HBT cascodes, a technique to overcome the small gain and output swing of deeply scaled MOSFETs is to create a composite transistor with increased MAG and safe operating voltage swing by series stacking SOI MOSFETs in a supercascode structure. This is possible in 14-nm FD-SOI and SOI FinFET technologies but not in bulk FinFET technology. Fig. 26 reproduces the schematics and measured output power and drain efficiency of a tuned 140-GHz power DAC series-stacked output stage [40] designed in the 45-nm PD-SOI technology. The measured output power is 12–13 dBm from 128 to 142 GHz but, because of the much more complex topology needed to achieve over 10-dB gain in the output stage and because of the losses of the output matching network, the efficiency is significantly smaller than the ideal value simulated for the lossless common-source PA in Fig. 25.

In the circuits discussed in this paper, it has been assumed that inductors and capacitors have infinite quality factor. As explained, this has been necessary in order to better link the benchmark circuit performance to the transistor technology and to render the benchmark circuit exercise manageable by reducing the number of design variables. While in broadband circuits, like the TIA and THA, the quality factor of the reactive elements is largely irrelevant, for tuned circuits such as the LNA, PA, and VCO, the quality factors of inductors, transformers, capacitors, and transmission lines can significantly degrade the high-frequency performance parameters such as gain, noise figure, phase noise, and PAE, and also increase power consumption. For example, in low power IoT and touchless gesture control sensors, the main limitation for power savings is the quality factor of the passive elements that can be fabricated in a given technology, which, in turn, depends on the dielectrics and metals employed in the back-end. For a given amplifier gain, reducing the amplifier bias current along with the transistor size also reduces the transconductance and power gain, unless the load impedance is proportionally increased. However, the effective load impedance for a reactive network can only be increased by increasing the quality factor of the inductors, capacitors, transformers, and/or transmission lines that form it. Unfortunately, the more advanced is the CMOS or SiGe BiCMOS node, the thinner are the dielectrics and metals employed, degrading the quality factor. While the latter can be improved, at a significant cost, by deploying thicker "RF" metal layers and dielectrics on top of the standard BEOL, the lower level metal layers limit the current that can be extracted in a single metal

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layer from a MOSFET gate finger or an HBT emitter. This problem has become apparent in 22- and 14-nm FD-SOI and FinFET technology, where the current driving capability of the contact vias and first metal layers limit the maximum current density at which a MOSFET can be operated reliably at junction temperatures of 110 °C and especially at 125 °C to less than 0.2 mA/μm, unless the gate finger width is significantly reduced. The low current densities or the very narrow gate fingers further degrade f_T, f_{MAX}, and NF from the peak values reported in the literature and in this paper, and which are reached at drain current densities of 0.3–0.4 mA/μm. Unless new metals are introduced, this problem will be exacerbated in future technology nodes.

VI. CONCLUSION

The high-frequency performance of state-of-the-art CMOS and SiGe BiCMOS technologies and how it will evolve in future technology nodes beyond 2030 has been reviewed. Measurements from dc to 325 GHz show for the first time that today's production SiGe BiCMOS and CMOS technologies have f_T and f_{MAX} which simultaneously exceed 325 GHz (based on the measured H_{21} and MAG of fully wired transistors up to 325 GHz), sufficient for the development of commercial mm-wave ICs operating at frequencies beyond 120 GHz. TCAD and atomistic simulations confirm that silicon CMOS is theoretically scalable to physical gate lengths of 2 nm, but surface scattering and quantum effects will most likely lead to degradation of the high-frequency performance below 10-nm physical gate lengths. With the caveat that they are very sensitive to the mobility model employed, simulations predict that the cutoff frequency of silicon MOSFETs will peak at about 700 GHz. The performance saturation of mm-wave CMOS power amplifiers with scaling is already apparent in the 28-nm node. In contrast, SiGe HBTs show ideal performance scaling to f_T and f_{MAX} of 0.78 THz and 2 THz, respectively. Moreover, simulations of SiGe HBT benchmark circuits based on sophisticated compact models derived using TCAD predict that circuit performance will continue to improve with scaling and that silicon systems on chip will be realizable with fundamental frequencies of operation approaching 300 GHz. These will be more than adequate for all the large volume high data rate radio, fiber-optic, and sensing applications envisaged today for the next 15 years. For applications beyond 300 GHz, system architectures will continue to rely on multiplier chains, subharmonic mixing, and free space power combining.

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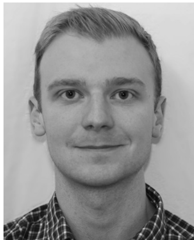

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