W-BAND FRONT-END INTEGRATED CIRCUITS
IN 65NM CMOS TECHNOLOGY

BY

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W-band Front-End Integrated Circuits  
In 65nm CMOS Technology  

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Abstract  

Design and Implementation of W-band LNAs, down-converter, IQ-receiver and 80GHz DCO in 65nm is discussed in this thesis. Design methodology of the shunt-series, transformer-feedback LNA is investigated and compared to the traditional series-series, inductive feedback LNA. The performance of the down-converter incorporating the transformer-feedback LNA is described. With high bandwidth, low noise and low power consumption, the down-converter is suitable for imaging and remote sensing applications. The IQ-receiver is implemented to assess the feasibility of an image-reject receiver architecture and verify the quadrature operation of the VCO presented in [1]. The design of an 80GHz DCO is presented. This topology with digitally controlled, binary-weighted varactors offers a linear tuning curve and can be used in realizing fully digital synthesizers.
Acknowledgments

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<th>Description</th>
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</thead>
<tbody>
<tr>
<td>$B_{sopt}$</td>
<td>optimum noise susceptance of amplifier (S)</td>
</tr>
<tr>
<td>$C_{DB}$</td>
<td>MOSFET drain to bulk capacitance (F)</td>
</tr>
<tr>
<td>$C_{GD}$</td>
<td>MOSFET gate to drain capacitance (F)</td>
</tr>
<tr>
<td>$C_{GS}$</td>
<td>MOSFET gate to source capacitance (F)</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>output capacitance (F)</td>
</tr>
<tr>
<td>$C_{PAD}$</td>
<td>pad capacitance (F)</td>
</tr>
<tr>
<td>$C_{SB}$</td>
<td>MOSFET source to bulk capacitance (F)</td>
</tr>
<tr>
<td>$e_n$</td>
<td>equivalent series noise voltage (V)</td>
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<tr>
<td>$F$</td>
<td>noise factor (in linear units)</td>
</tr>
<tr>
<td>$F_{MIN}$</td>
<td>minimum noise factor (in linear units)</td>
</tr>
<tr>
<td>$F_{MINa}$</td>
<td>minimum noise factor of amplifier (in linear units)</td>
</tr>
<tr>
<td>$f$</td>
<td>frequency (Hz)</td>
</tr>
<tr>
<td>$f_T$</td>
<td>cutoff frequency (Hz)</td>
</tr>
<tr>
<td>$f_{Teff}$</td>
<td>effective cutoff frequency (Hz)</td>
</tr>
<tr>
<td>$G$</td>
<td>power gain (in linear units)</td>
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<tr>
<td>$G_P$</td>
<td>transformer primary loss conductance (S)</td>
</tr>
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<td>correlated noise conductance of amplifier (S)</td>
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<tr>
<td>$G_{na}$</td>
<td>noise conductance of amplifier (S)</td>
</tr>
<tr>
<td>$G_{nf}$</td>
<td>noise conductance of feedback (S)</td>
</tr>
<tr>
<td>$G_u$</td>
<td>un-correlated noise conductance (S)</td>
</tr>
<tr>
<td>$G_{ua}$</td>
<td>un-correlated noise conductance of amplifier (S)</td>
</tr>
<tr>
<td>$G_{uf}$</td>
<td>un-correlated noise conductance of feedback (S)</td>
</tr>
<tr>
<td>$G_s$</td>
<td>source noise conductance (S)</td>
</tr>
<tr>
<td>$G_{sopt}$</td>
<td>optimum source noise conductance (S)</td>
</tr>
<tr>
<td>$G_{sopta}$</td>
<td>optimum source noise conductance of amplifier (S)</td>
</tr>
<tr>
<td>$g_m$</td>
<td>transconductance (A/V)</td>
</tr>
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<td>$g_{meff}$</td>
<td>effective transconductance (A/V)</td>
</tr>
<tr>
<td>$g'_{meff}$</td>
<td>effective transconductance per unit gate width (A/V.m)</td>
</tr>
</tbody>
</table>
IDS  MOSFET drain source current (A)
IP3  third-order inter-modulation intercept (in dBm units)
i_c  correlated noise current (A)
i_n  equivalent shunt noise current (A)
i_s  source noise current (A)
i_u  un-correlated noise current (A)
J_{opt}  minimum noise figure current-density (A/m)
k  Boltzmann constant (1.38×10^{-23} J/K)
k_2  MOSFET noise constant
L_D  drain inductor (H)
L_G  gate inductor (H)
L_M  broad-banding inductor (H)
L_S  source inductor (H)
L_P  transformer primary inductance (H)
L_{SEC}  transformer secondary inductance (H)
NF  noise figure (in dB units)
NF_{MIN}  minimum noise figure (in dB units)
N_f  MOSFET number of fingers
P_{1dB}  1-dB compression point (in dBm units)
V_{DS}  MOSFET drain to source voltage (V)
V_T  MOSFET threshold voltage (V)
P  power consumption (W)
Q  quality factor
R_G  MOSFET gate resistance (Ω)
R_{LG}  gate inductor loss resistance (Ω)
R_{LS}  source inductor loss resistance (Ω)
R_S  MOSFET source resistance (Ω)
R_{SEC}  transformer secondary loss resistance (Ω)
R_S'  MOSFET source resistance per unit gate width (Ω.m)
R_{cora}  correlated noise resistance of amplifier (Ω)
R_n  noise resistance (Ω)
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{na}$</td>
<td>noise resistance of amplifier ($\Omega$)</td>
</tr>
<tr>
<td>$R_{nf}$</td>
<td>noise resistance of feedback ($\Omega$)</td>
</tr>
<tr>
<td>$R_{sopt}$</td>
<td>optimum source noise resistance ($\Omega$)</td>
</tr>
<tr>
<td>$R_{sopta}$</td>
<td>optimum source noise resistance of amplifier ($\Omega$)</td>
</tr>
<tr>
<td>$R_{of}$</td>
<td>un-correlated noise resistance of feedback ($\Omega$)</td>
</tr>
<tr>
<td>$T$</td>
<td>temperature (K)</td>
</tr>
<tr>
<td>$W_G$</td>
<td>MOSFET gate width ($\mu$m)</td>
</tr>
<tr>
<td>$W_f$</td>
<td>MOSFET finger width ($\mu$m)</td>
</tr>
<tr>
<td>$\omega$</td>
<td>angular frequency (rad/s)</td>
</tr>
<tr>
<td>$\omega_T$</td>
<td>angular cutoff frequency (rad/s)</td>
</tr>
<tr>
<td>$\omega_{Teff}$</td>
<td>effective angular cutoff frequency (rad/s)</td>
</tr>
<tr>
<td>$X_{sopta}$</td>
<td>optimum source reactance of amplifier ($\Omega$)</td>
</tr>
<tr>
<td>$Y_c$</td>
<td>correlation admittance (S)</td>
</tr>
<tr>
<td>$Y_{cor}$</td>
<td>correlated noise admittance (S)</td>
</tr>
<tr>
<td>$Y_{cora}$</td>
<td>correlated noise admittance of amplifier (S)</td>
</tr>
<tr>
<td>$Y_{corf}$</td>
<td>correlated noise admittance of feedback (S)</td>
</tr>
<tr>
<td>$Y_{sop}$</td>
<td>optimum source noise admittance (S)</td>
</tr>
<tr>
<td>$Y_s$</td>
<td>source admittance (S)</td>
</tr>
<tr>
<td>$Z_0$</td>
<td>source resistance ($\Omega$)</td>
</tr>
<tr>
<td>$Z_{IN}$</td>
<td>input impedance ($\Omega$)</td>
</tr>
<tr>
<td>$Z_L$</td>
<td>load impedance ($\Omega$)</td>
</tr>
<tr>
<td>$Z_{corf}$</td>
<td>correlated noise impedance of the amplifier ($\Omega$)</td>
</tr>
<tr>
<td>$Z_{sopta}$</td>
<td>optimum source noise impedance of amplifier ($\Omega$)</td>
</tr>
</tbody>
</table>
## List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>AMOS</td>
<td>Accumulation mode metal-oxide-semiconductor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal-oxide-semiconductor</td>
</tr>
<tr>
<td>CG</td>
<td>Common gate</td>
</tr>
<tr>
<td>CS</td>
<td>Common source</td>
</tr>
<tr>
<td>DCO</td>
<td>Digitally controlled oscillator</td>
</tr>
<tr>
<td>DSB</td>
<td>Double side-band</td>
</tr>
<tr>
<td>DSL</td>
<td>Digital subscriber line</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital signal processing</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal communication commission</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of merit</td>
</tr>
<tr>
<td>GP</td>
<td>General purpose</td>
</tr>
<tr>
<td>HBT</td>
<td>Heterojunction bipolar transistor</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate frequency</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LP</td>
<td>Low power</td>
</tr>
<tr>
<td>LSB</td>
<td>Lower side-band</td>
</tr>
<tr>
<td>MAG</td>
<td>Maximum available power gain</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-insulator-metal</td>
</tr>
<tr>
<td>MOM</td>
<td>Metal-oxide-metal</td>
</tr>
<tr>
<td>NFET</td>
<td>n-Channel field effect transistor</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious free dynamic range</td>
</tr>
<tr>
<td>SiGe</td>
<td>Silicon-Germanium</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-a-chip</td>
</tr>
<tr>
<td>USB</td>
<td>Upper side-band</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra wide band</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage controlled oscillator</td>
</tr>
</tbody>
</table>
1 Introduction

The uninterrupted scaling of the CMOS technology into the nanometer regime has prompted engineers to conduct extensive research on the capabilities of CMOS for implementation of mm-wave integrated circuits [1-5], which have for long been the exclusive domain of compound semiconductors [6]. With a unity gain cutoff frequency of 185 GHz, the 65nm GP NFET is comparable in speed to the 0.13μm SiGe HBT, albeit with a lower breakdown voltage. Despite the shortcomings of CMOS for analog applications, the prospect of integrating the RF radio front-end and the DSP unit onto a single silicon chip gives CMOS a considerable advantage. Although mask generation and fabrication costs associated with nano-scale CMOS is extremely high, large volume production is expected to push down the unit price and render CMOS economical.

1.1 Motivation

With the growth of the market for wireless data transmission, the industry has progressively moved from one standard to the next. WiFi-N, the latest in the family of the 802.11 standards for wireless local area connectivity, achieves a potential network throughput of 200Mbps [7]. However, the 2.4GHz and 5GHz public bands are quickly running out of spectrum. The ultra wide-band (UWB) standard, while covering a larger spectrum (3.1-10.6 GHz), suffers from stringent power transmission constraints (-41dBm/MHz) so as to limit interference to those sharing the spectrum [8]. Thus the UWB technology has the potential for high data rate applications at very limited range.

It seemed inevitable that RF engineers would direct their attention towards the mm-wave frequencies, most notably the un-licensed 60GHz band (57-64 GHz) and the W-band (71-95 GHz). The past few years have seen an exponential growth in the number of publications discussing design issues and potential architectures in the 60GHz band. The high path loss at 60GHz, arising from the oxygen absorption, has been advertised as providing implicit security. However, this phenomenon does limit the communication range of a 60GHz radio [9].

While the challenges associated with IC design in silicon at W-band frequencies are similar to the 60GHz band, the lower path loss, higher beam directivity and a larger spectrum
(12.9GHz) allow for a wider range of applications, including: mm-wave imaging, automotive RADAR and last mile point-to-point links.

### 1.1.1 mm-Wave Imaging

Detection of concealed metal objects (weapons) is one possible application of the mm-wave imager, which has attracted new attention in light of recent security concerns. An active imager detects a target by illuminating the subject and creating an image based on the echo. In passive imaging, a thermal profile of the subject is created based on the contrast of thermal energy between metal objects and the human body. The passive imager does not emit radiation and is thus suitable for imaging the human body. Figure 1.1 shows the block diagram of a passive imager. The receiver detects the source radiation as noise power and the integrator reduces the variation on the signal.

![Block diagram of the passive imager.](image)

With a wavelength of 3-4 mm, the W-band imager can detect objects through clothing, fog and smoke [10]. The thermal resolution of the imager is given by (1.1), where $T$ is the noise temperature of the receiver. The resolution is inversely proportional to the bandwidth of the RF receiver ($B$) and the integration time ($\tau$) [11]. Low noise and large bandwidth are essential requirements of such a system.

\[ \Delta T \sim \frac{T}{\sqrt{B\tau}} \]  

(1.1)
1.1.2 Automotive RADAR

Many luxury automobiles manufactured today take advantage of automatic cruise control and collision avoidance systems. At the core of this system, lies a Doppler radar shown in Figure 1.2. The range and velocity of the target vehicle can be determined from the echo of the transmitted signal.

\[ R = \frac{c\tau}{2} \]  \hspace{1cm} (1.2)

And the velocity (v) of the target can be determined from the Doppler shift (\( \Delta f \)):

\[ v = \frac{c\Delta f}{f_{LO}} \]  \hspace{1cm} (1.3)

1.1.3 Point-to-Point Last Mile Radio

The IEEE 802.16 working group is poised to develop formal specifications for a broadband wireless access standard, known as WiMAX [12]. The wireless metropolitan area network would be an alternative to wired broadband access such as cable or DSL. With the opening of the W-band by the Federal Communication Commission (FCC) for broadband mm-wave
technologies [13], the prospect of implementing high speed, point-to-point links for the WiMAX backhaul network seems highly attractive (Figure 1.3). With 13GHz of available bandwidth (71-76, 81-86 and 92-95 GHz), multi-gigabit rates could be achieved with simple, cost effective architectures. Moreover, the pencil beam nature of the W-band transmission allows networks to operate in proximity without fear of interference.

![Figure 1.3: Point-to-point WiMAX backhaul links.](image)

1.2 Noise and Linearity in Cascaded Systems

The systems described in 1.1 are comprised of smaller cascaded blocks. For instance, the receiver chain includes the LNA, down-conversion mixer and IF amplifier. The overall performance of the system can be estimated from the noise and linearity characteristics of the building blocks.

The noise factor (F) is defined as the ratio of the signal-to-noise-ratio (SNR) at the input to the SNR at the output of a two-port network. On a logarithmic scale, this ratio is referred to as noise figure (NF).
\[ F = \frac{SNR}{SNR_0}, \quad NF = 10 \times \log_{10}(F) \]  

(1.4)

While the noise figure limits the minimum detectable signal, the distortion arising from the inherent non-linearity of the circuit sets the upper bound. In large signal operation, a power series expansion of the transfer characteristics, rather than a linear model, is needed to study the non-linear effects of the circuit [14].

\[ v_{OUT} = c_0 + c_1 v + c_2 v^2 + ... \]  

(1.5)

Although not repeated here, it can be shown that the response of the circuit to a sinusoidal excitation contains the fundamental frequency term, as well as second and third order harmonics caused by quadratic and cubic terms in the transfer characteristic. For a band-pass system, such as a tuned amplifier, n\textsuperscript{th} order harmonics that are at much higher frequencies relative to the fundamental lie far out of the band of interest and are of little importance. In the case of two sinusoidal inputs at frequencies \( \omega_1 \) and \( \omega_2 \), the cubic term in the transfer characteristic gives rise to third-order inter-modulation components at \( 2\omega_1 - \omega_2 \) and \( 2\omega_2 - \omega_1 \) (Figure 1.4). If the input signals are close in frequency, the inter-modulation products could lie in band and cause distortions.

![Figure 1.4: Input and output spectrums for a two-tone test.](image)

The two common measures of linearity in a circuit are the third-order inter-modulation intercept (IP3) and the 1-dB compression point (\( P_{1dB} \)). Figure 1.5 shows the fundamental harmonic and the third-order inter-modulation term (IM3) versus input power on a logarithmic scale. The IM3 term is insignificant at low input power. However it grows with a slope that is three times that of the fundamental.
The input-referred IP3 is defined as the input power at which the power of the IM3 term is equal to that of the fundamental. Although the limitations of the circuit prevent the power of the IM3 term to reach the fundamental, the IP3 can be estimated from the linear extrapolation of the two curves. The input-referred 1-dB compression point is the input power where the gain of the circuit drops by 1 dB. The spurious-free dynamic range (SFDR), as the name implies, is defined as the signal to noise ratio, precisely when the IM3 power equals the noise floor (see Figure 1.5).

![Figure 1.5: Plot of the fundamental and third inter-modulation terms versus Input power.](image)

A system comprised of cascaded blocks, each characterized by the gain (G), the noise factor (F) and the linearity parameters (P_{1dB}, IIP3), can be represented by an equivalent stage as shown in Figure 1.6. The equivalent noise factor is given by:

\[ F_{eq} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \ldots + \frac{F_N - 1}{G_1G_2G_3\ldots G_{N-1}} \]  

(1.6)

It can be seen that the noise factor of the first stage directly adds to the equivalent noise factor, while the contribution of the subsequent stages is divided by the equivalent gain of the previous stages. Thus, in the case of a receiver, an LNA with sufficient gain and low noise can reduce the sensitivity of the system to the noise contribution of the subsequent stages.
The equivalent 1-dB compression point and the third-order inter-modulation intercept are given by:

\[
\frac{1}{P_{1dB,EQ}} = \frac{1}{P_{1dB,1}} + \frac{G_1}{P_{1dB,2}} + \frac{G_1G_2}{P_{1dB,3}} + \ldots + \frac{G_1G_2G_3\ldots G_{N-1}}{P_{1dB,N}} \tag{1.7}
\]

\[
\frac{1}{\text{IIP3}_{EQ}} = \frac{1}{\text{IIP3}_1} + \frac{G_1}{\text{IIP3}_2} + \frac{G_1G_2}{\text{IIP3}_3} + \ldots + \frac{G_1G_2G_3\ldots G_{N-1}}{\text{IIP3}_N} \tag{1.8}
\]

While not as straight forward to derive as the noise factor case, the expressions do indicate that the equivalent linearity of the system is mostly constrained by the linearity of the final stage, due to the fact that the signal at the input of the final stage has already been considerably amplified by the previous stages.

### 1.3 Technology Overview

The circuits described in this thesis were fabricated in STMicroelectronics’ digital 65-nm CMOS process with standard 7-layer Cu back-end. Both LP and GP transistors are available on the same die. However, because GP transistors exhibit 20-30% higher \(g_m\) and \(f_T\), and lower \(V_T\), they were used exclusively in all circuits.

Measurements of transistor test-structures, conducted by my colleague Alexander Tomkins, show peak \(f_T\) of 185GHz for an 80\(\mu\)m General Purpose (GP) NMOS biased at 0.3mA/\(\mu\)m to 0.35mA/\(\mu\)m, with \(V_{DS} = 0.7V\) (Figure 1.7).
Figure 1.7: Measured $f_T$ of the GP NMOS transistor versus current density ($V_{DS} = 0.7V$).

Figure 1.8: Measured $f_T$ of the GP NMOS transistor versus $V_{DS}$ ($V_{GS} = 0.7V$).

Figure 1.8 shows the measured $f_T$ of the same transistor versus $V_{DS}$, with $V_{GS} = 0.7V$. The results indicate that cascading more than two transistors in 65nm CMOS would seriously degrade the high-frequency performance of the transistors. Finally, the maximum available power gain (MAG) of the GP NMOS transistor is shown in Figure 1.9. The transistor has a MAG of 8.4dB at 94GHz. The glitch observed in the measurement is due to the fact that the measurement range of the VNA has been extended from 57GHz to 94GHz with HF modules. The glitch occurs as the VNA switches from one frequency range to the other.

Figure 1.9: Maximum available power gain of the GP NMOS.
## 2 Low Noise Amplifier

The overall noise figure, and thus the sensitivity of a receiver depend primarily on the gain and noise performance of the first amplification stage. An LNA with high gain and low noise can reduce the sensitivity of the system to the noise contribution of the subsequent stages. The amplifier also needs to be linear so as to limit the inter-modulation tones that lie in band. Other performance metrics contributing to the figure of merit of an LNA (given below) are center frequency ($f$) and power consumption ($P$) [15].

$$FOM_{LNA} = \frac{G \times IIP_3 \times f}{(F-1) \times P} \quad (2.1)$$

The input impedance of the LNA needs to be matched to the source impedance so as to maximize power gain. In addition to that, the stability factor of the amplifier should also be considered to prevent oscillation.

### 2.1 Simultaneous Noise and Input Impedance Matching

The noise of any two-port network can be modeled by an equivalent series noise voltage and shunt noise current (Figure 2.1) placed at the input of the 2-port [16].

![Figure 2.1: Equivalent 2-Port representation of a noisy system.](image)
The noise factor of the two-port network is given by [16]:

$$F = \frac{i_n^2 + |i_n + Y_s e_n|^2}{i_n^2}$$  \hspace{1cm} (2.2)

In order to take into account the correlation between the two noise sources, the shunt noise current is typically written as the sum of correlated and un-correlated terms. The correlated noise current is related to the noise voltage through the correlation admittance, $Y_{cor}$. The remaining independent noise sources, as well as the signal source noise, can also be represented as thermal noise generated by equivalent noise resistance or noise conductance.

$$i_n = i_c + i_u$$  \hspace{1cm} (2.3)

$$i_c = Y_s e_n$$  \hspace{1cm} (2.4)

$$R_n = \frac{e_n^2}{4kT \Delta f}$$  \hspace{1cm} (2.5)

$$G_u = \frac{i_u^2}{4kT \Delta f}$$  \hspace{1cm} (2.6)

$$G_s = \frac{i_s^2}{4kT \Delta f}$$  \hspace{1cm} (2.7)

One can find the minimum achievable noise figure by substituting the above equations into (2.2) and taking the derivative with respect to the real and imaginary parts of the source admittance. The noise factor equation can now be written as:

$$F = 1 + \frac{R_n}{G_s} |Y_c + Y_s|^2 + \frac{G_u}{G_s} = F_{MIN} + \frac{R_n}{G_s} |Y_s - Y_{s opt}|^2$$  \hspace{1cm} (2.8)

Thus for a certain optimum source impedance, the noise factor of the two-port is reduced to the minimum noise factor. However, since the source impedance in RF applications is typically set to 50Ω, one must design the amplifier such that the optimum source impedance equals 50Ω.
The most commonly used LNA topologies are the common source (CS) and the cascode shown in Figure 2.2. The popularity of these topologies, implemented with series-series feedback, is due to the fact that a unique, optimal solution exists that simultaneously matches the input and noise impedances of the stage to $50\ \Omega$ \cite{17}. The noise impedance matching is accomplished by sizing the input stage transistors, i.e. changing $g_{\text{meff}}$ in (2.9), and biasing it at the minimum noise figure current density.

$$R_{\text{opt}} = R_S + R_G + \frac{k_2}{\omega(C_{GS} + C_{GD})} \approx R_S + R_G + \frac{k_2 f_{\text{eff}}}{f \times g_{\text{meff}}}$$ \hspace{1cm} (2.9)

The input impedance is matched by gate and source inductors.

$$Z_{\text{in}} = R_S + R_G + \omega f_{\text{eff}} L_S + j \omega(L_S + L_G) - j \omega \frac{\omega}{\omega \times g_m}$$ \hspace{1cm} (2.10)

In (2.9) and (2.10) $f_{\text{eff}}$ and $g_{\text{meff}}$ denote the effective unity gain cutoff frequency and transconductance of the entire stage. They both depend on the drain current density and can be obtained from transistor simulations or more accurately from measurements, and include the effect of parasitic source resistance $R_S$. Parameter $k_2$, approximately 0.5, characterizes the noise of the MOSFET \cite{18}.
Common-source and cascode topologies without feedback, i.e. with $L_S = 0$ in (2.10), as well as common-gate ones cannot achieve simultaneous noise and impedance matching, except by accident, at a single frequency.

As discussed in [17], at mm-wave frequencies the pad capacitance introduces an additional parallel resonant at the input of the series-series feedback LNA. This is illustrated in Figure 2.3.

Therefore matching the input and noise impedance over a broad bandwidth would be more problematic with series-series feedback topology.

Alternatively, a shunt-series reactive feedback topology that would simultaneously compensate the pad capacitance and the input capacitance of the transistor over a broader bandwidth at millimeter-wave frequencies could be employed instead. Such a topology was recently proposed in [19] for the 3-10 GHz range (UWB applications). Figure 2.4 shows the equivalent circuits describing the input and noise impedance of the transformer-feedback LNA. With first order approximation, which ignores $R_G$, $R_S$ and assumes that the coupling co-efficient is equal to one, the input equivalent circuit simplifies to a single parallel-resonance. Therefore this feedback scheme is expected to yield a broader match at the input.
The expressions for the optimum noise impedance and the minimum noise figure, as well as the step-by-step algorithmic design methodology are described for each LNA in the following sections.

### 2.1.1 Inductive-Feedback LNA

The expressions for the optimal noise impedance and the minimum noise figure of this amplifier can be derived using the noise impedance formalism and Z-matrices [18, 20].

\[
Z_{sopt} = \sqrt{\frac{R_{sopt}^2}{G_{na}} + 2G_{corf}R_{corf}(Z_{11f}) + 2R_{corf}(Z_{11f})^2 + \frac{|Z_{corf} - Z_{11f}|^2}{G_{na}} + j[X_{sopt} - \Im(Z_{11f})]} 
\]

(2.11)

\[
F_{MIN} = 1 + 2G_{na}[R_{corf} + R_{sopt} + \Re(Z_{11f})]
\]

(2.12)

Where the parameters of the amplifier (i.e. MOS cascode) are shown with the subscript “a” and the parameters of the feedback network are shown with subscript “f”. For the feedback network consisting of inductors \(L_G\) and \(L_S\) with loss resistors \(R_{LG}\) and \(R_{LS}\) respectively:

\[
G_{nf} = 0, R_{nf} = R_{LG} + R_{LS}, Z_{corf} = 0, Z_{11f} = R_{LG} + R_{LS} + j\omega(L_S + L_G), Z_{12f} = j\omega L_S
\]

(2.13)

If \(L_G\) and \(L_S\) are ideal (infinite Q), then (2.13) becomes:

\[
G_{nf} = 0, R_{nf} = 0, Z_{corf} = 0, Z_{11f} = j\omega(L_S + L_G), Z_{12f} = j\omega L_S
\]

(2.14)
Therefore the noise-figure of the noise-matched LNA is identical to the minimum noise-figure of the MOS cascode. By substituting (2.14) in (2.11), the real part of the optimal noise impedance can be derived to be equal to that of the main amplifier. Only the imaginary part changes due to presence of \( L_G \) and \( L_S \). One can conclude that loss-less feedback does not change the optimum noise resistance \( R_{sopt} \) and thus noise impedance matching can only be achieved by transistor sizing. The following is a step-by-step design methodology for the inductive-feedback LNA as described in [17].

**Step 1:** Size the transistor for \( R_{sopt} = 50\Omega \) according to (2.9).

\[
N_f = \frac{1}{Z_0} \left[ R_G(W_f) + \frac{R_S'}{W_f} + \frac{k_z f_{T_{eff}}}{f \times g_{meff} W_f} \right] = \frac{1}{50} \left[ \frac{200}{200} + \frac{200}{1} + \frac{0.5 \times 100 \text{GHz}}{80 \text{GHz} \times 1.1 \text{mS} \times 1} \right] = 19.4 \approx 20
\]

Where \( W_f \) is the finger width and \( R_S' \) is the source resistance per unit gate width.

**Step 2:** Calculate the bias current in the first cascode stage, assuming \( J_{opt} = 0.25 \text{mA/\mu m} \).

\[
I_{DS} = J_{opt} W_G = 0.25 \frac{mA}{\mu m} \times 20 \mu m = 5 mA
\]

**Step 3:** Find \( L_S \) for input resistance matching, according to (2.10).

\[
L_S = \frac{Z_0 - R_G - R_S}{2\pi f_{T_{eff}}} = \frac{50 - (200 / 20) - (200 / 20)}{2\pi \times 100 \times 10^9} = 48 \text{pH}
\]

**Step 4:** Find \( L_G \) to cancel the imaginary part of the input noise impedance, according to (2.10).

\[
L_G + L_S = \frac{\omega_{t_{eff}}}{(2\pi f)^2 W_G g_{meff}} = \frac{2\pi \times 100 \times 10^9}{(2\pi \times 80 \times 10^9)^2 \times 20 \mu m \times 1.1 \frac{mS}{\mu m}} = 113 \text{pH}, L_G = 65 \text{pH}
\]

### 2.1.2 Transformer-Feedback LNA

The expressions for the optimal noise impedance and the minimum noise figure of the transformer-feedback amplifier can be derived using the noise admittance formalism and G-matrices [18]. The G-matrix entries of the transformer-feedback network can be written as:
\[ g_{11f} = -\frac{j}{\omega L_p} + G_p, \quad g_{12f} = \frac{M}{L_p}, \quad g_{21f} = -\frac{M}{L_p}, \quad g_{22f} = j\omega L_{SEC}(1-k^2) + R_{SEC} \]  

Where \( L_p \) is the inductance of the primary, \( L_{SEC} \) is the inductance of the secondary, \( k \) is the coupling factor, and \( M \) is the mutual inductance of the transformer. \( G_p \) and \( R_{SEC} \) are the loss conductance of the primary and loss resistance of the secondary, respectively. As derived in the Appendix A, if the imaginary part is tuned out by the parallel inductance of the transformer primary, the input conductance of the amplifier with feedback can be written as:

\[ G_{IN} = \frac{M}{L_p} + G_p \]  

The input resistance of the transformer-feedback LNA, Similar to the case of the inductive-feedback LNA, does not vary with frequency and is a function of the feedback network parameters: \( L_p, \) \( L_{SEC} \) and \( M. \) However, it does depend on the MOS transconductance, \( g_{\text{meff}}. \)

The expressions for the optimal noise admittance and the minimum noise figure of the amplifier with feedback are derived in the Appendix A as:

\[ Y_{\text{opt}} = \sqrt{G^2_{\text{opta}} + \frac{G_{\text{opta}}}{R_{\text{na}}} + 2G_{\text{cota}} \Re(g_{11f}) + \Re^2(g_{11f}) + \frac{R_{\text{na}}}{R_{\text{na}}}} + j|B_{\text{opta}} - \Im(g_{11f})| \]  

\[ F_{\text{MIN}} = 1 + 2R_{\text{na}}[G_{\text{cota}} + G_{\text{opta}} + \Re(g_{11f})] \]  

If the transformer is lossless \((G_p = 0, R_{SEC} = 0)\), then:

\[ R_{nf} = 0, G_{nf} = 0, Y_{\text{opta}} = 0, \Re(g_{11f}) = 0 \]  

And \( G_{\text{opt}} \) (2.17) and \( F_{\text{MIN}} \) (2.18) of the amplifier become identical to those of the MOS cascode.

\[ R_{n} = R_{na}, G_{u} = G_{ua}, Y_{\text{cor}} = Y_{\text{cota}} \]  

\[ Y_{\text{opta}} = G_{\text{opta}} + j(B_{\text{opta}} + \frac{1}{\omega L_p}) \]
Therefore, despite the different topologies employed for their input stage, the two LNAs exhibit similar flexibility in adjusting the optimal noise resistance (conductance), from $g_{meff}$, and the input resistance (conductance), from $L_{SEC}$ and $L_{P/M}$, respectively. Although (2.21) and (2.22) ignore the parasitic resistance of the MOS and the finite $Q$ of the transformer, they can be accounted for in an analytical manner, as shown in the Appendix A. The following is a step-by-step design methodology for the transformer-feedback LNA, similar to the one developed for the inductive-feedback LNA in [17].

**Step 1:** Size the transistor for $R_{s opt} = 50 \, \Omega$ according to (2.9).

$$N_f = \frac{1}{Z_0} \left[ R_G(W_f) + \frac{R_s}{W_f} + \frac{k_2 f_{reff}^2}{f g_{meff} W_f} \right] = \frac{1}{50} \left[ 200 + \frac{200}{1} + \frac{0.5 \times 100 GHz}{80 GHz \times 1.1 mS \times 1} \right] = 19.4 \approx 20$$

Where $W_f$ is the finger width and $R_s'$ is the source resistance per unit gate width.

**Step 2:** Calculate the bias current in the first cascode stage, assuming $J_{opt} = 0.25 mA/\mu m$.

$$I_{DS} = J_{OPT} W_G = 0.25 \frac{mA}{\mu m} \times 20 \mu m = 5 mA$$

**Step 3:** Determine $L_p$ for input susceptance cancellation from (A.17) in Appendix A.

$$L_p = \frac{1}{\omega^2 \left( C_{PAD} + \frac{g_{meff}}{\omega_{reff}} \right)} = \frac{1}{(2\pi \times 80 \times 10^9)^2 \times \left( 20 fF + \frac{22 mS}{2\pi \times 100 \times 10^9} \right)} = 72 \, pH$$

**Step 4:** Find $M/L_p$ for input conductance matching from (2.16), assuming a $Q$ of 10 for the primary and a pad capacitance of 20fF.

$$G_p = \frac{1}{\omega L_p Q} = \frac{1}{2\pi \times 80 \times 10^9 \times 72 \times 10^{-12} \times 10} = 2.8 mS$$

$$M = \frac{Z_u - G_p}{g_{meff}} = \frac{20 mS - 2.8 mS}{22 mS} = 0.78$$
2.2 80GHz Low Noise Amplifier

Figure 2.5 shows the schematic of the 80GHz LNA with transformer-feedback and inductive-feedback (inset) input stages. Each LNA consists of three cascode stages. Except for the feedback network at the input stage, all the bias currents and component values are identical in all stages for the two LNAs.

![LNA schematic with transformer-feedback and inductive-feedback (Inset).](image)

With the exception of M/L_P, all component values derived for the first stage in the previous section are very close to the final values determined by simulation, indicating that a fairly accurate initial hand-design is possible even at 80GHz. Although the hand analysis provides good initial values, the design methodology described earlier is most effectively conducted by simulation. To avoid iterations in the design of the transformer, the transistor (cascode) must be replaced by the extracted layout to account for parasitic effects.

Note that the transformer-feedback LNA has an extra element of freedom through L_SEC or k, making the design more complicated than the inductive-feedback LNA. By choosing a smaller inductance for the secondary, the (current) gain of the amplifier stage is increased. However, the lowest value of L_SEC is limited by the power gain and the current gain of the transistor itself at
80-90GHz, and is also constrained by the inductance of the primary, the coupling coefficient (k) and layout. The gain in the first stage of both LNAs is set by the Q and inductance, respectively, of the drain inductor of M2.

The second and third stages have no inductive degeneration so as to maximize gain. All stages are biased at 0.25mA/μm. This value was experimentally found to give the best overall noise figure (Figure 2.17).

The inductor used between the CS and the CG transistors in each stage (L_M in Figure 2.2) forms an artificial transmission line along with the parasitic capacitances at the two end nodes. This bandwidth extension technique results in higher gain and lower NF for the cascode stage [18]. Figure 2.6 shows the simulated $f_T$ and $NF_{MIN}$ of the 20μm cascode stage versus the broad-banding inductor value. The 180pH inductor has been chosen to achieve a compromise between maximum gain and minimum noise figure. The broad-banding inductor value can be determined for each stage in a similar fashion. Note that wider transistors in the second and third stages contribute bigger parasitic capacitance and thus require smaller inductors.

![Figure 2.6: Simulated $f_T$ and $NF_{MIN}$ of the 20μm cascode stage versus the broad-banding inductor ($L_M$).](image)

The load inductor in each stage has been chosen to resonate with the parasitic capacitance at the drain node of the CG transistor according to (2.23).

$$L_D = \frac{1}{(2\pi \times f)^2 C_{OUT}} \quad (2.23)$$
This parasitic capacitance consists of the parasitic capacitance of the CG transistor \((C_{DB} + C_{GD})\) and the loading of the next stage (the AC coupling capacitor in series with the gate capacitance of the next stage). For the first stage, the load inductor can be found to be:

\[
C_{OUT} = (C_{DB2} + C_{GD2}) + \left(\frac{C_{AC} \times C_{GS3}}{C_{AC} + C_{GS3}}\right) \approx 48 \text{fF}
\]

\[
L_D = \frac{1}{(2\pi \times 80\text{GHz})^2 C_{OUT}} = 82 \text{pH}
\]

The initial guess is very close to the value determined by simulation.

The transistors in the LNA have 1\(\mu\)m finger width with minimum gate length, and are contacted on one side of the gate. The source and drain diffusion regions are contacted in a tapered fashion so as to minimize side-wall capacitance between source and drain contacts (See Figure 2.7).

![Figure 2.7: Transistor layout (left) and source and drain metallization (right).](image)

The gate resistance and source resistance are approximately 200\(\Omega\) per finger and the effective transconductance is about 1.1mS/\(\mu\)m at a drain current density of 0.25mA/\(\mu\)m. The \(f_{\text{Teff}}\) of the cascode with inductive broadbanding is 100GHz, which according to (2.9) results in an optimal noise resistance of 50\(\Omega\) at 85-90GHz for a 20-\(\mu\)m cascode stage.
2.2.1 Passive Component Design

The inductors employed in the LNAs were designed in ASITIC [21]. They typically consist of 1.5 to 2.5 windings in top metal with lower level metal under-pass. The Y-parameters of the inductor are simulated in ASITIC. The 2-π equivalent circuit parameters can be extracted from the Y-parameters at low frequency [22], while the skin effect parameters can be extracted by fitting the inductance vs. frequency and Q vs. frequency curves. Figure 2.8 shows the layout and the 2-π equivalent circuit for an 80pH inductor. Figure 2.9 shows the measured and simulated inductance and quality factor of the 80pH inductor. There is less than 3pH discrepancy between the simulated and the measured effective inductance, which indicates high accuracy in inductor modeling. The high quality factor values of 15 to 20 provide evidence that high-Q passive design is possible with the regular digital back-end even at W-band frequencies.

![Figure 2.8: Layout of the 80pH inductor (left) and the 2-π equivalent circuit (right).](image)

![Figure 2.9: Simulated and measured inductance and quality factor of the 80-pH inductor.](image)
The 2:1 vertically stacked transformer employed in the transformer-feedback LNA was designed to achieve $k = 0.55$, $L_P = 70\,\text{pH}$ and $L_{SEC} = 35\,\text{pH}$. The primary has 2 windings in M6, with the over-pass in M7, and a diameter of 24$\mu$m. The windings are 3$\mu$m wide and spaced by 2$\mu$m. The secondary has a single, 2$\mu$m wide turn in M5.

The parasitic parameters of the primary and the secondary are extracted from simulated Y-parameters, while the capacitance between the primary and the secondary, as well as the coupling coefficient is determined directly from ASITIC “pix” command at 0.1GHz. Figure 2.10 shows the layout and 2-$\pi$ equivalent circuit for the 2:1 transformer.

The AC coupling capacitors are realized using the Metal-Oxide-Metal capacitors available from the design kit.

![Figure 2.10: 2:1 Transformer layout (left) and the 2-$\pi$ equivalent circuit (right).](image)

### 2.3 Experimental Results

This section presents the measurement results of the 80GHz LNA test structures and of the W-band down-converter which integrates the transformer-feedback LNA with Keith Tang’s double-balanced Gilbert-cell mixer.
2.3.1 80GHz LNA Test Structure Measurements

Figure 2.11 shows the die microphotograph of the inductive-feedback and transformer-feedback LNA test structures. The 2:1 transformer is indicated on the die photo of the transformer-feedback LNA. 0.5pF local de-coupling capacitors are employed on the VDD and VBIAS planes.

S-parameters of the two LNAs were measured on wafer using a 94GHz Wiltron 360 Vector Network Analyzer (VNA). The 20-fF pad capacitance has not been de-embedded from any of the circuit measurements.

The measured and simulated $S_{21}$, $S_{11}$ and NF$_{50}$ for the two LNAs are plotted in Figure 2.12 at the nominal supply of 1.5V. The simulation results include the pad capacitance and the RC parasitic effects captured by extracted layout at the cell level. The inductive-feedback and transformer-feedback LNAs have 13dB and 13.5dB gain respectively, centred at 80GHz. The 3dB bandwidth of the transformer-feedback LNA extends from 72GHz to 90GHz. The measured noise figure of the transformer-feedback LNA is systematically lower by 0.3-0.6dB and varies between 6.4dB and 8.4dB in the 75-88GHz band. The 2dB ripple in the measured noise figure is due to the variation of the noise source reflection coefficient between cold and hot states. The peaks and troughs occur at exactly the same frequencies for both LNAs. The $S_{11}$ of the transformer-feedback LNA is as low as -30dB at 87GHz and remains below -20dB from
80GHz to 90GHz. The agreement between measurement and simulations is reasonably good. The measured peak gain and noise figure are about 2.5dB below and 2dB above simulation, respectively.

Figure 2.12: Measured and simulated $S_{21}$, $S_{11}$ and NF for the inductive-feedback LNA (left) and the transformer-feedback LNA (right).

The real and imaginary parts of the input impedance are plotted in Figure 2.13 for both LNAs. The results show broader matching for the transformer-feedback LNA. The real part of the input impedance of the inductive-feedback LNA is 25-30Ω in the band of interest. According to (2.10), in order to achieve 50Ω matching we need to increase the degeneration inductance ($L_s$). However, increasing $L_s$ would in turn reduce the power gain of the first stage, which results in lower overall gain and higher noise figure. This shows the superiority of the transformer-feedback matching scheme. The $S_{21}$ of the transformer-feedback LNA, measured across 5 dies, shows 0.5dB variation, indicating excellent repeatability over process variation, as shown in Figure 2.14.
The measured gains (S21), noise figure (NF) and input return loss (S11) of both LNAs are plotted versus the supply voltage in Figure 2.15. At 1.2V supply, the inductive-feedback LNA and the transformer-feedback LNA have 10.5dB and 11dB gain respectively. Figure 2.16 plots the peak gain versus current density of the first stage transistor for the transformer-feedback LNA. The gain peaks at roughly 0.3mA/μm, which coincides with the peak fT current density in this technology. The noise figure of the transformer-feedback LNA at 81GHz versus current
density of the first stage transistor is plotted for different supply voltages in Figure 2.17. The minimum noise figure current density changes from 0.15mA/μm for $V_{DD} = 1V$ ($V_{DS} = 0.5V$) to 0.28mA/μm for $V_{DD} = 1.8V$ ($V_{DS} = 0.9V$). These results confirm the findings in [23] indicating that at scaled $V_{DS}$ ($V_{DS}$ decreasing by the technology scaling factor “S” from node to node), the minimum noise figure current density remains constant across frequency and technology nodes.

![Figure 2.16: Transformer-feedback LNA gain versus the current density of the first stage transistor.](image1)

![Figure 2.17: Transformer-feedback LNA noise figure versus the current density of the first stage transistor for different supply voltages.](image2)

The measured P1dB of the transformer-feedback LNA is -15.1dBm at 80GHz, as shown in Figure 2.18.

It is important to note that large signal measurements are prone to +1dB/-1dB error and therefore for accurate gain measurements, only small signal (S-parameter) measurements can be trusted.

![Figure 2.18: 1dB Compression point of the transformer-feedback LNA.](image3)
The following table summarizes the performance of the 80GHz transformer-feedback LNA.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.5V Nominal</td>
</tr>
<tr>
<td>Centre Frequency</td>
<td>80GHz (3dB: 72GHz to 90GHz)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>30mW</td>
</tr>
<tr>
<td>Gain (@ Centre Frequency)</td>
<td>13.5dB</td>
</tr>
<tr>
<td>NF</td>
<td>6.4dB – 8.4dB</td>
</tr>
<tr>
<td>P1dB</td>
<td>-15.1dB</td>
</tr>
<tr>
<td>Chip Size</td>
<td>490µm×300µm (Core: 120µm×170µm)</td>
</tr>
</tbody>
</table>

### 2.3.2 W-band Down-Converter

The transformer-feedback LNA, along with the mixer designed by Keith Tang and presented in [24] were integrated into a 75-90GHz down-converter front-end. The down-converter features the single-ended LNA, a double-balanced Gilbert-cell mixer and differential IF amplifier for driving 50Ω loads (See Figure 2.19).

Dual coil, vertically stacked, 1:1 transformers are used at the LO port and as the load of the last stage of LNA for single-ended to differential conversion. The transformer centre-taps are used to bias the mixer. The measured $S_{21}$, $S_{11}$ and $S_{22}$ of the transformer are shown in Figure 2.20. The transformer has 2dB loss in the 70GHz to 90GHz range. In this implementation, the clock signal is provided by the external source.

Figure 2.21 shows the down-converter chip microphotograph. The receiver chip occupies 460µm×500µm including pads. The differential down-conversion gain and the Double Side Band (DSB) noise figure of the down-converter at 1GHz IF, along with the $S_{11}$ of the LNA are shown in Figure 2.22.
Figure 2.19: Block diagram of the W-band down-converter.

Figure 2.20: Measured $S_{21}$, $S_{11}$ and $S_{22}$ of the 1:1 transformer.

Figure 2.21: Die photo of the W-band down-converter.

Figure 2.22: Down-converter gain, NF and LNA $S_{11}$ versus RF frequency.
The down-converter has a peak gain of 13dB centred at 80GHz, with the 3dB bandwidth extending from 75GHz to 90GHz. The DSB noise figure of the down-converter is 8.5dB to 10dB at 1GHz IF frequency over the entire RF bandwidth. The down-conversion gain and DSB noise figure were also measured versus IF frequency with the LO frequency set to 89GHz, shown in Figure 2.23 and Figure 2.24. The gain is 12dB at 1GHz IF frequency and the 3dB bandwidth is 9GHz. The DSB NF is 7dB to 9dB in the entire measurement range. The measured compression point of the down-converter is shown in Figure 2.25 for the RF input of 80GHz, and the LO signal at 75GHz. The input-referred 1dB compression point is -16.2dBm.

Table 2.2 summarizes the performance of the W-band down-converter.
Table 2.2: Performance summary of the W-band down-converter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.5V Nominal</td>
</tr>
<tr>
<td>RF Bandwidth</td>
<td>75GHz – 90GHz</td>
</tr>
<tr>
<td>IF Bandwidth</td>
<td>9GHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>67mW (42mW in LNA and Mixer)</td>
</tr>
<tr>
<td>Gain (@ Centre Frequency)</td>
<td>13dB</td>
</tr>
<tr>
<td>NF</td>
<td>8.5dB – 10dB</td>
</tr>
<tr>
<td>P1dB</td>
<td>-16.2dBm</td>
</tr>
<tr>
<td>Chip Size</td>
<td>460μm×500μm</td>
</tr>
</tbody>
</table>

Figure 2.25: Down-converter 1dB compression point.
3 W-band IQ Receiver

This section describes the design of an 85GHz to over 100GHz IQ receiver. This receiver is intended to demonstrate the feasibility of an image-reject architecture, and to verify the quadrature operation of the VCO presented in [1]. The need for an image-reject architecture stems from the fact that in regular heterodyne down-conversion, the Lower Side-Band (LSB) and Upper Side-Band (USB) channels down-convert to the same IF frequency. Thus if the desired information lies in the USB, any interferers in the LSB would corrupt the down-converted signal, and vice versa (Figure 3.1).

![Figure 3.1: Corruption of down-converted output due to image signal in heterodyne receiver.](image)

The proposed image-reject architecture is based on the Hartley receiver shown in Figure 3.2. Effective lower-side (or upper-side) rejection depends on quadrature LO generation and on excellent matching between the two Gilbert-cells making up the IQ mixer.

![Figure 3.2: Hartley image-reject architecture.](image)
The Image-Rejection Ratio (IRR), defined by the image-to-signal ratio at the output divided by the image-to-signal ratio at the input, is limited by phase and amplitude mismatch introduced by clock signals and any un-symmetry and mismatch in circuit design. It can be shown that IRR is related to amplitude mismatch ($\Delta A/A$ in V/V) and phase mismatch ($\theta$ in radians) by [14]:

$$ IRR = \frac{(\Delta A / A)^2 + \theta^2}{4} $$

(3.1)

Figure 3.3 plots the IRR (quoted in dB as a positive number) versus amplitude in a family of curves corresponding to phase mismatch of 2 to 10 degrees. An IRR of 20dB can be achieved by allowing for amplitude mismatch of no more than 10% and phase mismatch of no more than 10 degrees.

Phase mismatch in the LO signal would directly translate to phase mismatch in the output signal. Moreover, poor mixer design, which could result in unsymmetrical loading of the VCO, can also contribute to output phase mismatch. In a similar way, output amplitude mismatch could be caused by amplitude mismatch in the quadrature LO signals and mismatch present in mixer circuits (which lead to gain mismatch). The VCO integrated in this work is designed by my colleague Katya Laskin and presented in [1]. Design methodology for the quadrature VCO is out of the scope of this work. This thesis is focused on the design of the IQ mixer.
Figure 3.4 shows the block diagram of the IQ receiver. The receiver features the single-ended LNA, double-balanced, Gilbert-cell IQ mixer, two IF amplifiers to drive 50Ω loads and the quadrature VCO presented in [1] with single-ended LO buffers. 1:1 transformer is used as the load of the last stage of LNA for single-ended to differential conversion. Transformers have also been used between the LO buffers and the mixers so as to present the same loading to the VCO as in the case of the receiver in [1]. The receiver has been designed to operate from 1.2V supply.

Operating at 15% higher frequency, the low noise amplifier used in the IQ receiver has been slightly modified from the 80GHz transformer-feedback LNA presented in Section 2. Its schematic is shown in Figure 3.5. The layout of the transistors in the LNA was changed from single-side gate contacts to double-side gate contacts to maximize gain and minimize NF (see Figure 3.6). Metal-Insulator-Metal (MIM) capacitors were used in place of MOM capacitors. The load inductors were reduced to increase the centre frequency of the LNA. Since this 85GHz-100GHz LNA was also integrated in W-band receiver and transceiver phased arrays (not included in this thesis), its second and third stages were modified to present a 75Ω real impedance to the phase shifter. The new compact layout shown in Figure 3.7 is optimal for realizing large arrays that occupy small die area.

![Figure 3.4: Block diagram of the IQ receiver.](image-url)
Figure 3.5: Schematic of the modified transformer-feedback LNA.

Figure 3.6: Transistor layout with double-sided gate contacts.

Figure 3.7: Layout of the modified transformer-feedback LNA.
3.1 IQ Mixer Design

The IQ mixer consists of the RF differential transconductance pair, which is fed by the signal from the LNA, and two mixing quads, which are driven by the I and Q LO signals. The schematic of the mixer is shown in Figure 3.8. The 1:1 transformer at the output of the LNA converts the single-ended RF signal to differential format. The transformer primary acts as the load of the last stage of the LNA (see Figure 3.5). The centre-tap of the transformer secondary is used to bias the transistors in the transconductance pair, which are sized for minimum noise as in the LNA (20μm). The 100pH common-mode inductor suppresses even mode harmonics. The RF signal is coupled from the transconductor to the mixing quads using two 1:1 transformers. The mixing quad bias current is provided by a current source while their gate voltage is set through the centre-tap of the secondary of each transformer. This topology has the advantage of separating the biasing of the mixing quads and the transconductance pair (at the price of higher power consumption). Since the transistors are not cascaded, they can be biased separately, and have higher $V_{DS}$, which is important for the high-speed operation.

![Figure 3.8: Schematic of the IQ mixer.](image)

The transconductance pair is biased at 0.3mA/μm, which has been proven to be the sweet spot for linearity in CMOS circuits [25]. The gate width of the mixing quad FETs is 16μm, which minimizes power consumption and the LO power needed for proper mixer operation. The
reduction in current also allows for faster switching of the transistors and higher gain. The mixing quad transistors are biased at 0.15mA/μm for minimum noise and fast switching.

A perfectly symmetrical layout of the mixer is crucial to minimizing amplitude and phase mismatch, as needed for good image-rejection ratio. Layout symmetry was ensured by utilizing half-circuit cells, and by mirroring the cell in the final mixer layout. Figure 3.9 reproduces the die microphotograph of the IQ mixer.

![Chip microphotograph of the IQ mixer.](image)

Special attention was particularly paid to the layout of the mixing quad. Asymmetry in the layout cannot be completely eliminated due to the nature of the mixing quad. However, striving to reduce it improves the image rejection. The same layout approach could also be used for an up-conversion mixer, where layout symmetry minimizes LO to RF leakage. Figure 3.10 shows the layout of the mixing quad. Note that the transistors in each differential pair are inter-digitated in this design.

The differential IF amplifiers with a voltage gain of 1 are designed to drive the 50Ω loads with a bandwidth that exceeds 10GHz, as needed in high resolution passive imagers. The transistor size is 40μm for a current density of 0.25mA/μm provided by a current source.
Figure 3.10: Layout of the mixing quad.

Figure 3.11 shows the schematic of the amplifier, along with the off chip measurement and biasing scheme (shown in grey). This external biasing provides half of the current required to bias the 40μm transistors at 0.3mA/μm (for maximum linearity) while maintaining a $V_{DS}$ of 0.65V.

Figure 3.11: Schematic of the IF amplifier with external biasing.
The IQ receiver transient response (simulated with extracted models) with RF frequency at 89GHz and ideal quadrature LO signals at 99GHz (IF frequency at 10GHz) is shown in Figure 3.12. The RF input power is -20dBm and the LO power on each side is 0dBm. The LO signal power corresponds to the measured VCO output power presented in [1]. The plot shows the output quadrature signals superimposed on the RF signal.

![Figure 3.12: Transient response of the IQ receiver.](image)

The phase and amplitude mismatch corresponding to the IQ receiver (with ideal quadrature LO signals) were simulated with the Monte Carlo analysis based on process variation and mismatch in the circuit. The results are shown in Figure 3.13. The results indicate nominal amplitude mismatch of 4% and phase mismatch of 2.5 degrees (0.0436 radians). The nominal image rejection ratio can be calculated to be 30.6dB.

![Figure 3.13: Monte Carlo analysis of the amplitude mismatch (left) and phase mismatch (right).](image)
3.2 Experimental Results

This section presents the measurement results for the 85GHz-100GHz LNA test structure and of the 90GHz-100GHz IQ receiver.

3.2.1 LNA Test Structure Measurement Results

Figure 3.14 shows the die microphotograph of the LNA test structure. The chip measures $350\mu m \times 370\mu m$ (with a core active area of $200\mu m \times 80\mu m$). Figure 3.15 compares the measured and simulated $S_{21}$ and $S_{11}$ of the LNA. The peak gain is 11.7dB gain, centred at 91GHz-94GHz. The frequency range of the small signal measurement is inadequate to determine the upper 3dB frequency of the LNA. The $S_{11}$ is similar to that of the 80GHz LNA presented in Section 2, and is better than -15dB from 75GHz to 94GHz. Figure 3.16 shows the measured $S_{21}$ versus the supply voltage. The LNA gain remains higher than 9dB when the power supply voltage is reduced to 1V. The gain and linearity were measured from 75GHz to 100GHz using the large signal setup described earlier. Figure 3.17 shows the gain obtained from large signal measurements as a function of frequency, confirming the s-parameter results. The 3dB bandwidth of the LNA extends from 80GHz to beyond 100GHz. The measured 1dB input compression point of the modified LNA, measured at 90GHz, is -12.3dBm (Figure 3.18). The performance of the modified LNA is summarized in Table 3.1.

![Figure 3.14: Die photo of the modified LNA test structure.](image)
Table 3.1: Performance summary of the modified LNA.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2V Nominal</td>
</tr>
<tr>
<td>Centre Frequency</td>
<td>91GHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>24mW</td>
</tr>
<tr>
<td>Gain (@ Centre Frequency)</td>
<td>11.5dB</td>
</tr>
<tr>
<td>NF</td>
<td>Not Measured</td>
</tr>
<tr>
<td>P1dB</td>
<td>-12.3dBm</td>
</tr>
<tr>
<td>Chip Size</td>
<td>350μm×370μm (Core: 200μm×80μm)</td>
</tr>
</tbody>
</table>
3.2.2 IQ Receiver Measurement Results

The die microphotograph of the IQ receiver is shown in Figure 3.19. The chip measures 800μm × 510μm, including all pads. As described in Figure 3.11, one side of each I or Q output is terminated on chip. Therefore only the single-ended I and Q terminals of the receiver are monitored. The tuning range of the VCO was measured to be 97.2GHz to 101.2GHz. For the following measurements, the VCO frequency is set to 99GHz. The gain and linearity of the receiver was measured in the large signal setup. The differential down-conversion gain is plotted versus IF frequency in Figure 3.20 for 1.2V and 1.0V supply, with the LO frequency set to 99GHz.

The receiver has 10.5dB gain centred at 10GHz IF, which corresponds to 89 GHz RF frequency. This is to be expected since the modified LNA has a centre frequency of 91GHz-94GHz. The noise figure of the receiver was measured versus the IF frequency, with the LO frequency set to 99GHz. The results are shown in Figure 3.21. The receiver has 6.7dB to 8.5dB noise figure over the entire measurement band.

![Die microphotograph of the IQ receiver.](image.png)
Figure 3.22 shows the receiver DSB noise figure at 1GHz IF, versus the current density of the modified LNA. The minimum noise figure current density is 0.25mA/μm for 1.2V supply and 0.2mA/μm for 1V supply. Finally, the receiver 1dB compression point is plotted in Figure 3.23 for IF frequency of 1GHz. The input-referred 1dB compression point of the receiver is -13dBm.

In order to verify the quadrature operation of the receiver, it is necessary to operate the receiver at very low IF frequency (roughly 100MHz). This is due to the fact that the SMA cables that connect the IF ports to the measurement equipment can introduce appreciable phase at frequencies above 200MHz to 300MHz, despite having identical length. The setup shown in Figure 3.24 was used to assess the performance of the cables. In-phase signals are created using
a splitter, and fed to the DC-500MHz oscilloscope via identical SMA cables. The oscilloscope’s response to 100MHz signals are shown in Figure 3.25 (left). It can be seen that at 100MHz, the cables introduce minimal phase mismatch (less than 1 degree) and amplitude mismatch (less than 1%). However, as the frequency of the test signal is increased to 500MHz, as shown in Figure 3.25 (right), the phase mismatch and amplitude mismatch deteriorate to 5 degrees and 10.6% respectively.

![Figure 3.24: Setup used to verify SMA cables.](image)

Figure 3.24: Setup used to verify SMA cables.

The setup shown in Figure 3.26 was used to verify the operation of the IQ receiver. The VCO frequency is varied from 97.2GHz to 101.2GHz, while maintaining an IF frequency of 100MHz. The measurement results indicate that the VCO DOES NOT oscillate in quadrature. The IQ signals display 160 degrees to 170 degrees phase difference over the entire measurement band. Figure 3.27 shows the phase and amplitude mismatch of the receiver versus the LO frequency.
(IF = 100MHz). The response of the circuit at 98.6GHz LO frequency is shown in Figure 3.28. Therefore image rejection in this receiver has not been achieved. The modifications that are required to ensure the quadrature oscillation of the VCO are out of the scope of this thesis.

**Figure 3.26:** IQ receiver test setup.

**Figure 3.27:** Phase and amplitude mismatch of the receiver versus LO frequency.
The following table summarizes the performance of the IQ receiver.

**Table 3.2:** Performance summary of the IQ receiver.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>RF Bandwidth</td>
<td>80GHz – 100GHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>208mW</td>
</tr>
<tr>
<td>Gain (@ Centre Frequency)</td>
<td>10.5dB</td>
</tr>
<tr>
<td>NF</td>
<td>6.7dB – 8.5dB</td>
</tr>
<tr>
<td>P1dB</td>
<td>-13dBm</td>
</tr>
<tr>
<td>Chip Size</td>
<td>800μm × 510μm</td>
</tr>
</tbody>
</table>
4 80GHz Digitally Controlled Oscillator

Digitally Controlled Oscillators (DCO), realized using binary-weighted, digitally controlled MOS varactors have been demonstrated for mobile phones [26] and multi-GHz wireless applications [27]. This varactor topology yields a linear tuning curve, with the oscillation frequency determined by the digital word. With the implementation of a DCO, one can take advantage of the advanced digital CMOS technologies to realize a fully digital synthesizer.

Figure 4.1 shows the schematic of such a varactor with 7-bit digital control. Each varactor cell in the binary varactor bank is implemented as an Accumulation-mode NMOS (AMOS) varactor, which is a n-poly-thin-oxide capacitor. The AMOS varactor delivers a factor two capacitance variation as the binary control voltage drives the structure from accumulation to depletion [28]. To achieve good quality factor, the AMOS varactor cells have minimum gate length of 60nm, and the gate is contacted on both sides. The gate represents one port of the varactor, while the source and drain (shorted together) represent the second port, where the digital control is applied (Figure 4.2).

Alternatively, a digitally controlled varactor could be realized with binary weighted capacitors, controlled by switches (See Figure 4.3). The drawback of the latter topology is the series resistance of the switch (on the order of few ohms), which at high frequencies would seriously degrade the quality factor of the varactor.

![Figure 4.1: Differential, binary weighted varactor.](image1)

![Figure 4.2: Unit AMOS varactor cell.](image2)
4.1 Circuit Design

The DCO consists of the core Colpitts oscillator and the differential clock buffer. Figure 4.4 shows the schematic of the single-ended LC oscillator. It can be shown [14] that the small signal impedance seen at the gate of the oscillator consists of a negative real component, which is equal to:

\[ R_{NEG} = -\frac{g_m}{C_1 C_2 \omega^2} \]  

Therefore the structure shown in Figure 4.4 will oscillate given that the transistor has a \( g_m \) which is high enough to overcome the resistive loss of the LC tank. The frequency of oscillation depends on the tank inductor and capacitor and is given by [29]:

\[ \omega = \frac{1}{\sqrt{L_1 C_1 C_2}} \]
The phase noise of the oscillator is minimized by using a larger transistor with larger bias current, which maximizes the tank voltage swing, and reducing the tank inductor \( L_1 \) [30]. The tank voltage swing is given by [29]:

\[
V_{\text{osc}} = \frac{2I_{\text{dc}}L_1}{C_2R}
\]

(4.3)

Where \( R \) denotes the total loss resistance associated with the tank. This series resistance is assumed to be \( 5\Omega \) for the combination of the inductor and capacitor plus \( 200\Omega/\mu\text{m} \) of gate resistance.

Thus the design methodology starts by reducing \( L_1 \) as much as possible and increasing the \( C_1/C_2 \) ratio for maximum tuning range. A 40\( \mu \text{H} \) inductor has been chosen for this design. This value will ensure that any parasitic inductance introduced by additional interconnect would not dramatically alter the effective tank inductance and change the oscillation frequency.

The varactor cells have 0.8\( \mu \text{m} \) finger width. The smallest varactor cell is comprised of a single finger AMOS. Therefore to achieve 7\( B \) control, the largest cell is scaled to 64 fingers for a total varactor size of 128 fingers. Transistor measurements show a maximum capacitance of 80\( \text{fF} \). Based on a typical 2:1 capacitance ratio, the minimum value of the varactor capacitance is assumed to be half that value. Therefore the varactor capacitance range is determined to be 40\( \text{fF} \) to 80\( \text{fF} \). \( C_1 \) and transistor sizes can now be determined to ensure that the lower bound of the oscillation frequency (corresponding to maximum varactor capacitance) is 80GHz.

In a real circuit, the parasitic capacitances introduced by the transistor and passives would affect the oscillation frequency. Therefore (4.2) needs to be modified to account for the effect of these parasitic capacitances, shown in Figure 4.5. In Figure 4.5, \( C_{\text{GS}} \) and \( C_{\text{GD}} \) are the parasitic capacitances of the MOSFET and \( C_{\text{B}} \) includes the source-to-bulk capacitance of the MOSFET (\( C_{\text{SB}} \)) as well as the source/drain-to-bulk capacitance of the AMOS varactor (\( C_{\text{BVAR}} \)). (4.2) can now be re-written as (4.4).
In designing the oscillator, the following parasitic capacitances were taken into account according to transistor measurements:

\[
C_{GS} = 0.7 \text{ fF} / \mu m \\
C_{GD} = 0.5 \text{ fF} / \mu m \\
C_B = C_{SB} + C_{BVAR} = 0.7 \text{ fF} / \mu m + 0.7 \text{ fF} / \mu m = 1.4 \text{ fF} / \mu m
\]

The simple MATLAB code shown in Appendix B was written to analyze the effect of the oscillator transistor size on the negative resistance, tuning range and tank voltage swing. In this analysis, the gate inductance is set to 40pH, the varactor capacitance range is 40fF to 80fF and the transistor transconductance is assumed to be 1mS/\mu m. \(C_1\) is scaled with the transistor size so as too keep the minimum value of the oscillation frequency (\(C_{VAR} = 80\text{fF}\)) constant at 80GHz.

The negative resistance, tuning range and tank voltage swing are plotted versus the transistor width in Figure 4.6, Figure 4.7 and Figure 4.8 respectively.
The transistors in the oscillator have been sized 60μm (75×0.8μm) to result in sufficient negative resistance and adequate tuning range. This also ensures that the tank voltage swing is above 1V. Using (4.4), $C_1$ can be estimated to be:

$$C_{TANK} = \frac{1}{(2 \pi f_{osc})^2 L_1} = 100 \text{fF}$$

$$C_1 = \frac{C_{VAR} \times C_{TANK} - C_{VAR} \times C_{GD} + C_B \times C_{TANK} - C_B \times C_{GD} - C_{GS}}{C_{VAR} + C_B + C_{GD} - C_{TANK}} = 80 \text{fF}$$

The tuning range of the oscillator can be estimated according to (4.4).
80GHz Digitally Controlled Oscillator

\[
\frac{f_{\text{OSCH}}}{f_{\text{OSCL}}} = \left( \frac{C_{GD} + (C_1 + C_{GS})(C_{VAR} + C_B)}{C_1 + C_{GS} + C_{VAR} + C_B} \right)^{1/2} = 1.044
\]

\[
f_{\text{OSCH}} = 1.044 \times 80\text{GHz} = 83.5\text{GHz}
\]

The estimated range corresponds to 3.5GHz.

Figure 4.9 shows the schematic of the DCO. The transistors in the oscillator and the varactors have 0.8μm finger width, and are contacted on both sides with two rows of contacts (see Figure 4.10), in order to minimize the phase noise of the oscillator. The transistors in the oscillator are biased at 0.25mA/μm for minimum noise, for a total current of 30mA in the differential oscillator.

Figure 4.9: Schematic of the DCO.
The common node of the oscillator is biased from $V_{DD}$ through a 1k$\Omega$ resistor (series combination of 220$\Omega$ and 880$\Omega$). The 0.8pF capacitor filters any noise that might be injected into the gate of the transistors from $V_{DD}$. The 16pH load inductors are designed to resonate with the large parasitic capacitance contributed by the 60$\mu$m transistors and the 40$\mu$m transistors in the clock buffer. The inclusion of the 250pH common mode inductor and the 1pF capacitor across the 10$\Omega$ biasing resistor has been experimentally shown to improve the phase noise of the oscillator [31]. The 250pH inductor is designed to be as large as possible, while the self-resonance frequency remains above $2 \times f_{\text{osc}}$ (i.e. 160GHz). The differential clock buffer is DC coupled to the oscillator and is tuned to 80GHz with 80pH inductive loads. The inclusion of the clock buffer prevents direct loading of the oscillator output, which could affect the oscillation frequency. Figure 4.11 shows the simulated oscillation frequency as a function of the three most significant bits. The simulated tuning range is 79GHz to 84GHz, in good agreement with the hand analysis. The simulated transient waveforms of the tank voltage as well as the output at 84GHz are shown in Figure 4.12. The voltage swing on the tank exceeds 1V$_{pp}$.

![Figure 4.10: DCO transistor and varactor layout.](image1)

![Figure 4.11: Simulated DCO oscillation frequency as a function of 3 most significant bits.](image2)
The phase noise of the oscillator was simulated to be -87dBc/Hz @ 79GHz and -79dBc/Hz @ 84GHz (Figure 4.13 and Figure 4.14).
4.2 Experimental Results

The fabricated DCO chip is shown in Figure 4.15. The die is pad limited, since separate pads were used for the digital control bits. The total chip size (including pads) is 470μm × 600μm, while the active core occupies 160μm × 210μm. **Due to a layout error, the digital control of the tuning voltage could not be demonstrated.** The mistake was made in the layout of the varactors. The different varactor cells were laid out in the same N-Well, and thus the seven control voltages were in effect shorted together through the N-Well.

One reason for this error is the fact that the varactor layout could not be verified with the Layout Versus Schematic (LVS) procedure, since the design kit has no models for the custom-made varactor. In simulations the varactors are modeled simply as ideal capacitors with a series resistance (to capture the loss), and the corresponding layout must be verified manually.

The operation of the oscillator was verified at the two extreme settings of the digital control word, by setting all the bits to either “0” or “1”, and measuring the oscillation frequency, phase-noise and the output power of the oscillator. The measured tuning range is 79GHz to 83.5GHz, in very good agreement with the hand analysis and simulations. This corresponds to 6% tuning range. Figure 4.16 shows the output spectrum of the oscillator at the two extremes.

![Die photo of the DCO.](image-url)
The output spectrum of the oscillator with a 10MHz span is shown in Figure 4.17. The measurements show the phase noise of the oscillator to be -92dBc/Hz at the lower range and -79dBc/Hz at the higher range of the tuning curve. The variation in the phase noise at the two extremes is due to the fact that the varactor Q changes by a factor between the two control levels. The output power of the oscillator was measured to be -4dBm to -3dBm.

The output power and tuning range measurements across 8 dies are compiled in Table 4.1.
Table 4.1: Measured tuning range and output power of oscillator versus die.

<table>
<thead>
<tr>
<th>Die</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tuning Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>79GHz</td>
<td>79.5GHz</td>
<td>79GHz</td>
<td>79.1GHz</td>
<td>79GHz</td>
<td>79.3GHz</td>
<td>79.1GHz</td>
<td>79GHz</td>
</tr>
<tr>
<td></td>
<td>To</td>
<td>To</td>
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<td>To</td>
<td>To</td>
<td>To</td>
<td>To</td>
</tr>
<tr>
<td></td>
<td>83.5GHz</td>
<td>83.6GHz</td>
<td>83.6GHz</td>
<td>83.6GHz</td>
<td>83.7GHz</td>
<td>83.8GHz</td>
<td>83.8GHz</td>
<td>83.6GHz</td>
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<tr>
<td></td>
<td>Output Power</td>
<td>-4dBm</td>
<td>-4dBm</td>
<td>-3.7dBm</td>
<td>-4dBm</td>
<td>-4.4dBm</td>
<td>-3dBm</td>
<td>-4.4dBm</td>
</tr>
<tr>
<td></td>
<td>To</td>
<td>To</td>
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<td>To</td>
<td>To</td>
<td>To</td>
<td>To</td>
</tr>
<tr>
<td></td>
<td>-2.8dBm</td>
<td>-3dBm</td>
<td>-2.7dBm</td>
<td>-2.6dBm</td>
<td>-3.2dBm</td>
<td>-3.9dBm</td>
<td>-3.9dBm</td>
<td>-3dBm</td>
</tr>
</tbody>
</table>

The overall performance of the oscillator is summarized in Table 4.2.

Table 4.2: Performance summary of the oscillator.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2V Nominal</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>79GHz – 83.5GHz (6%)</td>
</tr>
<tr>
<td>Output Power</td>
<td>-3dBm – -4dBm</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-92dBc/Hz – -79dBc/Hz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>72mW</td>
</tr>
<tr>
<td>Chip Size</td>
<td>470μm×600μm (Core: 160μm × 210μm)</td>
</tr>
</tbody>
</table>
5 Conclusion

The research presented in this thesis is focused on exploring the capabilities of the 65nm CMOS technology for implementation of W-band front-end integrated circuits for wireless applications. Simple, low power architectures have been demonstrated for the purpose of imaging, RADAR and multi gigabit per second radio. High quality inductors and transformers have been realized in digital CMOS back-end metallization. The small die area, which has been achieved with the lumped component approach to mm-wave design, demonstrates the possibility of the integration of the RF front-end and DSP units unto a single ship, for SoC solutions.

5.1 Contributions

The contributions made to the field of CMOS mm-wave design include:

- Design methodology of a shunt-series transformer-feedback amplifier is presented. The theoretical hand analysis is in good agreement with values arrived at by simulation, suggesting that a fairly accurate design based on hand-calculations is possible even at 80GHz. S-parameter and noise figure measurements confirm the broader input matching, higher gain and lower noise figure of the transformer-feedback LNA. The LNA has 13.5dB gain centred at 80GHz, and 6.4dB to 8.4dB noise figure across the 75-94GHz band. Measurements across dies show predictable and repeatable performance at 80GHz. This work contributed to the publication of the first W-band CMOS receiver, presented in [1].

- The performance of a W-band down-converter incorporating the LNA was measured with large IF-bandwidth of 9GHz, low noise figure of 7dB to 9dB and low power consumption.

- Design of an 80GHz-100GHz IQ receiver has been discussed. This receiver is designed to demonstrate the feasibility of an image-reject architecture, and verify the quadrature operation of the VCO presented in [1]. Measurements on the receiver indicate 10.5dB gain centred at 90GHz, with the 3dB bandwidth of 20GHz. The measured NF is 6.7dB to 8.5dB over the measurement band.
• Design of an 80GHz digitally controlled oscillator has been discussed. This oscillator topology yields a linear tuning curve. With the implementation of a DCO, one can take advantage of the advanced digital CMOS technologies to realize a fully digital W-band synthesizer. Due to error in layout, the digital tuning of the DCO was not achieved. However, measurements indicate 6% tuning range (79GHz to 83.5GHz), which agree with hand analysis and simulations. The phase noise of the oscillator was measured to be -92dBC/Hz at the lower oscillation range and -79dBC/Hz at the higher oscillation range.

5.2 Future Work

While this thesis is focused on RF front-end receiver circuits, the implementation of the Phase Locked Loop (PLL) unit (required for the LO signal generation) remains one of the most challenging areas of the mm-wave radio design. A 90GHz static frequency divider, implemented in 65nm CMOS technology has been demonstrated in [32], which along with the DCO could form the basis of a fully digital, W-band frequency synthesizer.

The implementation of phased arrays is also of major interest at mm-wave frequencies. Phased arrays achieve electrical beam-forming by the means of RF or LO phase shifting. With a single receiver, obstacles in the line of propagation could seriously deteriorate the received signal quality. A phased arrays receiver could adaptively change the angle of reception to avoid interference and thus increase the SNR. Phased array transceivers would also compensate for the low transmission power capability of CMOS transmitters.

5.3 Selected Publications


Appendix A

To analyze circuits consisting of two-ports connected in shunt at the input and in series at the output, as illustrated in Figure A.1, one can use g-parameters and the noise impedance formalism:

\[ i_n = i_u + Y_{cor} v_n \]  \hspace{1cm} (A.1)

In order to derive the equivalent input noise source expressions, one can write:

\[
\begin{bmatrix}
  g_{11} & g_{12} \\
g_{21} & g_{22}
\end{bmatrix} =
\begin{bmatrix}
  g_{11f} & g_{12f} \\
g_{21f} & g_{22f}
\end{bmatrix} +
\begin{bmatrix}
  g_{11a} & g_{12a} \\
g_{21a} & g_{22a}
\end{bmatrix}
\]  \hspace{1cm} (A.2)

\[ v_n = f(v_{nf}, i_{nf}, v_{na}, i_{na}) \]  \hspace{1cm} (A.3)

\[ i_n = f(v_{nf}, i_{nf}, v_{na}, i_{na}) \]  \hspace{1cm} (A.4)

The input equivalent noise sources can be calculated in two steps:

**Step 1:** The expression of the input noise voltage is obtained by short-circuiting the inputs and outputs of the two circuits in Figure A.1 and forcing the short circuit output currents to be equal:

\[ \text{Figure A.1: Two noisy two-ports connected in parallel at the input and series at the output (left) and noise equivalent circuit representation of the two shunt-series connected two-ports (right).} \]
Appendix A

\[ v_n = \frac{g_{21f} v_{nf} + g_{21a} v_{na}}{g_{21}} \]  

(A.5)

**Step 2:** The expression of the input noise current is obtained by open-circuiting the inputs and outputs of the two circuits in Figure A.1 and forcing the open circuit output voltages to be equal.

\[ i_n = i_{nf} + i_{na} + \frac{g_{11a} g_{21f} - g_{21a} g_{11f}}{g_{21}} v_{nf} + \frac{g_{11f} g_{21a} - g_{21f} g_{11a}}{g_{21}} v_{na} \]  

(A.6)

If the unilateral amplifier approximation holds, as in the case of a transistor at \( f \ll f_T \), then:

\[ g_{21} \approx g_{21a}, g_{12} \approx g_{12f} \]  

(A.7)

And one obtains:

\[ v_n = v_{na}, i_n = i_{nf} + i_{na} + g_{11f} (v_{na} - v_{nf}) \]  

(A.8)

\[ R_n = R_{na}, G_u = G_{uf} + G_{ua} + \left| Y_{cor} - g_{11f} \right| i R_{nf}, Y_{cor} = Y_{cora} + g_{11f} \]  

(A.9)

\[ Y_{SOPT} = \sqrt{\frac{G_{sota}}{R_{na}} + 2G_{cor} \Re(g_{11f}) + \Re^2(g_{11f}) + \left| Y_{cor} - g_{11f} \right|^2 \frac{R_{nf}}{R_{na}} + j B_{sota} - \Im(g_{11f})} \]  

(A.10)

\[ F_{MIN} = 1 + 2R_{na}[G_{cor} + G_{sopot} + \Re(g_{11f})] \]  

(A.11)

We note that the noise voltage of the amplifier with shunt-series feedback is equal to that of the main amplifier. The noise currents of the amplifier and the feedback networks add while \( Z_{IN} \) and \( Z_{SOPT} \) decrease. One can conclude that shunt-series transformer feedback can be used for noise matching in situations where the noise impedance of the original two-port is higher than that of the source impedance. The g-parameters of the transformer (with the loss of the primary described by \( G_P \) and that of the secondary by \( R_{SEC} \)) can be expressed as:

\[ g_{11f} = \frac{-j}{\omega L_p} + G_P, g_{12f} = \frac{M}{L_p}, g_{21f} = \frac{-M}{L_p}, g_{22f} = j \omega L_s (1 - k^2) + R_{SEC} \]  

(A.12)

The g-parameters of the cascode are:
\[ g_{11a} = y_{11a} - \frac{y_{12a} y_{21a}}{y_{22a}} = j\omega(2C_{gd} + C_{gs}) = j\frac{g_m}{f_T} \] (A.13)

\[ g_{22a} = \frac{1}{y_{22a}} = \frac{g_m^2 + G_L - j\omega(C_{gd} + C_{db})}{\left(\frac{g_m^2 + G_L}{g_m}\right)^2 + \omega^2(C_{gd} + C_{db})^2} \] (A.14)

\[ g_{12a} = \frac{y_{12a}}{y_{22a}} = 0 \] (A.15)

\[ g_{21a} = -\frac{y_{21a}}{y_{22a}} = \frac{g_m G_L + g_m^2 - j\omega g_m (C_{gd} + C_{db})}{\left(\frac{g_m^2 + G_L}{g_m}\right)^2 + \omega^2(C_{gd} + C_{db})^2} \] (A.16)

Where \( f_{Ta} \) is the cutoff frequency of the cascode stage and accounts for the Miller capacitance \( C_{GD} \).

The \( g \)-parameters of the entire amplifier with feedback shown in Figure A.2 are obtained by adding the \( g \)-parameters of the amplifier and those of the feedback network. We take into account that the cascode stage is loaded by \( G_L \) which describes the loss conductance of the load inductor \( L_D \).

---

\[ R_{FIN} = R_G + R_S + \frac{f_{Ta}(1-k^2) L_S}{j} \]

\[ X_{IN} = j\frac{f_{Ta}}{j} \]

\[ R_{IN} = \frac{R_G + R_S + f_{Ta}(1-k^2) L_S}{j} \]

**Figure A.2:** CS MOS LNA with shunt-series feedback (left), open loop amplifier with loading from feedback network (middle) and simplified equivalent circuit of the open loop amplifier (right).
Finally, the input admittance of the amplifier with feedback becomes:

\[
Y_{IN} = g_{11} - \frac{g_{12} g_{21}}{g_{22}} \approx \frac{M}{L_p} \frac{j f L_p}{f \tau_a} + \frac{g_m M}{L_p} + G_p
\]  

(A.21)

Equation (A.21) indicates that the feedback can be used to match the real part of the input admittance to 20mS over a broad bandwidth and to tune out the input capacitance of the cascode stage and the pad capacitance.

The noise sources at the input of the transformer feedback network are given by:

\[
\gamma_{nf}^2 = 4kT \Delta f \frac{M^2}{L_S^2} R_{SEC}
\]  

(A.22)

From them, the noise parameters of the feedback network can be derived:

\[
R_{nf} = \frac{M^2}{L_S^2} R_{SEC}, G_{nf} = G_p, Y_{corf} = 0, \Re(g_{11f}) = G_p
\]  

(A.23)

The noise parameters of the amplifier with lossy transformer feedback then become:
The optimal noise admittance and the minimum noise figure increase due to a lossy feedback network. Note that if the transformer is lossless, $G_P = 0$, $R_{SEC} = 0$, and the feedback is purely reactive and does not degrade the noise figure. Unfortunately in this case, it also does not change the real part of the optimum noise impedance. As a result, the optimal transistor size and bias current for noise matching are still as large as in the case without feedback.
Appendix B

The simple MATLAB code, presented at the end of this section was written to analyze the effect of the oscillator transistor size on the negative resistance, tuning range and tank voltage swing. The negative resistance and voltage swing of the oscillator tank are almost linearly proportional to the width of the transistor (i.e. the transconductance and current). However, increasing the transistor size leads to more parasitic capacitances, which muffle the effect of the varactor capacitance variation and reduce the tuning range.

Figure B.1 describes the different capacitance variables used in the code.

\[ C_{1EQ} = C_1 + C_{GS} \]
\[ C_{2EQ} = C_{VAR} + C_B \]
\[ C_{EQ} = \left( C_{1EQ} \times C_{2EQ} \right) / \left( C_{1EQ} + C_{2EQ} \right) \]
\[ C_{TANK} = C_{EQ} + C_{GD} \]

The MATLAB code:

\[ W = 40:80; \]
\[ gm = 1.0e-3*W; \]
\[ Cgd = 0.5e-15*W; \]
\[ Cgs = 0.7e-15*W; \]
\[ Cb = 1.4e-15*W; \]
\[ L = 40e^{-12}; \]
\[ C_{\text{var}} = 80e^{-15}; \]
\[ C_{\text{tank}} = \frac{1}{((2\pi \times 80e^9)^2) \times L}; \]
\[ C_{\text{1eq}} = \frac{(C_{\text{var}} \times C_{\text{tank}} - C_{\text{var}} \times C_{\text{gd}} + C_{\text{b}} \times C_{\text{tank}} - C_{\text{b}} \times C_{\text{gd})}}{(C_{\text{var}} + C_{\text{b}} + C_{\text{gd}} - C_{\text{tank}})}; \]
\[ C_{\text{2eq}} = C_{\text{var}} + C_{\text{b}}; \]
\[ C_{\text{eq}} = \frac{(C_{\text{1eq}} \times C_{\text{2eq}})}{(C_{\text{1eq}} + C_{\text{2eq}})}; \]
\[ F_{\text{osc}} = \frac{1}{(2\pi \times \sqrt{L \times (C_{\text{eq}} + C_{\text{gd})})}}; \]
\[ W_{\text{osc}} = 2\pi \times F_{\text{osc}}; \]
\[ R_{\text{neg}} = \frac{-g_{m}}{((W_{\text{osc}})^2) \times (C_{\text{1eq}} \times C_{\text{2eq}})}; \]
\[ V_{\text{swing}} = \frac{(2 \times W \times 0.25e^{-3} \times L)}{(C_{\text{3eq}} \times (5 + 200/W))}; \]
Bibliography


