TRANSMITTER FRONT-END ICs FOR 60-GHZ RADIO

by

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A thesis submitted in conformity with the requirements
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Graduate Department of Electrical and Computer Engineering
University of Toronto

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Abstract

The feasibility of millimeter-wave radio transmitter implementation in silicon is investigated in this thesis through the design, fabrication and testing of a novel 65GHz BPSK direct-modulation transmitter and a 60GHz single-sideband transmitter with 5GHz IF, both in 0.18μm SiGe BiCMOS. The BPSK transmitter is well-suited for low-cost, low-complexity mm-wave sensor applications, while the single-sideband transmitter, employing 5GHz and 65GHz polyphase filters for image rejection, offers a more sophisticated approach for 60GHz radio.

The power amplifier, as a crucial block in any transmitter front-end, is also explored through two 3-stage, 65GHz PAs implemented in 0.18μm SiGe BiCMOS and 90nm CMOS. The 90nm CMOS PA, representing the first 60GHz PA in CMOS reported to date, validates the specific designs techniques for optimizing linearity, while also demonstrating the potential of CMOS for mm-wave radio design.
Acknowledgments

I am grateful to my research advisor, Professor Sorin Voïnigescu, without whose mentorship and support none of this would have been possible. The opportunities he has given me and the knowledge he has imparted have made this a tremendously rewarding and memorable learning experience.

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<td>ASK</td>
<td>Amplitude Shift Keying</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Rate</td>
</tr>
<tr>
<td>BFSK</td>
<td>Binary Frequency Shift Keying</td>
</tr>
<tr>
<td>BPF</td>
<td>Bandpass Filter</td>
</tr>
<tr>
<td>BPSK</td>
<td>Binary Phase Shift Keying</td>
</tr>
<tr>
<td>BiCMOS</td>
<td>Bipolar Complementary Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>EIRP</td>
<td>Effective Isotropic Radiated Power</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>$f_T$</td>
<td>Unity gain frequency</td>
</tr>
<tr>
<td>$f_{MAX}$</td>
<td>Maximum oscillation frequency</td>
</tr>
<tr>
<td>$G_A$</td>
<td>Available Gain</td>
</tr>
<tr>
<td>$G_{MAX}$</td>
<td>Maximum Available Gain</td>
</tr>
<tr>
<td>HBT</td>
<td>Heterojunction Bipolar Transistor</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IRR</td>
<td>Image Rejection Ratio</td>
</tr>
<tr>
<td>ISM</td>
<td>Industrial, Scientific and Medical</td>
</tr>
<tr>
<td>$IP_{1dB}$</td>
<td>Input-Referred 1-dB Compression</td>
</tr>
<tr>
<td>LAN</td>
<td>Local Area Network</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LSB</td>
<td>Lower Sideband</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>MAG</td>
<td>Maximum Available Gain</td>
</tr>
<tr>
<td>MAN</td>
<td>Metropolitan Area Network</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-Insulator-Metal</td>
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<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
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<tr>
<td>NF</td>
<td>Noise Figure</td>
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<tr>
<td>$OP_{1dB}$</td>
<td>Output-Referred 1-dB Compression</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>PN</td>
<td>Phase Noise</td>
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<tr>
<td>PPF</td>
<td>Polyphase Filter</td>
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<tr>
<td>PRBS</td>
<td>Pseudo-Random Bit Sequence</td>
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<tr>
<td>PSA</td>
<td>Power Spectrum Analyzer</td>
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<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
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<td>QPSK</td>
<td>Quadrature Phase Shift Keying</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>Rx</td>
<td>Receiver</td>
</tr>
<tr>
<td>SiGe</td>
<td>Silicon Germanium</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
</tr>
<tr>
<td>SRF</td>
<td>Self Resonance Frequency</td>
</tr>
<tr>
<td>SSB</td>
<td>Single Sideband</td>
</tr>
<tr>
<td>Tx</td>
<td>Transmitter</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-Controlled Oscillator</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
</tr>
<tr>
<td>UNI</td>
<td>Unlicensed National Information Infrastructure</td>
</tr>
<tr>
<td>USB</td>
<td>Upper Sideband</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra-Wide Band</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
</tr>
<tr>
<td>WPAN</td>
<td>Wireless Personal Area Network</td>
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1

Introduction

Ever since the importance and feasibility of radio communication was established more than a century ago, it has revolutionized the way we share information. Today, the ubiquity of cellular telephony and satellite services attests to the rapid growth of wireless technology. But the demand for broadband multimedia applications such as wireless LAN bridges, WPAN, and wireless videoconferencing calls for an ever increasing capacity in wireless transfer that cannot be met with current 3G systems that support a maximum data rate of only 2Mb/s [5]. This is forcing the wireless industry to move beyond the traditional microwave frequency domain (2-30GHz) into the largely unexploited millimeter wave regime (30-300GHz) for its abundant available bandwidth. The 60GHz region is of special interest due to its numerous benefits for high data rate, short-range communication.

1.1. Motivation

As shown in Figure 1.1, the 7GHz of bandwidth centered around 60GHz is characterized by high levels (>10dB/km) of attenuation due to atmospheric oxygen absorption [6]. The attenuation over distance serves as a natural security mechanism, preventing the signal from being detected far beyond the intended recipient. An added benefit of the \( \text{O}_2 \) absorption is the lack of co-channel interference between links in the same geographic vicinity, allowing for higher frequency re-use than in long-range links. Phased arrays become feasible with the smaller antenna form factor at higher frequencies. Hence, better spatial directivity and higher antenna gain can be achieved [7].
1.1 Motivation

In light of the physical suitability of the 60-GHz region for short-range, high-density wireless links, the FCC has set aside the 57-64 GHz band for general unlicensed applications in 2001 (Table 1.1). Similar allocations were also made in Europe (59-63GHz) and Japan (59-66GHz) [1]. Making use of available spectrum at mm-waves effectively reduces interference from other wireless systems, most of which are currently operating in the congested low-GHz bands. Thus, compared to other standards such as UWB, the 60GHz band enjoys less stringent emission regulation (40dBm EIRP), making it possible to transmit multi-Gb/s signals over typical indoor distances of about 10m. Line-of-sight (LOS) and non-LOS operations are addressed in the IEEE802.16 standard for wireless MAN (10-66GHz) and the IEEE802.15 for WPANs (60GHz), respectively [8,9].

Table 1.1: FCC spectrum allocation for unlicensed use.

<table>
<thead>
<tr>
<th>Unlicensed Bands</th>
<th>Frequency Band (GHz)</th>
<th>Bandwidth (MHz)</th>
<th>IEEE Standard(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISM at 2.4GHz</td>
<td>2.4-2.4835</td>
<td>83.5</td>
<td>802.11b</td>
</tr>
<tr>
<td>UNI at 5GHz</td>
<td>5.15-5.35 / 5.725-5.825</td>
<td>300</td>
<td>802.11a</td>
</tr>
<tr>
<td>UWB</td>
<td>3.1-10.6</td>
<td>7500</td>
<td>802.15.3a, 802.15.4a</td>
</tr>
<tr>
<td>ISM at 60GHz</td>
<td>57-64</td>
<td>7000</td>
<td>802.15, 802.16</td>
</tr>
</tbody>
</table>

Figure 1.1: Atmospheric attenuation vs. frequency [1].
The majority of existing 60GHz radio front-end MMICs are implemented using the III-V compound semiconductors such as GaAs and InP [10–15]. Compound semiconductors enjoy a performance advantage at high frequencies due to their high electron mobility, high breakdown voltage, low substrate loss, and high quality factor (Q) passives. However, their high cost and low integration ability with CMOS-based DSP ultimately make them unsuitable for realizing complete 60GHz SoCs for the consumer marketplace.

The SiGe HBT is emerging as a strong contender for mm-wave applications, thanks to earlier advancements in bandgap engineering [16] and to the more recent achievements in reaching $f_T$, $f_{MAX}$ that exceed 200GHz [17–19]. Several 60GHz radio front-end circuits have been recently reported [20, 21] that demonstrate the comparable performance of SiGe to III-V implementations. In addition, numerous high-performance mm-wave circuits have also been implemented in SiGe for the automotive radar application at 77GHz [22–24]. Although an integrated 60GHz CMOS receiver has been reported [20, 25], the integrated transmitter has largely been unexplored. The difficulties of achieving adequate upconversion gain at high frequencies and meeting stringent linearity requirements for sophisticated modulation schemes make transmitter design at 60GHz a non-trivial task.

With the aggressive scaling of CMOS comes the promising solution for an all-CMOS 60GHz SoC. This has been shown in a 60GHz LNA designed in a standard 0.13µm CMOS process [26], 64GHz and 100GHz VCOs in 90nm CMOS [27] and a 63GHz VCO in standard 0.25µm CMOS [28]. However, for CMOS to emerge as a practical solution at 60GHz as it is beginning to in the low-GHz RFIC arena, there are still design bottlenecks to be overcome. One of these bottlenecks is in the design of the power amplifier — an important transmitter building block whose requirements for high breakdown voltage, low substrate loss and high power density make its implementation in CMOS more challenging than in III-V and SiGe technologies.

1.2. Objective

In this thesis, the feasibility of implementing millimeter-wave radio transmitters in silicon is studied. This is pursued through the design, fabrication and testing of two transmitters with different architectures, as well as various building blocks, including two sequence
asymmetric polyphase filters and two 3-stage power amplifiers implemented in 0.18µm SiGe BiCMOS and 90nm CMOS processes. The transmitters allow for a comparison of possible transmitter topologies for 60GHz radio, while tradeoffs in the choice of implementation technology for mm-wave radio are explored through the HBT and CMOS power amplifiers.

1.3. Organization

In Chapter 2, background information is presented on system-level considerations for 60GHz radio, various types of transmitter architectures, the power amplifier, and the implementation technologies used for this thesis work. The state-of-the-art is also reviewed in more detail. Chapter 3 focuses on mm-wave power amplifier design techniques and considerations, as illustrated in the designs of power amplifiers in 0.18µm SiGe BiCMOS and 90nm CMOS. The two designs also facilitate an evaluation of the tradeoffs in the choice of technology for mm-wave power amplifiers. Chapter 4 discusses the design and implementation of a novel 65GHz BPSK directly-modulated transmitter, followed by a discussion of a single-sideband transmitter for 60GHz radio. Chapter 5 presents the measurement procedure and results for all circuits. Chapter 6 concludes this thesis with a summary of the results and a discussion of possible improvements and potential directions for future research.
Background

This chapter presents the system-level considerations for 60GHz radio, as well as various suitable transmitter architectures. The design issues and challenges in PA integration in silicon are discussed, followed by an examination of the device-level characteristics that are crucial to the successful design of radio systems at mm-wave frequencies. The chapter concludes with a look at the state-of-the-art in 60GHz radio front-end research.

2.1. 60GHz Radio Architecture Overview

An example of a 60GHz radio architecture is the traditional heterodyne approach shown in Figure 2.1. It consists of the low noise amplifier and downconvert mixer on the RF receive side, and the power amplifier and upconvert mixer on the RF transmit side. Quadrature modulation is performed in the baseband for higher spectral efficiency. Improved isolation between the RF LO and the power amplifier is provided by the two-step conversion between baseband and RF. The classical radio architectures are experiencing a rebirth in mm-wave ICs due to their robustness and simplicity — two important factors of consideration at high operating frequencies. This is in contrast to systems in the low-GHz range where more complex architectures are feasible in light of the higher transistor gain and the lower impact of parasitics.

The successful design of any wireless link begins with a link budget analysis — a straightforward calculation that determines the feasibility of a given system in terms of the power gains and losses present. It provides insight into the various top-level tradeoffs in realizing a communication link, such as range, data rate and modulation technique,
Figure 2.1: Heterodyne front-end for 60GHz radio.

and is also a crucial first-step in defining the system design objectives. To perform a link budget analysis, one must first gain an understanding of the relevant system parameters, such as channel bandwidth, channel loss and the required reliability (defined by the BER). To that end, the following subsections discuss some of the key system parameters, leading to a link budget comparison between a 1.55Gb/s WLAN (60GHz) and an IEEE802.11a (5GHz) system.

2.1.1. Channel Characteristics

The wide-spread interest in 60GHz systems has resulted in a number of studies characterizing the 60-GHz channel. The specific measurement techniques and channel models are beyond the scope of this discussion. The interested reader is encouraged to consult the literature, i.e. [29–31] for the detailed findings. Instead, this subsection addresses the specific channel properties that play a role in the link planning process.

The free-space path loss at 60GHz is significantly higher than at 5GHz since, according to the classic Friis equation for radio links [1], the free-space loss increases quadratically with frequency:

$$P_r = \frac{G_t G_r \lambda^2}{(4\pi R)^2} P_t(W)$$  \hspace{1cm} (2.1)
2.1 60GHz Radio Architecture Overview

where $P_r$ is the received power, $P_t$ is the transmit power, $G_t$ and $G_r$ are the transmit and receive antenna gains, respectively, $\lambda$ is the wavelength ($\lambda = c/f$) and $R$ is the antenna separation distance. From this equation, the free space path loss can be determined as:

$$\text{PathLoss} = 20 \log \frac{4\pi R}{\lambda} (dB)$$

(2.2)

Thus, assuming a nominal omnidirectional antenna, the extra free-space loss incurred in moving from 5GHz to 60GHz is approximately 22dB, solely due to the decrease in wavelength.

In addition to the higher loss due to the frequency of operation, the 60GHz band is also susceptible to higher levels of attenuation. As mentioned in Chapter 1, a principal motivation for 60GHz radio is the high level of atmospheric attenuation. When transmitted indoors, signals at this frequency are also subjected to additional attenuation by the walls and floors [32], hence indoor transmission is limited to small indoor cells.

While the building structures provide natural cell boundaries, they also contribute to multipath fading by acting as obstacles blocking the LOS or alternative paths. The result is that waves from the transmitter travel along different paths and destructively interfere with waves along a direct LOS path. Their differences in phase may cause a complete cancellation of signals at the receive antenna. The effects of fading results in the need for extra RF power, expressed as a fade margin in the link budget.

2.1.2. Integrated Antennas and Phased Arrays

Given the various channel impairments present at 60GHz, one might wonder how any communication system can be feasible in this frequency range. Luckily, the power losses can be overcome with the use of directional antennas, whose implementation is made easier at higher frequencies due to the smaller antenna form factors. Directional antennas can improve the multipath profile by limiting the spatial extent of the transmit and receive signals; they also provide higher gain compared to their omni-directional counterparts. A revisit of the Friis equation reveals that the received power $P_r$ normalized to the transmit
power $P_t$ is proportional to the transmit and receive antenna directivities $D_{1,2}$.

$$\frac{P_r}{P_t} = \frac{D_1 D_2 \lambda^2}{(4\pi R)^2} \propto D_1 D_2$$  \hspace{1cm} (2.3)

The antenna gain is directly proportional to the directivity $D$ and the radiation efficiency $e_{rad}$:

$$G = e_{rad} D$$  \hspace{1cm} (2.4)

The maximum directivity that can be attained by an aperture antenna $^{2}$ is given by:

$$D_{\text{max}} = \frac{4\pi A}{\lambda^2}$$  \hspace{1cm} (2.5)

where $A$ is the aperture area.

Since the antenna efficiency cannot exceed unity, it is clear that the antenna gain is always less than or equal to the directivity. It can also be noted that higher antenna gain can be achieved simply by operating at a higher frequency, with a fixed antenna form factor. This gives the 60-GHz system a much needed advantage in light of the higher path loss.

The antenna directivity, and hence gain, can be further increased by employing an antenna array – a configuration that is easier to implement at 60GHz than at lower frequencies due to the smaller antenna form factors. An antenna array, or, more specifically, an adaptive antenna array, is highly effective in achieving high antenna gain in a dynamic, mobile environment [7, 33]. The direction of the main beam can be adapted electronically through the use of phase shifters to achieve optimal antenna gain at any moment. This makes the antenna array approach superior to a single directional antenna whose orientation cannot be quickly changed to adapt to the mobile environment.

An important consideration in designing a phased array system is the location of the phase shifters. While a straightforward approach is to connect an entire transceiver to each antenna and apply the phase shift digitally at baseband, the system complexity would cause the power and area consumption to exceed acceptable levels. Another ap-

$^{1}$Antenna directivity is a measure of the focusing ability of an antenna, and is defined as the ratio of the maximum radiation intensity in the main beam to the average radiation intensity over all space [1].

$^{2}$Aperture antennas refer to the type of antenna with a well-defined aperture area that emits radiation [1].
2.1 60GHz Radio Architecture Overview

The approach is to apply the phase shift in the analog domain, between the baseband and RF mixers. While only one set of ADC and DAC is needed at baseband, there is still the need for N RF mixers and PAs. A third approach, and the most area and power-efficient, is the use of RF phase shifters, situated before the PA in the transmitter, and after the LNA in the receiver. Figure 2.2 shows a possible implementation of such a phased array system.

![Phased Array System Diagram](image)

Figure 2.2: Possible implementation of a 60GHz phased array transceiver system.

Implementing the phase shift at RF is advantageous in reducing the number of RF mixers and baseband ADCs/DACs. Placing the phase shifters before the PA ensures that they do not need to handle large input power levels nor provide significant gain. Their noise contribution is also less critical in the receiver when placed after the LNA. Potential challenges in adopting this scheme are ensuring the phase accuracy of each path leading up to the phase shifters, as well as ensuring uniform loss for all phase shifters to avoid the need for equalization using variable gain amplifiers, which prevent array pattern degradation. A 24GHz phased array, based on an LO path phase-shifting architecture, has also been investigated [7], which has the advantage of minimal variation in signal amplitude for different values of phase shift. The main benefit of using a phased array, from the transmitter design point of view, is the more relaxed requirements on the PA output power, since each individual PA would only be required to deliver 1/N the total output power.
2.1.3. Link Budget Analysis

A link budget analysis can be performed once sufficient information about the radio channel and architecture is known. The following calculation illustrates the impact of the various system parameters on the overall link performance, and provides insight into the amount of transmit power needed for accurate data transmission, as defined by the BER.

The following assumptions are made about the system prior to calculating the link budget:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation Scheme</td>
<td>QPSK</td>
</tr>
<tr>
<td>Data Rate (Gb/s)</td>
<td>1.55</td>
</tr>
<tr>
<td>Receiver Noise Figure (NF) (dB)</td>
<td>10</td>
</tr>
<tr>
<td>Range (m)</td>
<td>10</td>
</tr>
<tr>
<td>Antenna Gain (dBi)</td>
<td>20 for both $G_{tx}$ and $G_{rx}$</td>
</tr>
<tr>
<td>Fade Margin (FM) (dB)</td>
<td>10</td>
</tr>
<tr>
<td>System Margin (dB)</td>
<td>20</td>
</tr>
</tbody>
</table>

**Receiver Sensitivity**

The receiver sensitivity is a measure of the required signal strength at the input of the receiver. It is dependent on several parameters such as data rate, modulation scheme, required BER and receiver noise figure. The modulation scheme is chosen to maximize the bandwidth efficiency. In 60GHz systems where the data rate may reach 1-2 Gb/s, the higher order modulation schemes found in current 3G systems, such as QPSK and 16QAM, are chosen for their high spectral efficiency. The tradeoff in using these types of modulation scheme is the higher SNR needed for a specified BER, which translates into a higher receiver sensitivity. Fortunately, the short-range, point-to-point nature of 60GHz links allows for a better SNR performance than, for example, mobile phone systems where the larger range of coverage limits the SNR performance.
The SNR needed to achieve an acceptable BER (typically $10^{-6}$ for wireless links) for a given channel data rate $R$ and bandwidth $B_T$, is found by:

$$SNR = \left( \frac{E_b}{N_o} \right) \left( \frac{R}{B_T} \right),$$  \hspace{1cm} (2.6)

where $(E_b/N_o)$ is a measure of the required energy per bit relative to the noise power, and is independent of the system data rate.

The system bandwidth is determined by the system data rate and the spectral efficiency ($\eta$) of the modulation scheme:

$$B_T = \frac{R}{\eta}$$  \hspace{1cm} (2.7)

Hence, following our initial assumptions, a 1.55Gb/s QPSK system with a spectral efficiency of 1.6bps/Hz [34] and $E_b/N_o$ of 10.5dB for a BER of $10^{-6}$ [35] would have a required SNR of 12.6dB.

The receiver sensitivity is also affected by the channel noise and the receiver noise figure. The channel noise is found by:

$$N = kTB,$$  \hspace{1cm} (2.8)

where $N = \text{noise power}$ $k = \text{Boltzman’s constant (1.38 x 10-23 J/K)}$ $T = \text{system temperature (usually 290K)}$ $B = \text{channel bandwidth}$

Thus, for a QPSK system with a channel bandwidth of 970MHz, the channel noise is found to be -83dBm. The receiver sensitivity is found to be:

$$P_{rx} = N + NF + SNR = -60dBm.$$  \hspace{1cm} (2.9)

**Path Loss**

Assuming a 10m transmission distance at 60GHz, the path loss ($PL$) is computed as:

$$PL = 20 \log \left( \frac{4\pi D}{\lambda} \right) = 88dB.$$  \hspace{1cm} (2.10)
Transmitter Power

Now, the required transmitter power can be found:

\[ P_{tx} = P_{rx} - G_{tx} - G_{rx} + PL + FM = -2dBm. \]  \hspace{1cm} (2.11)

Assuming a system margin of \( \approx 20dB \) to ensure reliable operation, the minimum required transmit power is 18dBm, which can be achieved with 6 parallel transmitters, each with 10dBm output power. For maximum linearity to support the variable envelope modulation schemes used, these powers represent the \( OP_{1dB} \) of the transmitters. The parallel transmitter architecture can be implemented using one of the phased array approaches discussed in the previous section.

The results of this link budget calculation are summarized in the table below. Also shown are results for a 60GHz link (1.55Gb/s WLAN) using 16-QAM modulation, and a 5GHz link (IEEE802.11a) using QPSK. For the 5GHz link, assumptions about the antenna gains, data rate and receiver noise figure are made based on typical values stated in [36]. From these calculations, it is evident that while using a modulation scheme with a higher spectral efficiency leads to a reduced channel bandwidth, it also requires a higher SNR and hence more stringent requirements on the receiver sensitivity, increasing the amount of transmit power required. Comparing the 60GHz and 5GHz links, it can be seen that a much lower transmitter output power is required at 5GHz due to the reduced path loss and lower data rate. Employing a parallel-PA topology (as in Figure 2.2) is imperative to achieving the level of output needed for a robust 60GHz link with a silicon implementation.
Table 2.2: Link budgets for 60GHz and 5GHz systems.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>60GHz - QPSK</th>
<th>60GHz - 16QAM</th>
<th>5GHz - QPSK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate (Mb/s)</td>
<td>1550</td>
<td>1550</td>
<td>12</td>
</tr>
<tr>
<td>$P_{rx}$ (dBm)</td>
<td>-60</td>
<td>-57.6</td>
<td>-82.7</td>
</tr>
<tr>
<td>SNR (BER = $10^{-6}$) (dB)</td>
<td>12.53</td>
<td>19.55</td>
<td>12.53</td>
</tr>
<tr>
<td>$E_b/N_0$ (BER = $10^{-6}$) (dB)</td>
<td>10.5</td>
<td>14.5</td>
<td>10.5</td>
</tr>
<tr>
<td>$B_T$ (MHz)</td>
<td>970</td>
<td>485</td>
<td>7.5</td>
</tr>
<tr>
<td>Rx NF (dB)</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Fade Margin (dB)</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Path Loss (10m)(dB)</td>
<td>88</td>
<td>88</td>
<td>66</td>
</tr>
<tr>
<td>Spectral Efficiency (bps/Hz)</td>
<td>1.6</td>
<td>3.2</td>
<td>1.6</td>
</tr>
<tr>
<td>$G_{tx}$ (dBi)</td>
<td>20</td>
<td>20</td>
<td>6</td>
</tr>
<tr>
<td>$G_{rx}$ (dBi)</td>
<td>20</td>
<td>20</td>
<td>6</td>
</tr>
<tr>
<td>System Margin (dB)</td>
<td>20</td>
<td>20</td>
<td>5</td>
</tr>
<tr>
<td>$P_{tx}$ (dBm)</td>
<td>18</td>
<td>20</td>
<td>-13.7</td>
</tr>
</tbody>
</table>

2.2. Transmitter Architectures

The transmitter performs the tasks of modulation, upconversion and power amplification. There are two types of upconversion found in radio transmitters: the homodyne, or direct, upconversion and the heterodyne, or two-step, upconversion.

In the direct upconversion approach (Figure 2.3), modulation and upconversion occur in the same circuit, with the transmitter carrier frequency being equal to the LO frequency. This has the attractive advantage of low hardware complexity, and relatively simple modulators can be used to implement schemes such as ASK, FSK and BPSK. For instance, ASK can be generated using switches, FSK can implemented with a switched VCO and BPSK can be generated by analog or digital $180^\circ$ phase shifters. Quadrature modulation schemes such as QPSK can be realized using the popular I-Q vector modulator. The main drawback of direct upconversion, however, is that because the LO frequency is the same as the carrier frequency, this architecture is susceptible to a phenomenon called “injection pulling” whereby the LO spectrum is corrupted and shifted by the high power PA output. This problem is especially significant in a phased-array employing multiple PAs.

The problem of injection pulling can be circumvented by using a two-step upconversion, in which the PA output is moved further away from the LO frequency. In the heterodyne transmitter (Figure 2.4), the baseband signal modulates a local oscillator.
(LO) signal to create an intermediate frequency (IF). The IF is then filtered and upconverted with a second LO carrier to produce the final RF signal for transmission. The use of the IF has the advantage of separating the frequencies of the VCOs and the PA, thereby alleviating the injection pulling problem. The tradeoff for the performance improvement is the added hardware complexity, leading to increased cost and power consumption. The choice of transmitter architecture, then, depends on the performance requirements of the application, as well as the desired level of integration.

Figure 2.3: Direct upconversion (homodyne).

Figure 2.4: Two-step upconversion (heterodyne).

2.3. The Single-Sideband Modulator

In both the direct and single-IF upconversion processes, there exists the problem of filtering out the unwanted sideband at RF, which is a byproduct of the mixing process. The conventional method has been to use an off-chip filter for its high Q-factor. However,
off-chip implementations hinder the development of fully integrated SoC transceivers, while on-chip implementations tend to occupy large die area, increasing the system cost.

An alternative method for generating single-sideband on-chip is to use the image rejection mixer – a topology that employs couplers to isolate the desired and image signals by introducing different phase shifts to the two frequencies present. The same topology may be used in up-conversion, where it is sometimes referred to as a “single-sideband (SSB) modulator” [1]. The block diagram for the SSB modulator is shown below in Figure 2.5. It consists of two identical mixers and two 90° hybrids performing the functions of quadrature generation and combination at the IF input and RF output, respectively. The LO signal is applied in-phase to the two mixers.

The operation of the SSB modulator can be better understood with the following time domain analysis using the small signal approximation. Assuming that the input IF and the LO are as follows:

\[ V_{IF} = IF \cos(\omega_{IF}t) \] 
\[ V_{LO} = LO \cos(\omega_{LO}t) \]

and that their amplitudes (IF, LO) are unity (since we are mostly interested in the frequency and phase responses), then it can be seen, based on the mixing operation, that

---

**Figure 2.5: Single-sideband modulator.**

The operation of the SSB modulator can be better understood with the following time domain analysis using the small signal approximation. Assuming that the input IF and the LO are as follows:

\[ V_{IF} = IF \cos(\omega_{IF}t) \] 
\[ V_{LO} = LO \cos(\omega_{LO}t) \]

and that their amplitudes (IF, LO) are unity (since we are mostly interested in the frequency and phase responses), then it can be seen, based on the mixing operation, that
the intermediate signals at points A, B, C and D are as follows:

\[ A = \cos(\omega_{IF} t - \frac{\pi}{2}) \]  
\[ B = \cos(\omega_{IF} t - \pi) \]  
\[ C = \cos(\omega_{IF} t - \frac{\pi}{2}) \cos(\omega_{LO} t) \]  
\[ D = \cos(\omega_{IF} t - \pi) \cos(\omega_{LO} t) \]

Expressing C and D as the sum of cosines gives:

\[ C = \frac{1}{2} \cos(\omega_{IF} t + \omega_{LO} t - \frac{\pi}{2}) + \frac{1}{2} \cos(\omega_{LO} t - \omega_{IF} t + \frac{\pi}{2}) \]  
\[ D = \frac{1}{2} \cos(\omega_{IF} t + \omega_{LO} t - \pi) + \frac{1}{2} \cos(\omega_{LO} t - \omega_{IF} t + \pi) \]

Since the signal at E is the sum of the signal at C shifted by \( \frac{\pi}{2} \) and the signal at D shifted by \( \pi \), it can be expressed as:

\[ E = \frac{1}{2} \cos(\omega_{IF} t + \omega_{LO} t - \pi) + \frac{1}{2} \cos(\omega_{LO} t - \omega_{IF} t) 
- \frac{1}{2} \cos(\omega_{IF} t + \omega_{LO} t - \frac{\pi}{2}) - \frac{1}{2} \cos(\omega_{LO} t - \omega_{IF} t + \pi) \]

which, after simplifying, reduces to

\[ E = \cos((\omega_{LO} - \omega_{IF}) t) \implies \text{LSB,} \]  

with LSB representing the lower sideband. Similarly, the signal at F is the sum of the signal at D shifted by \( \frac{\pi}{2} \) and the signal at C shifted by \( \pi \), hence,

\[ F = \frac{1}{2} \cos(\omega_{IF} t + \omega_{LO} t - \frac{3\pi}{2}) + \frac{1}{2} \cos(\omega_{LO} t - \omega_{IF} t + \frac{\pi}{2}) 
- \frac{1}{2} \cos(\omega_{IF} t + \omega_{LO} t - \frac{\pi}{2}) - \frac{1}{2} \cos(\omega_{LO} t - \omega_{IF} t + \frac{\pi}{2}) \]

which yields the upper sideband:

\[ F = \cos((\omega_{LO} + \omega_{IF}) t + \frac{\pi}{2}) \implies \text{USB} \]  

Thus, with the upper sideband and lower sideband generated at the two output ports of the modulator, there is the freedom to choose either as the desired signal while
2.4 Power Amplifiers

As the final stage in a radio transmitter, the power amplifier performs the important functions of amplifying the upconverted signal and delivering the desired power to a load, such as a 50Ω antenna. Its need to drive large power outputs often makes it the dominant block in an entire transceiver chain in terms of power consumption. The full integration of power amplifiers has long been hindered by the poor power-handling capability of integrated circuits, which is exacerbated by a lower breakdown voltage with each generation of scaling. The fundamental trade-off between breakdown voltage and $f_T$, as characterized by the $BV_{CEO} \times f_T$ product better know as the Johnson Limit [37]³, dictates the lower available transistor voltage swing at high frequencies. This presents an upper limit on the maximum achievable output power when coupled with limitations in current migration in the metals. Due to the lossy silicon substrate, on-chip passives suffer from lower quality factor and higher crosstalk through the substrate, leading to higher substrate loss for PA signals and reduced isolation between the PA and adjacent circuit blocks.

The difficulties typically encountered in PA integration at low GHz frequencies are slightly alleviated in 60GHz radio applications due to the shorter transmission distance and the higher antenna gains. Since the transmission is typically over $\approx 10m$ in an indoor environment, the maximum output power required from the PA is on the order of hundreds of milliwatts, as opposed to $>1W$ in the case of cellular applications. In addition, the feasibility of phased antenna arrays at these frequencies enable higher directivity and gain in the antennas, as well as parallel PA architectures. Despite the more relaxed requirements, successful integration of the PA at 60GHz is dependent on minimizing parasitic losses to maintain adequate gain (given the lower MAG of transistors at mm-waves), designing with low voltage swings for low breakdown devices, and achieving sufficient linearity for advanced modulation schemes. The integration of high perfor-

³The Johnson limit for silicon bipolar is about 100-200GHzV, while for InP it is about 500-1000GHzV.
mance RF front-end blocks such as the PA with baseband DSP on a silicon substrate is imperative to the realization of low cost 60GHz radio SoCs for the consumer market.

2.4.1. Power Amplifier Performance Parameters

The important performance metrics for PAs are output power, gain and efficiency. The maximum output power of the PA is specified at the 1-dB compression point, which is a measure of the input power level at which the PA gain is reduced by 1dB, as expressed in (2.24) and shown in Figure 2.6.

\[
OP_{1dB} = IP_{1dB} + (G - 1), \quad (2.24)
\]

where \( G \) is the small signal (linear) power gain.

![Figure 2.6: 1dB compression point.](image)

PA efficiency is a primary concern for many portable wireless devices since the PA is often the dominant consumer of DC power. The efficiency can be measured simply as the ratio of the RF output power to the DC input power:

\[
\eta = \frac{P_{out}}{P_{DC}} \quad (2.25)
\]

Since PAs often have relatively low gains, this measure tends to over-estimate the efficiency by not accounting for the RF input delivered to the amplifier. A more accurate
measure of efficiency is the power added efficiency which does take into account the effect of RF input power, and hence gain [38]:

\[ \eta_{PAE} = PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right) \frac{P_{out}}{P_{DC}} = \left(1 - \frac{1}{G}\right) \eta \]  

(2.26)

The performance parameters can be linked together in the following figure-of-merit (FoM) for mm-wave PAs [39]:

\[ FoM_{PA} = P_{out} \times G \times PAE \times f^2, \]  

(2.27)

where \( P_{out} \) is the \( P_{1dB} \) output power in watts, \( G \) is the gain as a ratio and \( f \) is the frequency of operation in GHz. The \( f^2 \) term reflects the degradation in transistor gain and output power with the square of frequency.

### 2.4.2. Power Amplifier Classifications

PAs are classified according to their bias condition (A, AB, B, C) and their mode of operation (classes D, E, F). Additionally, the classes can also be categorized as linear (A, AB, B) and nonlinear (C, D, E, F) amplifiers. Linear amplifiers find application in variable envelope modulation where the signal must be linearly amplified for correct demodulation by the receiver. However, since the design of PAs always involves a compromise between linearity and efficiency, linear PAs suffer from poor maximum power efficiency, limiting their use in low power applications. In contrast, nonlinear PAs, such as Class E and F, offer much better efficiency at the cost of linearity, making them ideal for low power devices employing constant envelope modulation schemes (ie. FSK, GMSK). Since this thesis is focused on 60GHz radio systems where high order, variable envelope modulation schemes such as M-QAM and QPSK are desired for their high spectral efficiency, the Class A PA is needed to achieve maximum linearity.

### 2.5. Linearity in Cascaded Systems

The need to cascade multiple amplification stages in a PA to achieve a desired power gain calls for an understanding of the gain and linearity relationship in a cascaded system.
This is also important in the overall transmitter design which involves the cascading of a number of building blocks.

With reference to Figure 2.7, the input \( (IP_1) \) and output \( (OP_1) \) 1dB compression points for a system are expressed as \( [4] \):

\[
\frac{1}{OP_1} = \frac{1}{OP_{1n}} + \frac{1}{OP_{n-1}} + \frac{1}{OP_{n-2}} + \ldots + \frac{1}{Ga_2 \times \ldots Ga_n \times OP_1}
\]

\[
\frac{1}{IP_1} = \frac{1}{IP_{11}} + \frac{Ga_1 \times Ga_2}{IP_{12}} + \frac{Ga_1 \times Ga_2}{IP_{13}} + \ldots + \frac{Ga_1 \times Ga_2 \times \ldots Ga_{n-1}}{IP_{1n}}
\]

where \( OP_1 \) and \( IP_1 \) are both linear units \( (W) \), and \( Ga \) is simply the power gain ratio.

![Figure 2.7: Linearity in a cascaded system.](image)

From these expressions, it can be seen that first, although increasing the number of cascaded stages improves gain, the overall linearity actually degrades as more stages are added. Secondly, both linearity and gain should be made progressively higher towards the final stage, whose impact on the overall linearity is greatest. Thus, the gain and linearity of the final stage should be maximized to achieve high system linearity. The difficulty in this lies in the ever-present tradeoff between linearity and gain, since linearity is often improved through the use of feedback, which invariably degrades gain. An adequate compromise between the two criteria can be reached if more gain contribution is made in the early stages, where linearity is not as crucial as in the later stages.

### 2.6. Technology Overview

This section provides an overview of the two implementation technologies used in this thesis: 0.18µm SiGe BiCMOS and 90nm CMOS, with a focus on the effect of device optimization through correct sizing and biasing on PA performance.
2.6 Technology Overview

2.6.1. Actives

The high frequency figures of merit (FoMs), $f_T$ and $f_{MAX}$, allow for a quantitative comparison between the SiGe HBT and CMOS technologies used in the PA designs, while also providing insight into the impact of bias and device geometry on circuit performance. The cutoff frequency, $f_T$, is arguably the most widely used FoM for transistor speed, and represents the frequency at which the common-emitter small-signal current gain, $h_{21}$, becomes equal to 1. The $f_T$ for SiGe HBTs is given by [4]:

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + \frac{1}{g_m} (C_{je} + C_\mu) + (R_e + R_c)C_\mu, \quad (2.30)$$

in which the dominant third term indicates a first order dependence of $f_T$ on the bias current $I_C$. The transit times $\tau_B$ and $\tau_C$ are directly proportional to the base and collector widths, while dependence on emitter length cancels out to a first order due to length dependence cancellation in the RC product.

The $f_T$ expression for the MOSFET is given by [4]:

$$\frac{1}{2\pi f_T} = \frac{(C_{gs} + C_{gd})}{g_m} + (R_s + R_d)C_{gd} + \left( \frac{C_{gs}}{1 + g_mR_s} + C_{gd} \right)R_d \frac{g_{ds}}{g_m}. \quad (2.31)$$

The dominant first term indicates a linear dependence of $f_T$ on $V_{gs}$, while the second and third (feedback) terms are weak functions of bias. To a first order, the MOSFET $f_T$ is independent of device finger width ($W_f$). But as a second order effect, $f_T$ decreases with lower $W_f$ due to the gate-bulk overlap capacitance $C_{GBO}$.

The maximum oscillation frequency ($f_{MAX}$) accounts for the effect of the base resistance for the HBT and the gate, source and channel resistance for the MOSFET. Since $f_{MAX}$ occurs at the frequency when $G_{MAX}$ (MAG) becomes unity, it directly reflects the high-frequency dependence of the transistor power gain and hence provides much insight into PA linearity. The $f_{MAX}$ for the HBT is approximately given by:

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_\mu R_b}}, \quad (2.32)$$

where there is a strong dependence on emitter width due to the $R_b$ term, and a weaker dependence on emitter length since $R_b \propto 1/l_E$ and $C_\mu \propto l_E$. The latter results in lower
sensitivity of the HBT $f_{MAX}$ to layout, since the emitter length is often varied while the emitter width is fixed at a minimum value for low base resistance.

In contrast, the MOSFET $f_{MAX}$ is heavily dependent on device layout by capturing the effects of the gate resistance $R_g$, which is directly proportional to the finger width, $W_f$:

$$f_{MAX} = \frac{f_T}{2\sqrt{R_g(g_{ds} + 2\pi f_T C_{gd}) + g_{ds}(R_i + R_s)}} \quad (2.33)$$

With $f_{MAX}$ being inversely proportional to $W_f$, the best design practice, then, is to minimize $W_f$ for $f_{MAX}$, but not beyond the point of $f_T$ degradation due to $C_{GBO}$. For the 90nm CMOS process, this translates to an optimal $W_f$ of 1-2µm.

Shown in Figures 2.8, 2.9 are the measured $f_T$ and $f_{MAX}$ curves for the 0.18 – µm SiGe HBT and 90nm CMOS processes used in this thesis. The plots are based on a 2.64 × 0.2 µm NPN 232 (EBC) device for the SiGe HBT, and $W_f$ of 1 and 2µm for the 90nm CMOS. Although their $f_T$ and $f_{MAX}$ performance are comparable, the HBT offers the advantage of higher $G_{MAX}$ whereas better linearity can be achieved in CMOS with the larger tolerance in current variation before 1dB compression. Table 2.3 provides a comparison of the relevant performance parameters for the SiGe HBT and CMOS processes.

| Table 2.3: Device performance comparison: 0.18µm SiGe BiCMOS vs. 90nm CMOS. |
|-----------------------------|----------------|----------------|
| Parameter                   | 0.18µm SiGe BiCMOS | 90nm CMOS      |
| Cutoff Frequency ($f_T$)    | 150GHz          | 140GHz (2µm device) |
| Maximum Oscillation Frequency ($f_{MAX}$) | 160GHz          | 175GHz (2µm device) |
| Maximum Available Gain (MAG) @ 60GHz | 10dB            | 8dB             |
| Breakdown Voltage           | 1.8V ($BV_{CEO}$) | 1.5V            |
| Supply Voltage              | 1.8V            | 1V              |
| Peak $f_T$ Current Density  | 1.2mA/µm        | 0.3mA/µm        |
| Peak $f_{MAX}$ Current Density | 1.2mA/µm        | 0.2mA/µm        |

**Biasing for Optimal Performance**

While the concept of biasing transistors at specific current densities for optimal noise, gain and linearity performance has long been in practice for high-speed circuits using bipolar transistors, it has now become equally important in nano-CMOS design where
2.6 Technology Overview

Figure 2.8: Measured $f_T$, $f_{MAX}$ for 90nm CMOS [2].

Figure 2.9: Measured $f_T$, $f_{MAX}$ for SiGe HBT [3].

Figure 2.10: Measured $f_{MAX}$ vs. $I_{DS}/W$ across technology nodes [4].

Figure 2.11: Measured $f_{MAX}$ vs. $V_{GS}$ across technology nodes [4].
the shrinking range of effective gate voltage ($< 300mV$) and larger process variations on $V_T$ make $V_{GS}$- and $V_T$- centric design no longer practical [40].

It has recently been found that the application of constant-field scaling rules to every new generation of CMOS scaling since the $0.5\mu m$ node has resulted in constant peak $f_T/f_{MAX}$ current densities of 0.2-0.3mA/$\mu m$ across foundries and technology nodes [40]. This is in contrast to the SiGe HBTs where the peak $f_T/f_{MAX}$ current bias is technology dependent. Adopting current density-centric biasing for MOSFET designs reduces the $f_T/f_{MAX}$ dependence on process variations of $V_T$ and gate length [40], leading to much more robust designs than biasing at constant $V_{GS}$.

The constant current biasing scheme also has implications on the linearity performance of PAs. The analysis of distortion in PAs is commonly performed using the Volterra series, which represents circuit nonlinearity as a summation of $n^{th}$ order operators. While it is useful in providing insight into the contribution of the various sources of distortion, its lengthy computations make it an unattractive tool for high frequency linearity analysis. A simpler, more effective method is to examine the flatness of the $f_{MAX}$ curve when plotted against $V_{GS}/V_{CE}$ or $I_{DS}/I_C$ [41]. The validity of this method comes from the direct dependence of $f_{MAX}$ on the maximum available gain of a transistor, $G_{MAX}$; and the gain variation with input voltage and current is essentially what defines the PA linearity. As shown in the measured $f_{MAX}$ vs. $I_{DS}/W$ plots across technology nodes (Figure 2.10), the maximum current swing before 1dB gain compression (corresponding to about an 11% decrease in $f_{MAX}$) remains constant at approximately 0.4mA$/\mu m$, while the maximum voltage swing decreases with each new technology node (Figure 2.11). This indicates the need for increased bias currents and larger device sizes with each new generation of scaling. Additionally, to achieve optimal linearity at any technology node, one should bias at slightly higher than peak $f_{MAX}$ (a point that coincides with peak $f_T$), where there is maximum tolerance on the current or voltage swings before gain compression.
2.6.2. Passives

While the performance of the active devices dictate the maximum achievable speed and gain of a circuit, in the design of tuned radio circuits, accurately modeled passives are what ultimately determine the center operating frequency, gain and the amount of power transfer available through optimum impedance matching. Thus, the sizing, modeling and implementation of passive components and parasitics play a critical role in the overall radio circuit design process.

An important benefit that results from operating in the mm-wave regime is the smaller form factor of integrated passives such as inductors and MIM capacitors. The reduction in their footprint above the lossy silicon substrate leads to improved quality factor (Q) and self-resonant frequency and, of course, more compact layouts. High Q inductors are critical in tuned radio circuits, since they dictate the selectivity of the system and help to reduce phase noise in VCOs. In the power amplifier, high Q translates directly to lower loss in the on-chip impedance transformation, thereby improving output power and efficiency.

Inductors

The inductors for both the SiGe HBT and CMOS power amplifiers were synthesized and modeled as multi-turn spirals with the help of the ASITIC software [42]. Microstrip transmission lines are a popular choice for mm-wave power amplifiers [20, 23] due to their higher current-handling capability and the reduced wavelength at mm-waves (2.5mm and 1.88mm for 60 and 80GHz). However, this approach still proves to be more area-intensive than spiral inductors, where mutual coupling in the coils gives rise to larger inductances for the same area. Large inductors can also be effectively realized using stacked structures by taking advantage of the increasing number of metal layers available in advanced (Bi)CMOS processes. The accurate modeling of inductors is critical to radio circuits, and a number of planar and three-dimensional inductors at mm-wave frequencies fabricated at U of T [43] have confirmed the accuracy of the ASITIC modeling tool. Hence, in this thesis, spiral inductors were used extensively in the design of matching networks for predictability in circuit performance and improvement in area consumption.
The inductors were designed with the optimization of Q and self-resonance frequency (SRF) in mind. As a good design practice, the peak-Q frequency (PQF) of the inductors should be higher than the circuit operating frequency, while the SRF should be at least $3 \times$ higher than the operating frequency. The specific design strategies [4,43] include using narrow metals and reducing the diameter to minimize footprint (thereby improving Q) and increasing the metal spacing to weaken the frequency dependence of the inductance caused by the proximity effect. Metal resistance is reduced through using thicker metal layers, as made available by the process. For reliability reasons, the minimum metal width is dictated by the current-handling capability of the metal layer, which is also process-dependent. Octagonal inductors, rather than standard rectangular spirals, were used for the SiGe PA to reduce on-chip radiation effects from the corners and to improve Q.

All inductors were modeled using the 2-$\pi$ network shown in Figure 2.12 [43], which models the substrate as a distributed RC network, while also accounting for the skin effect with a ladder network consisting of $L_f$, $R_f$ and $R_m$. The net result of skin effect is a decrease in the cross sectional area of a conductor, leading to an increase in the RF resistance. Thus, accounting for the skin effect is crucial at high frequencies. The component values were obtained through a Matlab script which fits the model to ASITIC network parameters. Smaller inductances ($<45pH$) were realized as metal strips over silicon or over metal. All inductors were designed to be smaller than required, with the additional inductance being contributed by the interconnects. The inductance values of the interconnects were also validated in ASITIC, after which they were modeled in the schematic as small inductors in series with the inductor 2-$\pi$ model.

**MIM Capacitors**

Metal-insulator-metal (MIM) capacitors were used in the design of matching networks as well as decoupling capacitors in both the SiGe and CMOS PAs. This type of capacitor is formed by a thin layer of dielectric between two floating metals situated high above the substrate. The increase in the density of MIM caps in recent years [44] has helped to reduce die area while thicker, low-resistive metal layers lead to better Q. Parasitic bottom
Figure 2.12: Inductor 2-π model.

plate capacitance is reduced by the distance between the bottom plate and the silicon substrate. All capacitors were sized to be as square as possible to minimize parasitic inductance.

Resistors

On-chip biasing in both PAs was facilitated by the availability of polysilicon resistors in the processes. For the SiGe PA, metal resistors were also available and were used for smaller resistances due to their lower sheet resistance, while unsilicided polysilicon resistors were used to realize larger resistor values. Similar types of resistors were sized in ratios and used in current mirrors for matching purposes. Polysilicon resistors are preferred due to their lower sensitivity to process variations. Only polysilicon resistors were used in the CMOS PA for resistive gate biasing. All resistors were sized to simultaneously meet current driving capability requirements.

2.7. State-of-the-Art

In recent years, the widespread interest from industry and academia in 60GHz radio for consumer applications has fueled considerable progress in the design of mm-wave radio circuits in silicon. The majority of the research effort, however, has been focused on building blocks and the receiver. Below is a brief summary of some mm-wave circuits in silicon reported to date.
Millimeter-wave research here at U of T has produced a 52GHz, 2-stage cascode LNA in 0.18$\mu$m SiGe HBT with 22dB gain and consuming 11.4mA from 3.3V [45], as well as a 65GHz, 2-stage cascode LNA, also in 0.18$\mu$m SiGe HBT, with 14dB gain [46]. The LNAs make use of inductors and transformers to minimize area consumption. A family of differential Colpitts varactor-tuned VCOs and LC oscillators for the 30-122GHz frequency range have also been designed and tested [47]. The 60GHz VCO achieves a phase noise of -103dBc/Hz at 1MHz offset, with a tuning range of 13%. In addition, a 65GHz receiver with 21dB downconversion gain and 12dB noise figure was also implemented in 0.18$\mu$m SiGe HBT [46].

In [26], the feasibility of mm-wave circuits using a mainstream CMOS technology has been demonstrated in the design of two wideband amplifiers in 0.13$\mu$m CMOS. The 40GHz amplifier achieves a peak $S_{21}$ of 19dB, $OP_{1dB}$ of -0.9dBm and IIP3 of -7.4dBm, while consuming 24mA from a 1.5V supply. The 60GHz amplifier has an $S_{21}$ of 12dB, $OP_{1dB}$ of 2dBm and an NF of 8.8dB, while consuming 36mA from a 1.5V supply.

A family of 60GHz transceiver building blocks has been implemented in a 0.12$\mu$m 200GHz $f_T$/$290GHz$ $f_{MAX}$ SiGe bipolar process [20]. These include: a 61.5GHz LNA with 4.5dB NF and 15dB gain, consuming 6mA from 1.8V; a downconverter with 18.6dB conversion gain and 13.3dB NF, consuming 55mA from 2.7V; a balanced 2-stage class-AB PA at 61.5GHz with 10.8dB gain, 11.2dBm P1dB, 4.3% maximum PAE and 16dBm saturated output power, drawing 150mA from 2.5V; and finally, a 67GHz differential Colpitts VCO with phase noise better than -98dBc/Hz at 1MHz offset from the carrier and 3.1% tuning range while drawing 8mA current from 3V. A branchline coupler is also implemented using microstrip transmission lines to provide quadrature LO signals in the downconverter.

One of the most challenging blocks for 60GHz radio, the PLL, has been demonstrated in [48]. The PLL is implemented in a SiGe BiCMOS process with 200-GHz $f_T$/$f_{MAX}$ and has a lock range of 54.5-57.8GHz.

A 60GHz direct-conversion receiver implemented in 0.13$\mu$m CMOS is presented in [25]. Folded microstrip lines are used to create resonance at 60GHz in a common-gate LNA and active mixers. The receiver achieves a voltage gain of 28dB with 12.5dB NF.
2.7 State-of-the-Art

while consuming 9mW from a 1.2V supply.

On the transmitter side, the focus has thus far only been on the PA. The 61.5GHz PA mentioned previously from [20] is one example. A 77GHz PA for automotive radar applications has also been presented in [23]. Fabricated in 0.12µm SiGe with $f_T/207$GHz and $f_{MAX}/285$GHz, this PA employs a balanced two-stage common emitter circuit topology, and is biased in class-AB. The PA draws 130mA from a 2.5V supply, and achieves 6.1dB of power gain and $OP_{1dB}$ of 11.6dBm. Another 77GHz PA in 0.12µm SiGe BiCMOS is reported in [49]. The PA makes heavy use of transmission lines and achieves 17.5dBm maximum output power and 12.8% efficiency. The challenges of PA integration in CMOS at mm-waves have resulted in very little work done in this area. To the best of the author’s knowledge, the highest frequency CMOS PA is at 40GHz, presented in [50]. Implemented as a single-ended, 3-stage cascode in a 0.18µm CMOS process with $f_{MAX}/84$GHz, this PA uses transmission lines as matching elements and achieve a power gain of 7dB and a maximum single-ended output power of 10.4dBm, while drawing 100mA from a 3V supply.

The state-of-the-art in mm-wave building blocks and systems are summarized in tables 2.4 and 2.5.

Table 2.4: State-of-the-art in mm-wave building blocks and systems in silicon.

<table>
<thead>
<tr>
<th>Block/Sys.</th>
<th>Freq.</th>
<th>Technology</th>
<th>Performance</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO</td>
<td>30-122</td>
<td>0.18µm SiGe BiCMOS</td>
<td>60G PN=-104dB/Hz @ 1MHz; 13% tuning</td>
<td>[47]</td>
</tr>
<tr>
<td>VCO</td>
<td>63GHz</td>
<td>0.25µm CMOS</td>
<td>PN=-85dB/Hz @ 1MHz; 4% tuning</td>
<td>[28]</td>
</tr>
<tr>
<td>VCO</td>
<td>64GHz</td>
<td>90nm CMOS</td>
<td>PN=-110dB/Hz @ 10MHz</td>
<td>[27]</td>
</tr>
<tr>
<td>VCO</td>
<td>67GHz</td>
<td>0.12µm SiGe BiCMOS</td>
<td>PN=-98dB/Hz @ 1MHz; 3.1% tuning</td>
<td>[20]</td>
</tr>
<tr>
<td>VCO</td>
<td>77GHz</td>
<td>0.35µm SiGe HBT</td>
<td>PN=-95dB/Hz @ 1MHz; 6% tuning</td>
<td>[22]</td>
</tr>
<tr>
<td>LNA</td>
<td>65GHz</td>
<td>0.18µm SiGe BiCMOS</td>
<td>Gain=14dB, NF=9dB (sim)</td>
<td>[46]</td>
</tr>
<tr>
<td>LNA</td>
<td>61.5GHz</td>
<td>0.12µm SiGe Bipolar</td>
<td>Gain=15dB, NF=4.5dB</td>
<td>[20]</td>
</tr>
<tr>
<td>LNA</td>
<td>60GHz</td>
<td>0.13µm CMOS</td>
<td>Gain=12dB, NF=8.8dB</td>
<td>[26]</td>
</tr>
<tr>
<td>PLL</td>
<td>55GHz</td>
<td>SiGe Bipolar</td>
<td>54.5-57.5GHz Lock Range</td>
<td>[48]</td>
</tr>
<tr>
<td>Rx</td>
<td>65GHz</td>
<td>0.18µm SiGe BiCMOS</td>
<td>Gain=21dB, NF=12dB</td>
<td>[46]</td>
</tr>
<tr>
<td>Rx</td>
<td>60GHz</td>
<td>0.13µm CMOS</td>
<td>Voltage Gain=28dB, NF=12.5dB</td>
<td>[25]</td>
</tr>
</tbody>
</table>
Table 2.5: State-of-the-art in mm-wave PAs in silicon.

<table>
<thead>
<tr>
<th>Freq.</th>
<th>Technology</th>
<th>$P_{sat}$</th>
<th>PAE</th>
<th>Gain</th>
<th>DC Power</th>
<th>Area</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>60G</td>
<td>0.12µm SiGe BiCMOS</td>
<td>11.2dBm(S)</td>
<td>4.3%</td>
<td>10.8dB</td>
<td>2.5V/150mA</td>
<td>2.1×0.8mm²</td>
<td>[20]</td>
</tr>
<tr>
<td>77G</td>
<td>0.12µm SiGe BiCMOS</td>
<td>17.5dBm(S)</td>
<td>12.8%</td>
<td>17dB</td>
<td>1.8V/165mA</td>
<td>1.35×0.45mm²</td>
<td>[49]</td>
</tr>
<tr>
<td>77G</td>
<td>0.12µm SiGe BiCMOS</td>
<td>12.5dBm(D)</td>
<td>3.5%</td>
<td>6.1dB</td>
<td>2.5V/130mA</td>
<td>2.1×0.75mm²</td>
<td>[23]</td>
</tr>
<tr>
<td>24G</td>
<td>0.18µm CMOS</td>
<td>14.5dBm(S)</td>
<td>14.5%</td>
<td>7dB</td>
<td>2.8V/100mA</td>
<td>0.7×1.8mm²</td>
<td>[51]</td>
</tr>
<tr>
<td>27G</td>
<td>0.18µm CMOS</td>
<td>14dBm(S)</td>
<td>8.2%</td>
<td>17dB</td>
<td>3V/100mA</td>
<td>1.2×1.7mm²</td>
<td>[50]</td>
</tr>
<tr>
<td>40G</td>
<td>0.18µm CMOS</td>
<td>10.4dBm(S)</td>
<td>2.9%</td>
<td>7dB</td>
<td>3V/100mA</td>
<td>1.2×1.7mm²</td>
<td>[50]</td>
</tr>
</tbody>
</table>

2.8. Summary

The system-level considerations and possible transmitter topologies for 60GHz radio have been presented in this chapter. The challenges of mm-wave PA implementation in silicon was also discussed, as well as the active and passive device characteristics that play a critical role in design optimization at high frequencies. The goal of this thesis, then, is to advance the state-of-the-art through the implementations of 60GHz transmitters in SiGe BiCMOS and a 60GHz power amplifier in CMOS.
Power Amplifiers in 0.18\SI{}{\mu m} SiGe BiCMOS and 90\SI{}{nm} CMOS

This chapter focuses on the design techniques and considerations of mm-wave Class A power amplifiers in silicon. An overview of the Class A PA design procedure is first presented, followed by detailed discussions of two 60GHz, 3-stage PAs implemented in 0.18\SI{}{\mu m} SiGe BiCMOS and 90\SI{}{nm} CMOS, that further illustrate the concepts presented in the first part of the chapter. Both amplifiers were designed as Class A PAs to meet the linearity requirements of 60GHz radio. The implementation of the PAs in two technologies with comparable $f_T/f_{MAX}$ performance, and both of which are strong contenders for the 60GHz radio application, also facilitate a technology comparison between SiGe HBT and CMOS in terms of the main PA performance criteria of linearity, gain, efficiency and ease of matching.

3.1. Class A PA Design in HBT and CMOS

3.1.1. Determination of DC Operating Points

Figure 3.1 shows a basic Class A stage with inductive loading. The same configuration can also be used in a MOS implementation. The Class A power amplifier is based on the standard small-signal, single-transistor amplifier, but with signal currents that are a significant fraction of the bias level. Class A PAs are biased to operate linearly by staying in the active region in a bipolar implementation, and in the saturation region for a MOS. Among the three single-transistor amplifier configurations, the common-emitter (source) configuration is preferred for its higher gain compared to the common-collector stage, and better stability compared to the common-base.
The loadline technique is an effective means to optimize the linearity of the PA, aiding in the determination of the DC bias current required for a specified load resistance and $O P_{1 \text{dB}}$ output power, under a given supply voltage. According to loadline theory, the maximum power a transistor can deliver to a load is a function of the supply voltage and the maximum current of the transistor. As shown in Figure 3.2, optimum linearity and output power is achieved when the transistor is biased such that the collector voltage swings equally in both the positive and negative directions without entering the cutoff or saturation regions. The inductive load at the collector presents a DC short, allowing the collector voltage to swing symmetrically about $V_{CC}$. The maximum linear output power is given by:

$$P_{\text{max}} = \frac{I_{pk} \times V_{pk}}{2} = \frac{I_{DC} \times (V_{CC} - V_{CE,\text{sat}})}{2}$$  \hspace{1cm} (3.1)$$

where $I_{pk}$ is equivalent to $I_{DC}$ and

$$V_{pk} = V_{CC} - V_{CE,\text{sat}}$$  \hspace{1cm} (3.2)$$

$P_{\text{max}}$ is achieved with an optimal load impedance of:

$$R_{\text{opt}} = \frac{(V_{CC} - V_{CE,\text{sat}})}{I_{DC}}$$  \hspace{1cm} (3.3)$$

where $R_{\text{opt}}$ represents the optimum load impedance seen at the collector node or, in other words, the load required for the PA to deliver maximum power. Thus, the optimum
load impedance for a device is essentially a function of the device itself and the bias point. Additionally, the maximum achievable output power is dependent on the bias current and the supply voltage $V_{CC}$, which is limited by the breakdown voltage of the active device. This is an initial approximation since losses in the matching networks and input/output impedances have not yet been taken into account, but it nevertheless provides a good starting point for the design. Once the bias current has been chosen based on the desired power level, the design procedure essentially becomes that of an impedance transformation between $R_{opt}$ and $R_L$, which is often a 50Ω antenna. Since $R_{opt}$ can potentially become very small, especially in deep-submicron CMOS implementations with low supply voltages and substrate resistivity, the design of a low loss impedance transformation network easily becomes the most challenging aspect of the design process.

The desired linearity of the Class A PA comes at the expense of efficiency. As seen in the above loadline plot, operating with a constant bias current results in the transistor being in the active region at all times, translating to continuous power dissipation. Although the maximum theoretical efficiency of the Class A PA is 50%, much lower values are often achieved in practice due to circuit nonidealities, such as inevitable losses in the interconnects and in the substrate and variations in bias conditions.
3.1.2. Transistor Sizing

For HBT designs, the transistors should be biased at peak $f_T$ for optimal linearity and gain performance. In the $0.18\mu m$ SiGe BiCMOS process, this corresponds to about $1.2mA/\mu m$ for a $V_{CE}$ of $1.5V$. Since the cascode $V_{CE}$ is made larger than that of the input pair to maximize output swing, and peak $f_T$ current density increases with $V_{CE}$, the cascode transistors are sized smaller to maintain peak $f_T$ bias. All transistors are of the “Digital” type which operate at the highest $f_T$. A “high voltage” type of HBT is also available in the design kit, and while it has a $BV_{CEO}$ of $6V$, its $38GHz$ $f_T$ renders it unusable for a $60GHz$ design.

In the case of the MOS PA, biasing at the constant peak $f_T$ current density of $0.3mA/\mu m$ ensures the best compromise between gain and linearity performance.

Based on this discussion and that of section 3.1.1, Table 3.1 summarizes the results of a numerical design example where the device sizes and bias currents needed to achieve $10dBm$ output power in single CE/CS stages are determined, using $0.18\mu m$ SiGe HBT and $90nm$ CMOS devices.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$0.18\mu m$ SiGe BiCMOS</th>
<th>$90nm$ CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>1.8</td>
<td>1</td>
</tr>
<tr>
<td>$V_{CE,sat}/V_{DS,sat}$ (V)</td>
<td>0.5</td>
<td>0.2</td>
</tr>
<tr>
<td>$V_{pk}$ (V)</td>
<td>1.8-0.5=1.3</td>
<td>1-0.2=0.8</td>
</tr>
<tr>
<td>$P_{max}$ Required (mW)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>$I_{pk}$ (mA)</td>
<td>$(2\times10)/1.3=15$</td>
<td>$(2\times10)/0.8=25$</td>
</tr>
<tr>
<td>$J_{peakfT}$ (mA/$\mu m$)</td>
<td>1.2</td>
<td>0.3</td>
</tr>
<tr>
<td>$L_e/W_f$ ($\mu m$)</td>
<td>15/1.2=13</td>
<td>25/0.3=83</td>
</tr>
<tr>
<td>$P_{DC}$ (mW)</td>
<td>1.8$\times$15=27</td>
<td>1$\times$25=25</td>
</tr>
<tr>
<td>Best Theoretical Efficiency (%)</td>
<td>10/27=37</td>
<td>10/25=40</td>
</tr>
</tbody>
</table>

3.1.3. Impedance Matching

The reduced available power gain at mm-waves compared with lower frequencies gives significance to the maximum power transfer theorem, which states that maximum power is delivered to a load when the load and source impedances are conjugately matched. Thus, impedance matching using (ideally lossless) reactive networks is an integral part...
of mm-wave PA design for maximizing power transfer in the operating frequency range. The concepts of quality factor (Q), and resonance are essential to the design of matching networks. The CE/CS stages of Figure 3.3 are loaded with a “tuned tank” consisting of the load inductor $L$, the capacitor $C$ which represents the parasitic transistor capacitances at the collector/drain node, and the resistor $R_p$ which is the equivalent parallel resistance at the resonance frequency $\omega_o$. This is the frequency at which the inductive and capacitive impedances cancel, leaving only the load resistor $R_p$:

$$\left(\omega_o L - \frac{1}{\omega_o C}\right) = 0 \rightarrow \omega_o = \frac{1}{\sqrt{LC}}$$  \hspace{1cm} (3.4)

The tank Q at resonance is given by:

$$Q = \frac{R_p}{|Z_{L,C}|} = \frac{R_p}{\omega_o L} = \omega_o R_p C,$$  \hspace{1cm} (3.5)

where it can be seen that Q increases with larger values of $R_p$. The effect of Q on the bandwidth of the tank circuit can be derived by normalizing the 3-dB bandwidth of the tank, which can be shown to be equal to that of a parallel RC network [38], to the resonant frequency:

$$\frac{BW}{\omega_o} = \frac{1}{RC\omega_o} = \sqrt{\frac{LC}{R}} = \frac{\sqrt{L/C}}{R} = \frac{1}{Q}$$  \hspace{1cm} (3.6)

Clearly, narrower bandwidths result from high values of Q.
With the resonance frequency and Q in mind, the output matching networks for all PA stages designed in this thesis, with the exception of the final HBT PA stage, are implemented as 1-stage L-match networks consisting of the load inductor $L_p$ and a coupling capacitor $C_c$ (Figure 3.4). $L_p$ is chosen such that the real part of the output impedance ($Z_{out}$) is transformed to the desired load resistance value, while $C_c$ reduces the reactive component of $Z_{out}$ to 0. The matching process can be visualized on the Smith Chart (Figure 3.5) where $L_p$ moves $Z_{out}$ onto the $Z_o$ circle, with $Z_o$ being the system characteristic impedance (i.e. 50Ω), and $C_c$ cancels the reactive component to bring $Z_{out}$ along the constant resistance circle to the center of the Smith Chart, representing $R_L$. While sizing $L_p$ to resonate with the parasitic capacitance in the tank maximizes $R_p$ and hence gain, there is also the risk of a lower frequency oscillation if the resonance shifts down in frequency after fabrication, due to excess parasitics. Thus, it is desirable to size $L_p$ to be slightly smaller than the resonance inductance value for better stability.

The lower bound of the value for $L_p$ is set by the reduction in gain, since it can be shown [41] that the maximum power gain ($G$) for the CE/CS stage is directly proportional to the equivalent load resistance ($R_p$):

$$G \approx \left( \frac{f_T}{f} \right)^2 \frac{R_p}{Z_o}$$

(3.7)

where $Z_o$ is the input impedance and $f$ the operating frequency. In addition to capturing the effects of $f_T$, $f$, $R_p$ and $Z_o$ on gain, this expression also indirectly reflects the tradeoff between gain and linearity, since high linearity requires a larger bias current and hence
device size, resulting in larger capacitances that reduce the size of $L_p$ needed to achieve (for example) a 50Ω match at 65GHz. The reduction in gain due to a small $L_p$ can be overcome by matching to a lower impedance, or, in the case of the final PA stage with a fixed 50Ω load, by using a multi-stage matching network which transforms the impedance in incremental steps. This is the motivation behind the 2-stage L-match network used for the final HBT PA stage.

The input matching networks used for the two PAs in this thesis is similar to that used for an LNA design, consisting of an emitter/source inductor which, together with $f_T$, controls the real part of the input impedance $Z_{in}$, and a base/gate inductor which cancels out the imaginary part of $Z_{in}$.

The small signal equivalent circuits for the CE/CS stages in Figure 3.3 are illustrated in Figure 3.6 and are used in the derivation of the input impedance. Based on the equivalent circuits, $Z_{in}$ for the HBT and MOS cases are expressed as:

$$Z_{in,HBT} = g_m \frac{L_E}{C_\pi} + j \left( wL_E - \frac{1}{wC_\pi} \right)$$ (3.8)

$$Z_{in,MOS} = g_m \frac{L_S}{C_{gs}} + j \left( wL_S - \frac{1}{wC_{gs}} \right)$$ (3.9)
Since the $\frac{g_m}{(C_{gs})}$ and $\frac{g_m}{(C_{\pi})}$ terms can be approximated as $2\pi f_T$ and are essentially fixed by the transistor bias, the degeneration inductor ($L_E/L_S$) should be chosen such that the real part of $Z_{in}$ is the source resistance, i.e., $50\Omega$. An inductor ($L_B/L_G$) at the base/gate can be used to cancel out the imaginary part of $Z_{in}$.

$$L_E \rightarrow \text{Re} \left\{ Z_{in,HBT} \right\} = \frac{g_m L_E}{C_{\pi}} \approx 2\pi f_T L_E = 50\Omega$$ (3.10)

$$L_B \rightarrow \text{Im} \left\{ Z_{in,HBT} \right\} = \left( wL_E - \frac{1}{wC_{\pi}} \right) = 0$$ (3.11)

$$L_S \rightarrow \text{Re} \left\{ Z_{in,MOS} \right\} = \frac{g_m L_S}{C_{gs}} \approx 2\pi f_T L_S = 50\Omega$$ (3.12)

$$L_G \rightarrow \text{Im} \left\{ Z_{in,MOS} \right\} = \left( wL_S - \frac{1}{wC_{gs}} \right) = 0$$ (3.13)

A more rigorous analysis using Y-parameters can also be applied in comparing the input and output impedance, gain and isolation of the MOS and HBT single-transistor and cascode topologies [41].

With the input impedance of the MOSFET being predominantly capacitive and hence high in Q, matching the real part of the MOSFET $Z_{in}$ to $50\Omega$ using a reasonable size of $L_S$ can become a daunting task. The size of $L_S$ is limited by the technology-dependent L-SRF product, with a minimum SRF of 120GHz required for a 60GHz application. A large $L_S$ also leads to a reduction in gain, since the gain is roughly proportional to the ratio of the drain to source inductances, provided that both inductors are operating well below their self-resonant frequencies and hence behave as true inductors. The MOS input match can be made easier by slightly increasing the gate width for a larger $R_g$, bringing
3.1 Class A PA Design in HBT and CMOS

\[ \Re\{Z_{in}\} \text{ closer to the source impedance. Input matching of the CE stage, on the other hand, is easier in light of the smaller Q of the HBT due to the presence of } r_\pi. \text{ The situation is reversed in the output match, with the Q of the HBT being higher than that of the MOS, making it harder to achieve broadband match in an HBT output stage.} \]

3.1.4. Stability and the Impact of Parasitics

The root-locus technique involving the calculation of poles and zeros of an amplifier and examining their movement in the s-plane is a popular method of stability analysis in analog design, but does not find much use at microwave and mm-wave frequencies where it is often difficult to identify the feedback loops that cause instability. Instead, the Rollett stability factor, \( k \), is employed for the 2-port representation of a single-stage amplifier and is based on the input and output reflection coefficients \( (S_{11}, S_{22}) \) and the forward and reverse transmission coefficients \( (S_{21}, S_{12}) \) [52]:

\[
k = \frac{1 + |\Delta|^2 - |S_{11}| - |S_{22}|^2}{2|S_{21}| |S_{12}|} \tag{3.14}
\]

where \( \Delta = S_{11}S_{22} - S_{12}S_{21} \). If \( k > 1 \) and \( \Delta < 1 \), the circuit can be said to be unconditionally stable, regardless of the passive matching impedances presented at the amplifier input and output. The main drawback of the \( k \)-factor stability analysis is that it provides little insight into the causes of instability, other than indicating that stability tends to improve with good reverse isolation (low \( S_{12} \)). This analysis is also unsuitable for multi-stage amplifiers if interstage matching is not implemented, since the input and output of an intermediate stage would be terminated with active networks. Thus, verifying the \( k > 1 \) criteria is a necessary, but by no means sufficient, step in stability analysis.

A good design practice for mm-wave PAs, where the circuit complexity is lower and the impact of parasitics is much more significant than at lower frequencies, is to also examine the critical nodes that may affect stability. For the cascode topology, two such critical nodes are the cascode base and the emitter of the input transistor (Figure 3.7). Any parasitic inductance at the cascode base and parasitic capacitance at the emitter of the input transistor creates series feedback and may result in negative input resistance,
which is one of the conditions for sustained oscillation. Although the example given below is for an HBT implementation, the same applies for the MOS case.

![Parasitic base inductance and emitter capacitance.](image)

In the case of emitter capacitance, the input impedance can be found to be:

\[
Z_{\text{in}} = -\frac{g_m}{\omega^2 C \pi C_E} + \frac{1}{j \omega C \pi} + \frac{1}{j \omega C_E},
\]  
(3.15)

where \( \Re \{Z_{\text{in}}\} < 0 \).

For the cascode inductance, the input impedance looking into the emitter of the cascode is:

\[
Z_{\text{in}} = \frac{1 - \omega^2 C \pi L_B}{g_m + j \omega C \pi},
\]  
(3.16)

where \( Z_{\text{in}} \) becomes negative when \( \omega^2 C \pi L_B > 1 \). This indicates that larger devices with higher \( C \pi \) have a higher tendency to oscillate. To prevent, or minimize, the risk of oscillation, a series resistance can be added to the base of the cascode to compensate for the possible negative resistance. This is done at the expense of reduced gain and linearity.

### 3.1.5. Maximizing Input and Output Linearity

The use of inductive emitter degeneration in the input matching has the added benefit of improving the linearity of the CE stage, since the maximum input voltage \( V_{pk} \) for linear operation can be approximated as the voltage drop across the degenerating inductor:

\[
V_{LE} = I_E \times \omega L_E,
\]  
(3.17)
Thus, increasing the bias current and/or $L_E$ improves the input linearity, but at the cost of lower gain due to feedback. For the CS stage, the maximum input voltage, $V_{pk}$, also includes $V_{eff}$:

$$V_{LS} = \frac{V_{eff}}{2} + I_D \times \omega L_S.$$  \hspace{1cm} (3.18)

Thus, the MOS amplifier is inherently more linear than the HBT for the same current and degenerating inductor size. Additionally, the MOS amplifier is less sensitive than the HBT to the effect of the degenerating inductor on linearity.

On the output side, an inductive load allows the collector/drain voltage to swing above the rail by an amount given by $R_p \times I_C$, which represents the upper limit on the output swing. The lower limit is set by the $V_{CE} - V_{CE,sat}$ or $V_{DS} - V_{DS,sat}$ of the output transistor. Thus, maximum output swing is achieved with the largest $R_p$ value possible, as dictated by the Q of the inductor, the bias current and the largest $V_{CE}$ or $V_{DS}$ across the transistor before breakdown.

$$V_{o,max} = \min \{V_{CE} - V_{CE,sat}, I_C \times R_P\}$$ \hspace{1cm} (3.19)

$$= \min \{V_{DS} - V_{DS,sat}, I_D \times R_P\}$$ \hspace{1cm} (3.20)

$$P_{out} = \frac{I_{DC} \times V_{o,max}}{2}$$ \hspace{1cm} (3.21)

### 3.1.6. Multi-Stage PA Design

In light of the $\approx 10$dB maximum available gain that one can expect from an HBT and $\approx 8$dB from a 90nm MOSFET, the achievable stage gain is often 3-4dB lower due to the limited maximum load impedance that can be realized at the collector/drain output at high frequencies, the losses in the matching networks and other circuit non-idealities. This indicates the need for multiple stages to achieve an adequate amplifier gain of $\geq 10$dB, especially in the case of CMOS. Driver stages with smaller device sizes and lower current consumption can be used to improve the overall system gain, while also easing the input matching process. A third benefit of a multi-stage design is the potential improvement in bandwidth through the use of techniques such as stagger-tuning. The $S_{21}$ bandwidth for
3.2 Summary

A single stage is dependent on the Q of the output tank. But by designing the individual stages for slightly different center frequencies, a wider bandwidth can be achieved for the cascade.

The amplifier stages should be designed beginning with the final PA stage, followed by each preceding stage so that the input and output compression points of each individual stage is optimized. Interstage matching is a good practice for maximizing power transfer and reducing the risk of instability.

3.2. Summary

The design methodology and considerations for mm-wave PAs in HBT and CMOS have been presented. The following sections build upon this discussion by providing two specific examples of PAs designed in 0.18\textmu m SiGe BiCMOS and 90\textit{nm} CMOS.

3.3. 3-Stage PA in 0.18\textit{um} SiGe BiCMOS

3.3.1. Design and Analysis

The 3-stage Class A PA in 0.18\textit{um} SiGe BiCMOS is designed to be a part of the 60GHz single-sideband transmitter discussed in Section 4.2. Since, in the transmitter, the role of the PA is to provide sufficient gain at 60GHz to compensate for the losses in the polyphase filters, while also exhibiting high linearity as expressed through the 1-dB compression point, a 3-stage topology is chosen for high gain, with each stage implemented as a cascode differential amplifier with scaled currents and inductive degeneration for linearity. The high reverse isolation offered by the cascode topology greatly simplifies the matching procedure by allowing the input and output matching networks to be independently optimized. This is especially significant for the 3-stage PA, where on-chip conjugate matching techniques are used extensively for inter-stage as well as input/output matching to maximize power transfer and to avoid instability due to reflections.

The design specifications for the PA are summarized in Table 3.2. Since a separate breakout test structure of the PA was fabricated with the intention of block-level char-
acterization, the PA was matched to 50Ω single-endedly at both the input and output to accommodate the 50Ω testing environment.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>3.3</td>
</tr>
<tr>
<td>Frequency Range (GHz)</td>
<td>56-70</td>
</tr>
<tr>
<td>$P_{1dB, out}$ (dBm)</td>
<td>&gt; 5 (differential)</td>
</tr>
<tr>
<td>$S_{21}$ (dB)</td>
<td>&gt; 15</td>
</tr>
<tr>
<td>$S_{12}$ (dB)</td>
<td>&lt; −40</td>
</tr>
<tr>
<td>$S_{11}$, $S_{22}$</td>
<td>&lt; −15</td>
</tr>
<tr>
<td>$Z_{in}$ (Ω)</td>
<td>50 (single-ended)</td>
</tr>
<tr>
<td>$Z_{out}$ (Ω)</td>
<td>50 (single-ended)</td>
</tr>
</tbody>
</table>

The schematics of the final PA stage and the first two driver stages are shown in Figures 3.8 and 3.9.

To maximize linearity, the design begins with the final stage, where the tail current is computed based on the desired output power and collector swing:

$$I_{pk} = \frac{P_{avg} \times 2}{V_{pk}} = \frac{10\text{mW} \times 2}{1.1V} = 18\text{mA}$$ (3.22)

The corresponding $I_{tail}$ for the differential circuit is 36mA, which is very close to the actual tail current of 37mA used in the final stage. The second stage should deliver at least the same amount of power as the $IP_{1dB}$ point of the third stage:

$$\text{OP}_{1dB_{stage2}} \geq \text{IP}_{1dB_{stage3}} \geq \text{OP}_{1dB_{stage3}} - (G_{stage3} - 1)$$ (3.23)

The tail current for the second stage can then be determined in a similar manner as (3.22), given that the target $OP_{1dB}$ is at least 5.1dBm (3mW):

$$I_{pk} = \frac{P_{avg} \times 2}{V_{pk}} = \frac{3.2\text{mW} \times 2}{1.1V} = 5.8\text{mA}$$ (3.25)
The differential $I_{\text{tail}}$ required for the second stage is 11.6mA, which is also close to the actual tail current of 15mA used for that stage. The same design procedure, involving the $IP_{1dB}$ of the second stage, also applies to the first stage:

$$OP_{1dB_{\text{stage1}}} \geq IP_{1dB_{\text{stage2}}} \geq OP_{1dB_{\text{stage2}}} - (G_{\text{stage2}} - 1)$$

Here, the calculated differential current is 3.2mA, for an $OP_{1dB} > -0.5$dBm. The actual current used is 9mA. The need for the higher current in the actual design compared with calculation may be due to the lack of inductive degeneration in the first stage for high gain. A larger current helps to ensure that the stage will not be limited by its input compression, in the absence of degeneration.

The choice of the interstage matching impedance between two stages affects both the
gain of the first stage and the input compression of the second, as it determines the amount of inductive degeneration available. The input linearity of the final PA stage is the most critical due to the high input power level at that stage. An interstage matching impedance of 60Ω differential is used between the second and third stages, while that between the first and second is 80Ω differential for a good compromise between gain in the first stage and input linearity in the second.

The transistors are biased at close to peak \( f_T \) for optimal linearity. Multiple base contacts are used in all HBTs to reduce base resistance for a high \( f_{MAX} \). Double collector contacts are used for lower collector resistance, but at the expense of higher \( C_{cs} \) and larger footprint. The emitter width of 0.2\( \mu \)m is used for all transistors to minimize the base resistance and parasitic junction capacitances \( C_{je} \) and \( C_{jc} \), leading to high \( f_T \) and \( f_{MAX} \). Multiple emitter fingers are employed for smaller footprint and lower parasitic capacitance with only a small penalty in collector resistance.

In addition to checking the \( k \) stability factor (simulated value of 1060 at 65GHz), small resistances (6 – 9Ω) are also placed at the base of the cascodes in all stages to

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prevent oscillation due to negative resistance looking into the bases of the cascodes. At the output of the final PA stage, a 2-stage L-match scheme is employed to broaden the output match bandwidth. Four 17fF pad capacitances, one for each signal pad, are also accounted for in the input and output match. This pad capacitance value is based on measurements of previously fabricated pad structures in the same technology.

For each of the PA stages, on-chip biasing is implemented using the current mirror with base-current compensation shown in Figure 3.10. The current ratio is established through \( Q_1:Q_3, R_3:R_B \) and \( R_4:2R_5 \), with the ratio \( k \) for stages 1, 2 and 3 being 4.5, 10.5 and 10 respectively. A minimum voltage drop of 150mV (6\( V_T \)) is set for \( R_4 \) and \( R_5 \) to ensure sufficient feedback through the degenerating resistor \( R_4 \) which desensitizes the reference current to ground resistance and changes in the \( V_{BE} \) of Q3. The addition of transistor \( Q_4 \) reduces the dependence of \( I_T \) on \( \beta \) by supplying the base currents of both \( Q_1 \) and \( Q_3 \) through its emitter. Voltage bias for the cascode pair is provided by the resistive divider formed by \( R_1 \) and \( R_2 \). Decoupling capacitors \( C_1 \) and \( C_2 \) create AC grounds at the bias nodes to minimize supply noise. They are each sized to be 2pF as a compromise between die area and low impedance at 65GHz.

![Figure 3.10: Bias circuitry for SiGe PA.](image-url)
3.3 3-Stage PA in 0.18µm SiGe BiCMOS

3.3.2. Circuit Simulations and Layout

The performance of each of the three stages is summarized in the block diagram shown in Figure 3.11. All S-parameter and compression point results are obtained using Spectre, and are extracted at 64GHz, which is the optimum operating frequency for the PA. Since the stages are stagger-tuned for a more broadband response, the gains at 64GHz do not necessarily reflect the peak gains of the stages. The "S" and "D" in the interstage matching refer to single-ended or differential, while all P1dB values refer to differential configurations.

![Figure 3.11: Summary of simulated 3-Stage HBT PA performance.](image)

The single-ended S-parameter and linearity performance for the 3.3V 3-stage cascade are shown in Figures 3.12 and 3.13. The reflection coefficients ($S_{11}$ and $S_{22}$) should ideally be $<-15$dB in simulation to guard against parasitics and process variations. A gain ($S_{21}$) of 17.2dB is achieved across the 3 stages, while the overall $OP_{1dB}$ is 7.1dBm differential. Simulated S-parameters and compression point for the final PA stage are also shown in Figures 3.14 and 3.15. While the addition of the first two driver stages greatly improves the overall gain and helps ease the task of matching to the 50Ω source impedance, it also leads to a degradation in linearity. The overall $S_{21}$ bandwidth is improved by stagger-tuning the stages, with stages 1, 2, and 3 centered at 69GHz, 59GHz and 60GHz, respectively (Figure 3.16). The selection of the center frequency for each stage is based on attaining a good compromise between bandwidth improvement and the corresponding gain degradation at the cascade center frequency due to stagger-tuning.
Figure 3.12: Single-ended S-parameter simulation of 3-Stage PA.

Figure 3.13: Simulated differential $OP_{1dB}$ compression point of 3-Stage HBT PA at 64GHz.

Figure 3.14: Single-ended S-parameter simulation of final HBT PA stage.

Figure 3.15: Simulated differential $OP_{1dB}$ compression point of final HBT PA stage at 64GHz.
Figure 3.16: Gain distribution of cascade showing the use of stagger tuning.

Figure 3.17 shows the full layout of the $800 \times 600 \mu m^2$ 3-stage PA. All inductors are realized as octagonal spirals to minimize footprint and antenna effects. High speed signals are routed in the top metal layers for minimal substrate capacitance, while bias lines are implemented in layers 3 and 4 and made as wide as possible to improve supply-decoupling and minimize inductance. Additional localized de-coupling is also provided by five 2.5pF MIM capacitors. Three separate bias pads allow independent bias control for each stage.
3.4. 3-Stage PA in 90nm CMOS

3.4.1. Design and Analysis

A 3-stage PA was also designed and fabricated in a 90nm RF CMOS process to investigate the merits of using CMOS for mm-wave radio design. It is based on a single-ended CS topology with inductive degeneration and interstage matching, and drives a 50Ω load. Although the cascode topology is suitable as an output stage for a PA due to its higher output impedance and flat $V_{DS}$ characteristic, which reduces voltage-induced distortions, the single-transistor CS configuration is advantageous in terms of the lower circuit complexity and lower supply voltage, which leads to higher efficiency. The main drawback of the single transistor topology is the reduced reverse isolation, which complicates the input/output matching process. The initial design goals are summarized in table 3.3.

Unlike in the HBT case where the currents are scaled in ratios of > 1, the last 2
3.4 3-Stage PA in 90nm CMOS

Table 3.3: Performance specifications for 90nm CMOS PA.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>1-1.5</td>
</tr>
<tr>
<td>Frequency Range (GHz)</td>
<td>56-70</td>
</tr>
<tr>
<td>$P_{1dB,\text{out}}$ (dBm)</td>
<td>&gt; 5 (single-ended)</td>
</tr>
<tr>
<td>$S_{21}$ (dB)</td>
<td>&gt; 5</td>
</tr>
<tr>
<td>$S_{11}, S_{22}$</td>
<td>&lt; −15</td>
</tr>
<tr>
<td>$Z_{in}$ (Ω)</td>
<td>50 (single-ended)</td>
</tr>
<tr>
<td>$Z_{out}$ (Ω)</td>
<td>50 (single-ended)</td>
</tr>
</tbody>
</table>

Stages in the CMOS PA are designed to have similar tail currents to maximize the overall linearity. As always, the design begins at the output stage, where the main optimization target is linearity. The tail currents are determined based on the calculation shown in Table 3.1. With a supply voltage of 1V and the 3 stages using 12.9mA/14.5mA/16.1mA, the PA achieves an overall $OP_{1dB}$ of 6.5dBm and gain of 12.6dB. The gain is distributed as 3dB/4.6dB/4.4dB across the 3 stages. Although the first stage generally has a higher gain in a multi-stage PA since its linearity requirement is the least stringent, in this case, the first stage gain is lower due to the large degeneration inductor needed to match the high-Q input to 50Ω. Fortunately, the gain of the first stage does not factor into the overall linearity of the cascade, as seen in equation 3.28, and is significant only when an overall high gain is desired, as in the case of the HBT PA where it is needed to improve the transmitter system gain. The heavy degeneration in the first stage does help with the $IP_{1dB}$, since it plays a dominant role in the overall input compression (equation 3.29).

\[
\frac{1}{OP_{1dB,\text{cascade}}} = \frac{1}{OP_{1dB_1} \cdot G_2} + \frac{1}{OP_{1dB_2} \cdot G_3} + \frac{1}{OP_{1dB_3}} \quad \text{(3.28)}
\]

\[
\frac{1}{IP_{1dB,\text{cascade}}} = \frac{1}{IP_{1dB_1}} + \frac{G_1}{IP_{1dB_2}} + \frac{G_1 \cdot G_2}{IP_{1dB_3}} \quad \text{(3.29)}
\]

All transistors are biased at close to the peak $f_T$ current density for MOSFETs — 0.3mA/µm — for optimal linearity. A finger width of 1µm was chosen for the transistors to minimize the effect of the gate series resistance $R_g$, thereby limiting reductions in $f_{MAX}$ due to resistive losses, while also avoiding $f_T$ degradation due to $C_{GBO}$. The gates are contacted on one side to minimize gate-drain overlap capacitance, $C_{gd}$, with the gate...
resistances modeled using (3.30).

\[
R_g = \frac{R_{gsq} W_f}{3 N_f l_g} + \frac{R_{cont}}{N_{cont} N_f} + \frac{R_{gsq} l_{access}}{N_f l_g},
\]  

(3.30)

where \(R_{gsq}\) is the gate sheet resistance per-square, \(W_f\) is the finger width, \(N_f\) is the number of fingers, \(l_g\) is the gate length, \(l_{access}\) is the contact-to-gate distance, \(R_{cont}\) is the contact resistance and \(N_{cont}\) the number of contacts. The gate length in this case refers to the physical gate length of 65nm, which corresponds to the width of the polysilicon trace.

The output matching networks are designed using the 1-stage L-match scheme consisting of the load inductor \(L_C\) and the coupling capacitor \(C_C\). Each stage is input-matched with \(L_G\) and \(L_S\) for tuning out the imaginary and real parts of the input impedance. The coupling capacitors, \(C_c\), used in the interstage matching allow each stage to be biased independently with resistive gate biasing through 5kΩ resistors.

The inductive degeneration in each stage, as part of the interstage matching, also improves the input linearity by increasing the allowable input voltage swing. The interstage matching impedances of 15Ω and 25Ω ease the task of matching the inputs of stages 2 and 3, due to the high-Q nature of the MOSFET input, as well as simplifying the interstage output matching, since the output impedance is always less than 50Ω. Similar to the case of the HBT PA, the sizes of the interstage matching impedances are chosen to achieve a good compromise between the gain of the previous stage (requiring a high impedance), the gain of the following stage (requiring a low impedance) and the linearity of the following stage (improved with a higher impedance). As an example of the linearity improvement in the MOS case, with 60pH of degeneration inductance, 14.5mA bias current and \(V_{eff}\) of 0.5V, the second stage allows up to 1.2\(V_{ppk}\) of maximum input swing, compared with only 0.5\(V_{ppk}\) in the case with no degenerating inductor.

The schematic of the PA, including all component values and DC settings in simulation, is shown in Figure 3.18.
3.4 3-Stage PA in 90nm CMOS

Figure 3.18: Schematic of 3-Stage CMOS PA.
3.4.2. Circuit Simulations and Layout

The simulated performance of the 3-stage design at 65GHz is shown in Figures 3.19 and 3.20. The simulation captures the effects of inductor 2-π models, all interconnect inductances and pad capacitances (20fF per signal pad). Since most of the spiral inductors are < 100pH, and hence lower in Q than larger inductors due to a smaller ratio of the imaginary-to-real components, the resulting PA is fairly broadband, with a 3-dB BW covering 61-74GHz. The simulated $OP_{1dB}$, with a 1V supply and $V_g$ of 0.8V, is 6.5dBm. Under this operating condition, the total efficiency is 10.3%.

The relatively poor isolation of the CS topology compared with the cascode results in a simulated $k$ stability factor of 4 at 65GHz, which, by being greater than 1, still ensures unconditional stability. The advantage of CMOS power amplifiers is that the risk of oscillations is lower than in an HBT design, due to the lower $g_m$ of the MOS compared with an HBT, which makes the realization of negative resistance more difficult.

The PA layout consists of two sets of ground-signal-ground pads for the single-ended input and output signals, and a set of power-ground-power pads for $V_{DD}$ and gate bias for the second and third stages. The first stage can be biased using a bias-T at the input signal pad. Taking advantage of the excellent backend of the RF CMOS process, spiral inductors are implemented in the top metal layer to minimize substrate capacitance. Although the inductors are small enough to be implemented as microstrip lines over silicon or over metal for lower loss, the spiral inductor implementation is chosen to maximize the Q while minimizing area consumption. The final design is essentially pad-limited vertically. Four 2pF MIM capacitors provide localized bias and power decoupling. The provision of a large metal ground plane with ample substrate contacts is crucial to reducing substrate resistance and ground inductance. Hence, the chip is covered with as much of metal 1 as possible while still adhering to the metal density rules. Each transistor is laid out with the minimization of parasitics in mind. Specifically, sources are contacted on the outside while drains on the inside to reduce the number of drain fingers and hence $C_{db}$ — the dominant capacitance in a MOSFET. Gates are contacted on 1 side to avoid metal overlap between gate and drain, hence minimizing $C_{gd}$. 
3.4 3-Stage PA in 90nm CMOS

![Graph showing S-Parameters (dB)](image1)

**Figure 3.19:** Simulated S-Parameter performance for CMOS PA ($V_{DD}=1V$).

![Graph showing RF Input Power vs. RF Output Power](image2)

**Figure 3.20:** Simulated 1dB compression point of 3-Stage CMOS PA at 65GHz ($V_{DD}=1V$).

![Diagram of 3-Stage CMOS PA layout](image3)

**Figure 3.21:** Layout of 3-Stage CMOS PA.
3.5. HBT vs. CMOS PA Implementation

Table 3.4: Performance comparison for 0.18\(\mu\)m SiGe BiCMOS PA and 90\(nm\) CMOS PA.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>0.18(\mu)m SiGe BiCMOS</th>
<th>90(nm) CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{1dB,\text{out}}) (dBm)</td>
<td>7.14 (D)</td>
<td>6.5 (S)</td>
</tr>
<tr>
<td>(S_{21}) (dB)</td>
<td>17.2</td>
<td>12.6</td>
</tr>
<tr>
<td>3dB BW (GHz)</td>
<td>56-70</td>
<td>61-74</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>3.3</td>
<td>1</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>193.2</td>
<td>43.5</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>2.7</td>
<td>10.3</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>2.6</td>
<td>9.8</td>
</tr>
<tr>
<td>FoM</td>
<td>27.2</td>
<td>33.6</td>
</tr>
</tbody>
</table>

Table 3.4 summarizes the performance of the HBT and CMOS PAs. In terms of the PA FoM, both PAs have comparable performance, with the CMOS PA having a slightly higher FoM. The low supply voltage in nano-scale CMOS, combined with the inherently better linearity of the MOSFET device, result in much better PA efficiency and power consumption. The flatness of the MOSFET \(f_{\text{MAX}}\) vs. \(V_{\text{GS}}\) curve at the peak is an accurate indication of its stronger linearity performance, while also providing information regarding the allowable input/output voltage swing. The SiGe HBT implementation is well-suited in cases where a high gain is desired.

In terms of matching, the high-Q input of the MOSFET makes matching to a 50\(\Omega\) source impedance a daunting task. However, it is relatively easier to attain a broadband output match at the MOSFET output compared with the HBT, where a multi-stage matching network may be needed to broaden the bandwidth and match to 50\(\Omega\).

With the continued scaling of CMOS comes the inevitable reduction in breakdown voltage, which dictates the need for larger bias currents to achieve the same level of output power. This, in conjunction with the constant current biasing scheme, leads to larger device sizes and hence smaller output impedances, which complicates the output matching process. Hence, while PAs implemented in older technology nodes, such as 0.13\(\mu\)m CMOS, may not achieve the same speed and gain as in the 90\(nm\) node due to the lower \(f_T/f_{\text{MAX}}\), their higher breakdown voltage and larger \(V_{\text{DS}}\) swing before 1dB compression (Figure 2.11) allow for lower bias currents to generate the same output power, and hence allow for easier impedance matching to 50\(\Omega\). Similarly, the III-V
technologies, and even SiGe HBTs, have a clear advantage over CMOS in PA design due to their higher breakdown voltage.

Reducing the overall circuit complexity is key to achieving good linearity and gain performance at mm-waves. Smaller number of active components leads to fewer sources of nonlinearity. Thus, PA design, to a large extent, becomes device design, where the size and layout of the individual transistor are what determines the optimal PA performance. Of course, the accurate modeling of passives in the matching networks are the other half of the equation, and play an equally crucial role in maximizing the gain and linearity.

### 3.6. Summary

The steps and considerations in mm-wave PA design have been discussed and illustrated in the implementation of two 3-stage power amplifiers in SiGe HBT and CMOS. The two PAs serve to demonstrate the strengths and weaknesses of each technology in terms of the PA performance criteria. It has also been shown that a CMOS PA implementation is not only feasible, but also yields good linearity and efficiency, hence suggesting the suitability of an all-CMOS implementation of a 60GHz radio system.
4 60GHz Transmitters in 0.18µm SiGe BiCMOS

This chapter presents the designs of a 65GHz directly modulated BPSK transmitter and a 60GHz single-sideband transmitter with 5GHz IF and on-chip image rejection. Both transmitters were implemented in the 0.18µm SiGe BiCMOS technology described in section 2.6.1. The two designs, representing the direct modulation and the heterodyne approaches, offer a comparative look at the performance, complexity and feasibility of different 60GHz transmitter implementations.

4.1. 65GHz BPSK Transmitter in 0.18µm SiGe BiCMOS

4.1.1. BPSK Modulation

BPSK and BFSK are two closely related, one-dimensional forms of digital modulation with the advantage of being simple to generate and detect. Their lower sensitivity to amplitude noise makes them more suitable for RF applications than ASK. Although their spectrum usage is not as efficient as some of the more sophisticated modulation schemes, they do have the advantage of being detectable at very low SNR, with BPSK having a 3dB theoretical advantage over BFSK [38].

BFSK typically involves the direct modulation of a VCO to generate the discrete frequencies. One of the earliest 60GHz radio MMIC implementations involves an FM/FSK modulator with a dielectric resonator for VCO stabilization [10], to minimize drift in the

\textsuperscript{1}as opposed to two-dimensional types such as QPSK where two independent signals are used to create the symbols
VCO frequency due to time and variations in temperature and power supply. On the other hand, BPSK can be implemented simply as the carrier phase shift between two discrete values as a function of the binary data. To improve the ease of demodulation, the phase shift can be maximized by flipping the polarity of the two states, resulting in a 180° phase shift of the carrier for each data transition. This also leads to a simpler method of modulation, where the phase shift results from the multiplication of the carrier with the binary data. Figure 4.1 illustrates this concept.

\[
x_{\text{Baseband}}(t) \times A_c \cos(\omega_c t + \phi) = x_{\text{BPSK}}(t), \quad \phi = 0^\circ \text{ or } 180^\circ
\]

Figure 4.1: BPSK Modulation

The 65GHz BPSK transmitter takes advantage of the robustness and integration potential of the BPSK scheme to realize direct modulation, whereby the baseband data signal, in the range of 1-2GHz, is directly applied to a 65GHz oscillator through emitter followers and modulates the oscillator outputs through a mixing quad. The elimination of the upconversion mixer and power amplifier results in a novel and compact transmitter implementation, suitable for a variety of low-cost applications.

4.1.2. Circuit Design

The schematic of the transmitter is shown in Figure 4.2. It consists of three main parts: the Colpitts oscillator core, the mixing quad, and a set of emitter followers with current...
mirrors for biasing. Details on the design of each part are presented in the following sections.

Figure 4.2: 65-GHz BPSK transmitter schematic.

Colpitts Oscillator

The carrier in the BPSK transmitter is supplied by a Colpitts oscillator optimized for low phase noise\(^2\). The reader is referred to [53] for a detailed analysis and design procedure for low phase noise mm-wave VCOs. A brief discussion of the oscillator circuit and design considerations is presented here for a more complete understanding of the overall transmitter circuit.

\(^2\)The oscillator was originally designed by C. Lee [53]
One of four types of selective feedback LC VCOs (Colpitts, Clapp, Armstrong, Hartley), the Colpitts topology is best-suited for mm-wave HBT implementations due to its better isolation between the resonant tank and the output, as compared with the cross-coupled VCO, which also finds use at mm-waves. Negative resistance and low phase noise are also easier to achieve with the Colpitts topology at high frequencies [38].

Figure 4.2 shows the schematic of the BPSK transmitter with the Colpitts oscillator core operating on the fundamental. A differential cascode topology is employed in the oscillator for higher output power and better tank isolation. The resonant tank is formed by the inductor $L_B$ and capacitors $C_1$ and $C_2$, which constitute a capacitive divider with an equivalent capacitance of $C_{EQ}$. Since relatively large transistors are used to accommodate the large bias current required for low phase noise, capacitor $C_1$ is simply the $C_{BE}$ of transistors Q5 and Q6. Negative resistance seen looking into the base of Q5 or Q6 is generated by the capacitive degeneration of transistors Q5 and Q6, and is given by:

$$-R_P = -\frac{g_m}{\omega^2 C_1 C_2} + R_{BB},$$

where $R_{BB}$ is the transistor base resistance.

Since the amount of negative resistance must exceed the resistive losses in the tank at the frequency of interest for sustained oscillation, a high Q tank is desirable to reduce the amount of negative resistance needed. The oscillation frequency is set by the values of the passive components in the tank:

$$f_{osc} = \frac{1}{2\pi \sqrt{L_{tank} C_{EQ}}} = \frac{1}{2\pi \sqrt{L_{tank} \left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

Low phase noise is achieved through a number of design techniques. Based on the modified Leeson’s phase noise formula for the Colpitts topology (equation 4.3) [4], where $I_n$ is the equivalent noise current at the input of the negative resistance transistor and $V_{osc}$ is the tank voltage swing, phase noise is minimized with a high bias current and a
high tank Q. $C_1$ should also be maximized to improve phase noise.

$$L(f_m) = \frac{|I_n|^2}{V_{osc}^2} \times \frac{1}{f_m^2} \times \frac{1}{C_1^2 \left( \frac{C_1}{C_2} + 1 \right)^2} \quad (4.3)$$

Additionally the transistors are biased at the minimum noise figure current density ($J_{NF_{\text{min}}}$) of the cascode configuration. Inductive degeneration through $L_{E1}$ further improves phase noise, while inductors $L_{E2}$ isolate the half circuits to allow a single tail bias. The sizes of $L_{E1}$ and $L_{E2}$ are bounded by conditions 4.4 and 4.5 [4]. A common-mode resistor is used for biasing and, together with a parallel capacitor which shunts the high frequency noise from the resistor to ground, ensures lower phase noise than a transistor current source.

$$f_{osc} < \frac{1}{2\pi \sqrt{L_{E1}C_2}} \quad (4.4)$$

$$f_{osc} > \frac{1}{2\pi \sqrt{L_{E2}C_2}} \quad (4.5)$$

The oscillator is matched to 50Ω at the output through the matching network consisting of $R_C$ and $L_C$. The negative resistance transistors and cascode transistors are all biased through resistive divider networks connected to $V_{DD}$ with $\approx 200\text{fF}$ decoupling capacitors. The oscillator uses a 4V supply and has a tail current of 52mA.

**Mixing Quad and Emitter Follower Integration**

The BPSK transmitter (Figure 4.2) is implemented by integrating a mixing quad (transistors Q1-Q4) with the Colpitts oscillator. The mixing quad replaces the cascodes of the original oscillator, as well as the resistive divider bias circuitry. BPSK modulation is accomplished by redirecting the output of the oscillator (collectors of Q5 and Q6) between the positive and negative outputs of the mixing quad, under the control of the data input. The transistors in the mixing quad have a $V_{CE}$ of 1.8V, limited by transistor breakdown, to maximize the output swing. The mixing quad is driven by a set of emitter followers which serve two important functions. First, they provide buffering between the mixing quad and the input signal pads, and allow for on-chip 50Ω impedance matching to the input source impedance (also 50Ω) to minimize reflections. The 50Ω resistors are
connected between the input of the emitter followers and the power supply and can be used to achieve a broadband match in the low-GHz range of input signals. The second role of the emitter followers is to provide level-shifting of the 4V DC supply to bias the mixing quad. The excellent high frequency response of the emitter followers (simulated 3-dB bandwidth of 18GHz) also ensures sufficient bandwidth for the intended data rates of 1-2Gb/s.

The size of the emitter followers is set to about one-half that of the mixing quad transistor to achieve a good compromise between speed and power consumption, since a large size improves the speed and a small size reduces power. Hence, each emitter follower has a tail current of 10mA to drive the 25mA per side in the transmitter. This tail current is needed to ensure that the output (emitters) of the emitter followers and the input (bases) of the common-base mixing quad are low-impedance nodes\(^3\) — an important condition for oscillation. The emitter followers are biased at \(1/2J_{\text{peak}f_T}\) rather than at \(J_{\text{peak}f_T}\) to maintain adequate speed performance while avoiding potential instability due to negative resistance at high bias current density [4].

The tail currents of the emitter followers are set through current mirrors with a ratio of 1:5. Diode-connected transistors reduce the \(V_{CE}\) of the resistively degenerated bipolar current sources to avoid transistor breakdown. A 1pF on-chip decoupling capacitor is used to prevent the injection of supply noise into the circuit and to ensure stability of the bias circuit at high frequency.

4.1.3. Circuit Layout

Figure 4.3 shows the layout of the BPSK transmitter. It occupies a total area of \(660 \times 580 \mu m^2\) and consists of 3 power pads, 2 signal pads for the data input and 2 signal pads for the output. The Vdd pad supplies the main 4V DC power, while Vee is used to control the bias current in the oscillator such that the tank voltage swing does not exceed the transistor breakdown. Vb (4V) sets the current in the current mirrors through a 1.35kΩ poly resistor. All high frequency paths are routed using the top metal layers

---

\(^3\)Since the output impedance of a common-collector amplifier, or emitter follower, is \(1/g_m\), which is inversely proportional to the bias current \(I_C\).
4.1 65GHz BPSK Transmitter in 0.18µm SiGe BiCMOS

(5, 6) to minimize capacitance to the substrate while taking advantage of their higher current-carrying capability and lower resistance due to thicker metal. Large Vdd and ground planes in metals 1 and 2, respectively, provide good power supply decoupling and a low resistance ground. Implementing the ground plane in metal 2 between Vdd and the high frequency paths has the added benefit of shielding the signal paths from the power lines, preventing power supply noise from corrupting the high speed signals. To reduce parasitic inductance and minimize reflections at the output, 50Ω transmission lines implemented as 12µm wide microstrip lines over metal 2 ground are used to route the outputs to the pads.

Figure 4.3: Layout of 65GHz BPSK transmitter (660µm × 580µm).

Figure 4.4 shows a more detailed view of the mixing quad and the emitter follower layout. Symmetry in the differential circuit, and especially in the mixing quad, is ensured by directly mirroring one of the half circuits with respect to the centre axis. The compo-
4.1 65GHz BPSK Transmitter in 0.18\(\mu\)m SiGe BiCMOS

Components in the high frequency path are placed as closely together as possible to minimize parasitics, while the bias circuitry can be placed further away. All transistors have the same orientation for optimal matching. The emitter followers are placed close to the mixing quad to reduce parasitic inductance in the emitter which can potentially lead to instability. A 1pF MIM capacitor near the current mirrors provides localized power supply decoupling.

![Image of 65GHz BPSK transmitter layout]

Figure 4.4: Close-up view of 65GHz BPSK transmitter layout.

4.1.4. Simulation Results

The time and frequency domain simulation results for the transmitter are presented below. The transmitter was originally based on an 80GHz oscillator, which, after accounting for parasitics (predominantly in the form of capacitance in the metallization of the negative resistance transistors), decreased in frequency to 68GHz. With the mixing quad switched, the output carrier has a single-ended swing of 900mVppk or 3.1dBm in a 50\(\Omega\) load.
To simulate the functionality of the BPSK transmitter, it was modulated digitally using a PRBS generator block from the AHDL library. A $2^7 - 1$ pattern length was used for a reasonable simulation time. A 2Gb/s (or 1GHz) PRBS stream with finite rise and fall times and 500mVpp amplitude was first applied, resulting in the modulated waveform of Figure 4.5 and the corresponding spectrum in Figure 4.6. Figure 4.7 shows a zoomed-in view of the phase shift corresponding to the input data transition. Figures 4.8 and 4.9 show a similar simulation, but with a 3Gb/s data input.

Figure 4.5: Simulated transient response of BPSK transmitter with 2Gb/s, 500mVppk PRBS input.

Figure 4.6: Simulated spectrum of BPSK transmitter with 2Gb/s, 500mVppk PRBS input.

Figure 4.7: Close-up view of phase shift in BPSK transmitter transient response to a 2Gb/s, 500mVppk PRBS input.
4.1 65GHz BPSK Transmitter in 0.18µm SiGe BiCMOS

Figure 4.8: Simulated transient response of BPSK transmitter with 3Gb/s, 500mVppk PRBS input.

Figure 4.9: Simulated spectrum of BPSK transmitter with 3Gb/s, 500mVppk PRBS input.

Table 4.1 summarizes the simulated characteristics of the transmitter. The 1.5Vppk output swing was taken single-endedly over a 50Ω load and corresponds to a PRBS input of 500mVppk at 2Gb/s. The impact of the additional circuitry on the oscillator phase noise was also examined through simulating the transmitter with the mixing quad switched to enable convergence during the periodic steady state analysis. Since the main factors affecting phase noise, namely tank swing, tank Q and bias current, remained constant, there was minimal change in the phase noise. The transmitter consumes a total DC power of 332mW.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier Frequency (GHz)</td>
<td>68</td>
</tr>
<tr>
<td>Typical Input Data Rate (Gb/s)</td>
<td>0.5-3</td>
</tr>
<tr>
<td>Typical Input Amplitude (Vppk)</td>
<td>0.5 (per side)</td>
</tr>
<tr>
<td>Output Voltage Swing (Vppk)</td>
<td>1.5 (per side)</td>
</tr>
<tr>
<td>Oscillator Phase Noise (dBc/Hz @ 1MHz)</td>
<td>-95.4</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>4</td>
</tr>
<tr>
<td>Oscillator Current (mA)</td>
<td>50</td>
</tr>
<tr>
<td>Total Current (mA)</td>
<td>83</td>
</tr>
<tr>
<td>Total Power (mW)</td>
<td>332</td>
</tr>
</tbody>
</table>
4.1.5. Summary

A novel 65GHz BPSK transmitter in silicon has been presented. Its compact layout and simple topology make it well-suited for low-cost, low-power mm-wave sensor applications where linearity and output power requirements are less stringent than for radio applications. Compared with existing mm-wave BPSK modulators using expensive III-V devices and microstrip couplers for satellite and wireless data communication applications (ie. [54, 55]), this implementation is superior in terms of both cost and area consumption. The less crowded 60GHz band, with significantly more free bandwidth compared with the 5GHz band, is also more tolerant of systems with double-sideband spectra.

4.2. 60GHz Single-Sideband Transmitter in 0.18µm SiGe BiCMOS

This section presents the design and analysis of a 60GHz radio transmitter with on-chip image rejection. In contrast to the BPSK transmitter presented in the previous section, this transmitter adopts the more sophisticated heterodyne method of upconversion for radio applications, with a 5GHz IF and a 65GHz LO carrier. The transmitter topology is based on the single-sideband modulator introduced in Section 2.3, and represents the first fully integrated radio transmitter with on-chip VCO in silicon at 60GHz.

4.2.1. System Overview

The choice of the classical single-sideband modulator for the transmitter topology arises from its inherent image rejection capability and its relative simplicity (when compared to 5GHz radio). A simpler topology is preferred to ensure robustness at mm-waves in light of the greater impact of parasitics on circuit performance and the lower available gain of the transistors. The block diagram of the single-sideband transmitter, along with an illustration of its frequency domain operation, is shown in Figure 4.10.

The quadrature generation at IF and image rejection at RF are performed by 5GHz and 65GHz polyphase filters, both of which are implemented as stagger-tuned 2-stages for broader bandwidth and lower sensitivity to component mismatch. Two double-balanced
Gilbert cell mixers, having the advantages of good port-to-port isolation and potentially high conversion gain, are combined in an image-reject mixer topology to perform the frequency upconversion. A differential cascode Colpitts VCO with accumulation mode varactors provides the LO signal in the 62-68GHz range, and drives the two Gilbert cells through emitter follower buffers. The 3-stage Class A PA discussed in Section 3.3 provides linear amplification and drives the RF signal to a 50Ω antenna load. The LSB from the upconverter is used to generate the desired RF signal range that covers the 60GHz radio band. A fully differential architecture is employed for the transmitter to improve immunity to on-chip crosstalk and power supply rejection.
Figure 4.10: SSB transmitter block diagram and frequency domain operation.
4.2 60GHz Single-Sideband Transmitter in 0.18μm SiGe BiCMOS

The design process for the individual blocks proceeds from the output to the input. The input compression point for each stage determines the output compression of the previous block. The main design optimization parameters for the transmitter are output power, linearity and system gain. Since the all-passive polyphase filters each introduce 9-10dB loss into the system, achieving adequate gain in the upconvert mixers and the PA is critical. This has resulted in the requirement for 3 gain stages in the PA, and the use of HBT differential pairs as transconductors in the Gilbert cell mixers in order to increase conversion gain (discussed in more detail in Section 4.2.2).

Figure 4.11 shows the gain distribution and linearity performance among the blocks in the system (specified at 60GHz), as well as the system operating conditions. The final $OP_{1dB}$ compression point for the transmitter is computed using the equation for linearity in a cascaded system, as described in Section 2.5:

$$\frac{1}{OP_{1_{\text{Tx}}}} = \frac{1}{OP_{1_{\text{PA}}}} + \frac{1}{Ga_{\text{PA}} \times OP_{1_{\text{Mixer}}}}$$ (4.6)

Based on the output compression points of the mixer and the PA, and the gain of the PA, the final transmitter $OP_{1dB}$ is found to be 6.8dBm (differential). A total system gain of 4.8dB is achieved. The following sections discuss in more detail the design of each block.

4.2.2. Up-Convert Mixers

The two upconvert mixers used in the single-sideband modulator are implemented as double-balanced Gilbert cells with resistively degenerated common-emitter HBT transconductance stages. The double-balanced mixer differs from the single-balanced and the unbalanced versions by accommodating LO and IF input signals which are both differential. Despite its relative complexity, the double-balanced mixer topology exhibits better port-to-port isolation and higher rejection of LO noise and feedthrough. As a result, the Gilbert cell has remained popular at RF frequencies and is now also the mixer topology of choice at mm-waves.

The principal design considerations for the mixers are: upconversion gain, linearity ($OP_{1dB}$), LO drive requirement, RF output impedance matching, and port-to-port iso-
4.2 60GHz Single-Sideband Transmitter in 0.18µm SiGe BiCMOS

Figure 4.11: SSB transmitter block diagram with simulated performance summary.

The design goals for a mixer in the transmitter differ from the requirements for a downconvert mixer in a receiver, where noise and rejection of out-of-band interferers have a critical impact on the receiver sensitivity. In the transmitter, gain and linearity must be maximized to ensure an error-free output signal. The following section discusses the design methodology and tradeoffs for the upconvert mixers.

**Upconversion Gain and Linearity**

The schematic of one of the upconvert mixers is shown in Figure 4.12. Due to the high losses imposed by the 5GHz and the 65GHz polyphase filters, attaining adequate upconversion gain in the mixers is a main goal in the design process. This is made challenging at 65GHz by the lower transistor gain and the smaller parallel load resistance achievable in the tuned tank. In light of the 9dB loss from the 65GHz polyphase filter and the input 1dB compression of -10dBm for the 3-stage PA, the mixer $OP_{1dB}$ should
be $> -1$dBm.

![Upconvert Mixer Diagram](image)

Figure 4.12: Upconvert Mixer

To compare the benefits of using a CMOS or an HBT input transconductor pair, the available gain ($G_A$) of BiCMOS and HBT cascodes as a function of the collector/drain current are simulated and compared in Figure 4.13. The plots correspond to device sizes of $0.2 \mu m \times 3.58 \mu m \times 2$ (EBC-232) for the HBT and $0.18 \mu m \times 2 \mu m \times 12$ for the n-channel MOSFETS. Although implementing the input transconductor pair in CMOS offers the advantage of improved input linearity, as shown by the larger variations in $I_{DS}$ that can be tolerated in the BiCMOS cascode before the onset of the 1dB gain compression, the higher $G_A$ of the HBT-HBT cascode presents the possibility of adequate upconversion gain and sufficient linearity through the negative feedback formed by resistive degeneration. This design flexibility makes the HBT the favoured candidate for the input transconductor pair.

A hand analysis of the expected upconversion gain and linearity reveals the design tradeoffs and yields the amount of resistive degeneration needed as well as the required tail...
current. The voltage gain of the mixer, without matching considerations and assuming an ideal square LO signal, is given by:

\[ \frac{v_o}{v_i} = -\frac{2}{\pi} g_{me} R_p, \]  

(4.7)

where by resistive degeneration \((R_e)\),

\[ g_{me} = \frac{g_m}{1 + g_m R_e}; \]  

(4.8)

and \(R_P\) represents the parallel resistance of the load tank at resonance, which may be approximated to a first order by:

\[ R_P = \omega \times L_P \times Q; \]  

(4.9)

Additionally, the input linearity of the mixer is determined by:

\[ V_{in, pk, linear} = R_E \times I_C; \]  

(4.10)

While it is apparent that increasing the bias current simultaneously improves the conversion gain and the input linearity, the resulting higher power consumption also becomes an important consideration since two mixers are used in the transmitter. Hence, improvements in linearity are made from increasing the degenerating resistors, rather
than scaling the current. To attain a good compromise between gain and linearity, the
final design uses close to 10mA per side with 25Ω resistive degeneration, allowing a
maximum linear input voltage swing of approximately 250mVpk on each side.

The output linearity is a function of the voltage swings across the load and the quad
transistors, and is limited by the lower of the two:

\[ V_{o,max} = \min \{I_C R_P, V_{CE3} - V_{CE,SAT3}\} \]  \hspace{1cm} (4.11)

The optimal design then, entails that the voltage drop is equally distributed between the
load and the \( V_{CE} \) of the quad transistors:

\[ I_C R_P = V_{CE3} - V_{CE,SAT3} \]  \hspace{1cm} (4.12)

Since inductive loads are used for the upconvert mixer, the \( V_{CE} \) of the quad transistors
can be set to 1.4V given a 3.3V supply, a \( V_{DS} \) of 0.4V on the MOS current source and a
\( V_{CE} \) of 1.2V on the input transconductor pair. The size of the load inductor is chosen as
part of the matching network that transforms the output impedance at the RF port to
100Ω differential. The realization of large inductive loads for maximizing gain is hindered
by the corresponding decrease in the inductor SRF, which is an important consideration
for 65GHz operation. With the load inductor fixed, the branch current then becomes the
main determinant of linearity. The equivalent parallel resistance, \( R_P \), of the load inductor
can be found by performing an S-parameter analysis and examining the real part of the
output tank impedance prior to the matching network. The resistance \( R_P \) when the load
inductor (represented as a 2-π model) resonates with the parasitic capacitances \( C_{bc} \) and
\( C_{c-bulk} \) of the quad transistors is 40Ω at 65GHz. This results in a branch current \( I_C \) of
23mA needed to achieve condition 4.12. Clearly, this large current is impractical both in
terms of power consumption and the LO drive requirement. It can be found by a simple
hand calculation that using the 10mA branch current, which optimizes the input linearity
and voltage gain as discussed earlier, allows a 1.6Vppk differential output swing, thereby
meeting the required mixer output linearity of \( > -1dBm \) while still keeping the power
consumption within reasonable levels.
Transistor Biasing

For an upconvert mixer, the HBT transconductor pair is biased for optimal linearity at the peak $f_T$ current density for a $V_{CE}$ of 1.2V, which also corresponds to the peak available gain current density. The mixing quad is implemented using HBTs for the reduced LO drive requirement. A lower voltage is required to switch the HBT compared to the MOS differential pair ($4V_T$ vs. $\sqrt{2}V_{eff}$). The operation of the mixing quad is akin to that of a digital switch, and hence the transistors are sized as in a CML/ECL gate, at $0.75 \times$ the peak $f_T$ current density for steady state conditions with equal current distribution across the quad. This ensures that none of the quad transistors will reach bias levels of $2J_{peakfT}$ when the current completely switches to one side, which leads to significant speed degradation due to the drop in $f_T$.

LO Drive Requirement

To examine the impact of the LO power on the mixer performance, the power conversion gain as a function of the LO drive level is shown in Figure 4.16 for an LO of 65GHz, an IF of 5GHz and an RF of 60GHz. As expected, higher conversion gain is attained with larger LO levels, since the LO amplitude is proportional to the amount of switching current available, and a larger switching current results in more abrupt switching of the differential pairs. The abrupt switching essentially reduces the period during which the transistors in the differential pair (ie. Q3 and Q4 in Figure 4.12) are simultaneously on. Since the VCO is on-chip, the LO drive level is limited to the maximum achievable VCO output swing, as dictated by the supply voltage and the transistor breakdown. The mixer operates with a differential LO level of $1V_{ppk}$, corresponding to the output swing after the emitter follower buffers for the VCO. Hence, all simulations are performed using a 65GHz, $1V_{ppk}$ sinusoid to represent actual operating conditions.

Port-to-Port Isolation

While the IF-RF, LO-IF and LO-RF isolations should all ideally be >40dB, the LO-RF isolation is especially critical in the upconverter due to the close proximity of the LO and RF frequencies, which complicates the task of filtering out the LO feedthrough. The

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Terry Yao
double-balanced Gilbert cell topology has the advantage of higher inherent isolation between the RF, IF and LO ports compared with the single-balanced or unbalanced mixers. In the single-balanced case with single-ended IF input, the LO signal is essentially amplified by the differential (switching) pair. On the other hand, the differential pairs in the Gilbert cell switching quad add the amplified LO signals in opposite phases, thereby creating a first-order cancellation. Further suppression of LO feedthrough can be accomplished through careful layout techniques, where substrate leakage — the main source of feedthrough and which is not captured in simulations — is minimized by employing isolation improvement techniques during the layout design phase (section 4.2.7).

**Simulation Results**

Figures 4.14 - 4.17 show the simulated performance of the mixer. The conversion gain and input linearity performance of mixers with HBT and MOS input transconductor (biased at 0.3mA/µm) pairs are compared in Figure 4.14. These are simulated using a non-ideal LO of 1dBm differential at 65GHz and an IF of 5GHz. While the case with the MOS input pair has better linearity performance (as expected), the conversion gain is significantly lower than in the HBT case. The HBT-HBT cascode is a more suitable implementation for its higher gain (even with resistive degeneration) and sufficient linearity ($OP_{1dB} > -1$dBm). Figure 4.15 shows the two upconverted sidebands where the conversion gain of the HBT mixer is plotted as a function of the RF frequency. Finally, the effect of the LO drive level on conversion gain can be seen in Figure 4.16, while Figure 4.17 shows the RF port output match.

**4.2.3. 5GHz and 65GHz Polyphase Filters**

The sideband suppression performance of the SSB transmitter is directly influenced by the phase and magnitude accuracy of the quadrature hybrids. While the monolithic integration of traditional microwave hybrid-couplers such as the branchline coupler [56] and the Lange coupler [56] becomes feasible at mm-wave frequencies, the limited bandwidth of the branchline coupler and the single-ended nature of the Lange coupler inhibit their ease of implementation in high-bandwidth radio systems with differential building
4.2 60GHz Single-Sideband Transmitter in 0.18µm SiGe BiCMOS

Figure 4.14: MOS and HBT mixer conversion gain and input 1dB compression.

Figure 4.15: HBT mixer power conversion gain vs. frequency.

Figure 4.16: HBT power conversion gain vs. LO power.

Figure 4.17: Differential matching at output RF port.
blocks. An alternative method of quadrature generation and combination is the RC-based sequence asymmetric polyphase filter—a popular block in low-GHz image reject receivers [57, 58]. The suitability of the polyphase filter arises from its differential mode of operation, its potential wide-band response, and its R-C structure, which allows for area-efficient on-chip integration.

Mathematically, a 90° phase shifter is represented by the Hilbert Transform, with the following transfer function:

\[
H(j\omega) = \begin{cases} 
-j & \text{for } \omega > 0 \\
0 & \text{for } \omega = 0 \\
 j & \text{for } \omega < 0
\end{cases}
\] (4.13)

Practical implementations of the Hilbert transform approximate the transfer function in a specific frequency band. The simplest type of Hilbert filter is the RC-CR network—a classical structure for quadrature generation, and also the basis for the polyphase filter.

Shown in Figure 4.18, the RC-CR network consists of a pair of RC lowpass and CR highpass filters, with equal values for R and C. At the corner frequency of the RC-pole and the CR-zero, \(1/2\pi(RC)\), the input signal is attenuated by 3dB, and experiences a 45° phase lag from the LPF and a 45° phase lead from the HPF. Hence, the two output signals have equal magnitudes and are always 90° out of phase at the corner frequency. A drawback of this circuit is the narrow bandwidth over which amplitude matching can be achieved. Furthermore, it is highly sensitive to manufacturing variations which may cause a discrepancy between the corner frequency and the operating frequency. These problems can be alleviated with the use of the polyphase filter (Figure 4.19), which is essentially a symmetrical and repetitive version of the RC-CR network. By sharing the RC of one input as the CR of another input, the RC-CR network is effectively repeated four times. The advantage of this repetitive structure is that it allows for the cascading of several stagger-tuned stages, leading to small amplitude error over a wider band, and a more precise 90° phase shift with each additional stage. The sensitivity to component mismatch—an important drawback of the polyphase filter—can thereby be reduced. A two-stage implementation offers an adequate compromise between bandwidth and power
loss, since each stage in a cascaded polyphase filter contributes at least 3dB of loss.

The section below discusses the design of the two polyphase filters used in the single-sideband modulator, followed by S-parameter simulation results.

**Design and Analysis**

Shown in Figure 4.20 is a single-stage polyphase filter equally loaded at the 4 output ports, driven by a differential signal $V_{p1}$ while the other two input ports are grounded. Although this configuration corresponds to that of the 5GHz polyphase filter used for quadrature generation at IF, the following analysis can be directly applied to the 65GHz filter used for quadrature combination due to the symmetric nature of the polyphase filter. Instead of generating 2 pairs of differential signals in quadrature from a differential input, the 65GHz filter combines 2 quadrature pairs and outputs a differential signal to the power amplifier. The selection of the USB or LSB is dependent on the connection sequence made at the input of the 65GHz filter.

Decomposing the differential signals into positive and negative components allows for a more simplified analysis of the filter half circuit. Knowing that $V_{p1} = 2V_{p1^+}$, $V_{p2} = 2V_{p2^+}$ and $V_{p3} = 2V_{p3^+}$, the half circuit of Figure 4.20 yields the following transfer functions:

\[
\frac{V_{p2}}{V_{p1}} = \frac{Z_L}{R + Z_L + j\omega CRZ_L} \tag{4.14}
\]

\[
\frac{V_{p3}}{V_{p1}} = \frac{j\omega CRZ_L}{R + Z_L + j\omega CRZ_L} \tag{4.15}
\]

To determine the appropriate component values for the filter, the performance criteria for the polyphase filter must first be established. The most important aspects of the polyphase filter performance are phase and amplitude match between the quadrature pairs. First, the phase difference between signals at port 2 and port 3 should be 90°. As seen from the following, this condition is true for all frequencies:

\[
\text{Phase}(V_{p3}) - \text{Phase}(V_{p2}) = \text{Phase}\left(\frac{V_{p3}}{V_{p2}}\right) = \text{Phase}(j\omega CR) = 90^\circ, \forall \omega \neq 0 \tag{4.16}
\]

Secondly, the signals at ports 2 and 3 should have the same amplitude at the frequency of interest, $\omega_o$. The relationship between R and C that satifies this criteria is found as
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Figure 4.18: RC-CR network.

Figure 4.19: 1-Stage polyphase network.

Figure 4.20: Single stage polyphase filter and half circuit.

follows:

\[
\left| \frac{V_{p2}}{V_{p1}}(j\omega_o) \right| = 1 \quad (4.17)
\]

Hence,

\[
|j\omega_o CR| = 1 \rightarrow \omega_o CR = 1 \quad (4.18)
\]

The differential input impedance, \( Z_{in} \), can be determined by performing a nodal analysis of the half circuit. With \( \omega_o C = 1/R \), \( Z_{in} \) is found to be:

\[
Z_{in}(j\omega_o) = R(1 - j) \quad (4.19)
\]
Thus, the selection of the component values for R and C can be based on the equations 4.18 and 4.19. To achieve a differential input/output impedance of 100Ω, the real part of $Z_{in}(R)$ should be sized to be 100Ω, while the capacitance C is determined by the desired center operating frequency $\omega_o$ of the stage. Inductors are used for matching purposes by cancelling out the imaginary part of the input/output impedance:

$$\Im\{Z_{in}(j\omega_o)\} = 0 \rightarrow L = \frac{-\Im\{Z_{in}(j\omega_o)\}}{\omega_o} = \frac{R}{\omega_o} \quad (4.20)$$

For reasons due to symmetry, two inductors of value $R/2\omega_o$ are used to achieve matching at each input/output port.

To broaden the bandwidth over which there is minimal amplitude variation between the I and Q paths, both filters adopt the 2-stage cascade topology, with the center frequencies of the stages being 4GHz and 6GHz for the IF polyphase filter, and 60GHz and 70GHz for the RF. The minimum loss of 3dB in each stage of the filter imposes an upper limit on the number of stages that can be cascaded. The filters should ideally attain gain and phase mismatches of less than 2% and 1.2°, respectively, in order to achieve 40dB of image rejection [59].

The schematics of the polyphase filters are shown in Figures 4.21 and 4.22, and the corresponding component values are summarized in table 4.2. The capacitors are implemented as square MIM capacitors for minimum parasitic inductance, while the resistors are realized as poly resistors for lower sensitivity to process variation as compared with metal resistors. The inductors for the 5GHz filter are sized to be 1.38nH instead of the theoretical 1.6nH to minimize area while still achieving adequate matching. They are designed as square multi-metal stacked inductors in M5 and M6 to maximize inductance while keeping the area consumption to a minimum. In the 65GHz polyphase filter, the smaller inductor sizes allow for a planar octagonal implementation. Since the interconnect inductance has a much larger impact at 65GHz than at 5GHz, the inductors are designed to be 88pH, with the remaining inductance being contributed by the interconnects. 15µm wide transmission lines on M6 with 50Ω characteristic impedance at 65GHz are used to connect the inputs of the 65GHz filter to the pads.
S-Parameter Simulation Results

More insight can be gained on the operation of the polyphase filters through S-parameter simulations. Since the polyphase filters operate differentially in the transmitter, and only single-ended S-parameter measurements can be made in the lab, the filters are simulated single-endedly and linear superposition is used to derive the equivalent phase and magnitude responses for differential inputs and outputs. Figure 4.23 shows the simulation results for the 5GHz filter, where the power and phase variations between the two differential quadrature outputs (ports 2 and 3) due to sinusoidal excitations at the positive and negative port 1 terminals are compared. Similarly, in Figure 4.24, the power and phase variation at the output port 3 due to inputs at ports 1 and 2 are shown. Additionally for the 65GHz case, the outputs at ports 3⁺ and 3⁻ should have a phase difference of 180° for each set of differential inputs applied at ports 1 and 2.
 impedance matching results for both filters represent single-ended simulations.

### Polyphase 5G SP Simulation Results

**Polyphase 5G SP Simulation Results**  (Single-Ended I/O)

![Polyphase 5G SP Simulation Results](image)

**Figure 4.23:** 5GHz polyphase filter S-parameter simulation results.

### 4.2.4. 3-Stage Power Amplifier

The reader is referred to Section 3.3 in the thesis for the design details on the 3-stage power amplifier used in this system.
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Polyphase 65G SP Simulation Results (Single-Ended I/O)

Figure 4.24: 65GHz polyphase filter S-parameter simulation results.

4.2.5. Low Phase Noise Colpitts VCO

The local oscillator (LO) signal is provided on-chip by a differential Colpitts VCO operating in the 62-68GHz range. It is a scaled and tunable version\textsuperscript{4} of the oscillator [53] used for the BPSK transmitter, with a reduced value of $C_2$ to enable a higher oscillation frequency. Accumulation mode varactors with $10 \times 2\mu m \times 0.18\mu m$ fingers are used, as opposed to fixed MIM capacitors, to allow for frequency tuning. Due to a lack of varactor models, MIM capacitors with values of 17-35fF are used to simulate the tuning range at the schematic level. The relatively large tail current of the VCO is needed to achieve minimum phase noise [53] and to provide an adequate level of LO power to drive the two upconvert mixers. The simulated performance of the VCO without EF buffers is summarized in table 4.3.

\textsuperscript{4}The modification of the VCO was done by Michael Gordon.

\textsuperscript{4}The modification of the VCO was done by Michael Gordon.
the two upconvert mixers. The emitter followers are biased at $1/2 J_{\text{peak}_{fr}}$ current density as in the case of the BPSK transmitter. Figure 4.25 is a schematic of the VCO with emitter follower buffers. The emitter followers also provide level shifting to generate an adequate DC level for the LO port of the mixers, thus eliminating the need for additional bias circuitry.

![Figure 4.25: 61-67GHz Colpitts VCO with emitter follower buffers.](image-url)

### 4.2.6. System Integration

With each block being impedance-matched at the input and output, the overall system integration simply entails the cascading of the blocks to form the full SSB transmitter. The 65GHz polyphase filter and the 3-stage PA are AC-coupled through two $15\mu m \times 15\mu m$ 230fF capacitors, which serve to de-couple the DC level of the mixer output from the input of the PA. The connection of the mixers to the 5GHz and 65GHz polyphase...
Table 4.3: Simulated VCO performance summary (without EF buffers).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tuning Range (GHz)</td>
<td>62-68</td>
</tr>
<tr>
<td>Phase Noise 1MHz 68GHz (dBc/Hz)</td>
<td>-97.5 (68GHz)</td>
</tr>
<tr>
<td>Phase Noise 1MHz 62GHz (dBc/Hz)</td>
<td>-98.4 (62GHz)</td>
</tr>
<tr>
<td>Single-Ended Voltage Swing (Vppk)</td>
<td>1.4</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>4</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>250</td>
</tr>
</tbody>
</table>

filters determines the suppression of the LSB or USB, since the polyphase filter generates quadrature signals and performs image rejection based on the positive and negative input sequences. Figure 4.26 illustrates the polyphase filter connections in the image reject mixer for LSB generation.

Figure 4.26: Polyphase filter configuration for LSB generation.

The IRR due solely to the image reject mixer topology, prior to amplification by the 3-stage PA, is found in simulation to be 37dB, as shown in Figure 4.27.

### 4.2.7. System Layout

Figure 4.28 shows the layout of the entire transmitter containing a total of 34 spiral inductors. It is based on a top-down hierarchical layout methodology whereby each block is individually optimized starting at the transistor-cell metallization level. Substrate contacts are placed extensively around the transistor, capacitor and resistor cells to reduce substrate resistance and crosstalk, and to ensure model validity. MIM decoupling capacitors ranging from 1pF to 5pF are placed close to all bias points and supply pads...
for high frequency noise filtering. Octagonal inductors are used extensively to reduce on-chip antenna effects due to radiation from 90° corners. On-chip isolation is critical, particularly between the VCO and the rest of the system, to minimize LO phase noise and feedthrough. Hence, the VCO is surrounded by a 32\(\mu\)m wide isolation ring which creates reverse-biased PN junctions with the appropriate Vdd and ground connections. The same type of isolation is also used for inductors. The DC pads are allocated with the consideration of the maximum current-handling capability of the pad (100mA/pad), based on the pad width and the metal current density at 110°C.

Figure 4.29 is a close-up view of one of the mixer cells. Matching between the two mixers and path symmetry between the mixers to the 65GHz polyphase filters are critical to minimizing amplitude and phase imbalance and ensuring adequate image rejection. Emitter follower buffers are placed close to the mixer rather than the VCO to avoid instability due to parasitic inductance at the buffer output.

Figure 4.30 shows the polyphase filter breakout structures, where 40\(\mu\)m \(\times\) 40\(\mu\)m signal pads are used for lower pad capacitance. For the 65GHz filter, 50\(\Omega\) (15\(\mu\)m wide) transmission lines connect the 4 inputs to the pads. The 65GHz filter core is also shown in Figure 4.31. The distance between the passives is minimized for lower component mismatch due to process variations and for reduced parasitics. The interconnect lengths are equalized to balance the parasitic resistance and inductance in each branch.
4.2 60GHz Single-Sideband Transmitter in 0.18μm SiGe BiCMOS

Figure 4.28: Layout of full SSB transmitter.
4.2 60GHz Single-Sideband Transmitter in 0.18µm SiGe BiCMOS

Figure 4.29: Layout of one Gilbert cell mixer.

4.2.8. System Simulations

Figure 4.32 shows the transmitter input and output impedance match, in which the effects of the pad capacitances are captured by 17fF capacitors placed at the input and output ports to ground. This value is based on measurements of previously fabricated pad structures. Figure 4.33 shows the transient responses of the 5GHz IF and 63GHz RF signals.

The simulated frequency spectra are shown in Figures 4.34 and 4.35. The spectra are obtained using the built-in DFT function in Spectre. The selection of the time interval over which to perform the DFT is crucial to the resolution of the frequency spectrum. For the DFT to be performed properly, the $f \times \Delta t$ product should be an integer, where $f$ represents the signal frequency, and $\Delta t$ is the specified DFT time interval. Since the simulations were performed using a real VCO with a non-integer oscillation frequency, the exact signal frequency must first be obtained so that the time interval for the DFT can be set correctly.
4.2 60GHz Single-Sideband Transmitter in 0.18µm SiGe BiCMOS

Figure 4.30: Layouts of 5GHz and 65GHz polyphase filter breakouts.

Figure 4.31: Layout of 65GHz polyphase filter core.
4.2 60GHz Single-Sideband Transmitter in 0.18\textmu m SiGe BiCMOS

Figure 4.32: Simulated input and output return loss of SSB transmitter.

Figure 4.33: Simulated differential transient response of 5GHz IF and 63GHz RF signals for 3dBm differential input and 68GHz LO.

Figure 4.34: Simulated differential output spectrum of SSB transmitter at nominal conditions with 5GHz, 3dBm differential IF and 68GHz LO.

Figure 4.35: Simulated differential output spectrum of SSB transmitter with 5GHz, 3dBm differential IF and 68GHz LO, with superimposed IF and LO signals.
Figure 4.34 shows the differential transmitter output spectrum with nominal component settings and bias points, and includes the effects of the 17fF pad capacitances, non-ideal inductors represented by the 2-π model, and layout parasitics extracted at the cell level. Figure 4.35 shows the same simulation, but with the LO and IF signals superimposed to reflect all signals present.

The simulated transmitter performance is summarized in Table 4.4.

Table 4.4: 65GHz SSB transmitter simulation summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier Frequency (GHz)</td>
<td>62-68</td>
</tr>
<tr>
<td>IF Frequency (GHz)</td>
<td>4-6</td>
</tr>
<tr>
<td>RF Frequency (GHz)</td>
<td>56-64</td>
</tr>
<tr>
<td>IRR (dB)</td>
<td>&gt;40</td>
</tr>
<tr>
<td>$IP_{1dB}$ (dBm)</td>
<td>3 (D)</td>
</tr>
<tr>
<td>$OP_{1dB}$ (dBm)</td>
<td>6.8 (D)</td>
</tr>
<tr>
<td>Upconversion Gain (dB)</td>
<td>4.8 (D)</td>
</tr>
<tr>
<td>$S_{11} @ 5GHz$ (dB)</td>
<td>&lt;-30 (D)</td>
</tr>
<tr>
<td>$S_{22} @ 65GHz$ (dB)</td>
<td>&lt;-25 (S)</td>
</tr>
<tr>
<td>VCO Phase Noise (dBc/Hz @ 1MHz)</td>
<td>-97.5 (68GHz)</td>
</tr>
<tr>
<td>Power - Mixers (mW)</td>
<td>151</td>
</tr>
<tr>
<td>Power - PA (mW)</td>
<td>193</td>
</tr>
<tr>
<td>Power - VCO + EF Buffer (mW)</td>
<td>432</td>
</tr>
<tr>
<td>Total Power (mW)</td>
<td>776</td>
</tr>
</tbody>
</table>

4.2.9. Summary

A 60GHz SSB transmitter with 5GHz IF has been presented in this section. Based on a classical image reject topology, the fully differential transmitter makes use of polyphase filters, rather than traditional microstrip hybrid couplers, for area efficiency and more broadband operation. The design considerations for each block has been discussed, and the level of image rejection achievable has been demonstrated through system-level simulations.
Experimental Results

This chapter presents the on-wafer measurement results for the 90nm CMOS power amplifier and the BPSK and SSB transmitters. In addition to the full SSB transmitter, various circuit breakouts were also fabricated and tested in an effort to better understand the system-level performance of the SSB transmitter and to investigate the accuracy of the active and passive device models used in simulation. The breakouts include the 3-stage SiGe HBT PA and the 5GHz and 65GHz polyphase filters. Measurement results for these blocks are also presented in this chapter.

5.1. 60GHz PA in 90nm CMOS

Figure 5.1 shows the die micrograph of the 3-stage CMOS power amplifier. The performance of the PA was characterized through a DC test to verify correct biasing conditions, an S-parameter test for the input and output matching, gain and isolation, and finally, a large signal measurement to find the output compression point. The setup for the DC and S-parameter tests are shown in Figure 5.2. The LRM (Line-Reflect-Match) algorithm available in the WinCal software from Cascade Microtech and the CS5 calibration substrate from GGB were used for network analyzer calibrations, which essentially define the S-parameter reference plane at the probe tips. IC-CAP, a measurement control and simulation software from Agilent, was used to control the VNA through the GPIB interface and to perform calculations and generate plots from the measured data.

As shown in Figure 5.3, the DC operation of the PA in measurement closely follows that in simulation. A total current of 44mA was measured at the nominal operating condition of 1V $V_{DD}$ and 0.8V $V_G$ for each stage, compared with the expected 43.5mA.
The current distribution among the 3 stages was verified by turning off stage 1 ($V_{G1}=0V$) and stages 2, 3 ($V_{G2,3}=0V$) and observing the total DC current draw. Figure 5.4 shows the case when stage 1 is turned off, with stages 2 and 3 consuming 21mA from a 1.5V supply, compared with the 22.5mA in simulation. The $I_{DD}$ vs. $V_G$ plot also clearly illustrates the linearity of the $I-V$ characteristic in sub-100nm MOSFETS, confirming the reduced region over which the square law is still applicable. With stages 2 and 3 turned off, the transconductance of the $32 \times 1\mu m$ transistor in stage 1 is plotted as a function of the gate voltage ($V_{G1}$) in Figure 5.5. It can be seen that in both the simulated and measured cases, the transconductance is close to the expected value of $\approx 1ms/\mu m$, and is relatively constant for most of the active bias range, thereby illustrating one of
the important results of the linear $I-V$ characteristic in nano-scale MOSFETs.

Figure 5.6 shows the measured vs. simulated S-parameters of the PA up to 65GHz. In addition to the pad capacitances, the simulated S-parameters also capture the effects of extracted parasitic capacitances in the transistor metallizations. The parasitic capacitances range from 10.9fF $C_{DS}$ to 18.6fF $C_{SB}$. A broadband match is achieved at the output, with $S_{22} < -10$dB over the 51-65GHz range. At the input, $S_{11}$ is $<-10$dB in the 60-65GHz range. The good matching at the center operating frequency of 60GHz is an indication of the accuracy of ASITIC in the modeling of the spiral inductors and the interconnects over silicon, all of which were taken into account in the design of the matching networks. As well, the good correlation confirms the validity of the RF MOSFET transistor models extracted at UofT based on MOSFET test structures from an earlier fabrication [2]. The amplifier has a peak gain of 5.2dB at 61GHz and a 3dB bandwidth of 52-65GHz. The 3 stages provide better than 30dB of isolation, as characterized by $S_{12}$ in Figure 5.7. The reduced gain compared with simulation can be attributed to the lower Q of the spiral inductors, which would also help broaden the bandwidth. It may also be due to the low ratio of the drain to source inductances, whose effects may not be fully captured in simulation. Characterization of the PA beyond 65GHz is limited by the operating range of the VNA. The large signal $P_{1dB}$ linearity test for the CMOS PA was performed using the setup shown in Figure 5.8. The Agilent 250kHz - 67GHz RF signal source provided the input to the PA, while the output power was measured on the Agilent E4419B power meter. Since the accurate de-embedding of loss in every connector and cable is crucial to obtaining the correct $P_{1dB}$ compression point, the setup diagram also shows the loss distribution based on measurement and equipment (probes, cables, adaptors) specifications.

The $OP_{1dB}$ was measured across 4 different dice, and range from 6.3-7dBm at 60GHz. In all cases, the supply voltage was set to 1.5V, $V_{G1}$ was set to 0.55V to maximize gain, and $V_{G2,3}$ was set to 0.65-0.75V for optimal linearity. Figure 5.9 shows the measured P1dB for one of the dice, with an $OP_{1dB}$ of 6.4dBm, and a saturated output power of 9.3dBm at 60GHz. Each stage consumes 5.2/10.1/11.2mA. The simulated $OP_{1dB}$ post-layout is 9.4dBm with 1.5V supply and the stages consuming 6.4/12.5/13.9mA.
gain also matches well with the small signal S-parameter test. The last 2 stages drew a total of 21mA, which, based on the transistor size ratios, corresponds to 10mA for the second stage and 11mA for the third stage. Thus, in accordance to theory, optimal linearity is achieved when the transistor in the final stage (40µm × 0.1µm) is biased at close to the peak $f_T$ current density of 0.3mA/µm. This dependence of $OP_{1dB}$ and gain on the bias of the final stage is shown in Figure 5.10. The PA efficiency as a function of input power is shown in Figure 5.11. The concave shape of the PAE curve reflects the changing relationship between input and output power as the PA goes into saturation. Maximum efficiency (21.4%) is achieved with the maximum saturated output power,
Figure 5.6: Measured vs. simulated $S_{11}$, $S_{22}$, $S_{21}$ for 90 nm CMOS PA.

while maximum PAE (7.4%) occurs just slightly beyond the 1dB compression point. The lower PAE is a result of the low gain of the PA. Finally, Figure 5.12 shows the supply dependence of $OP_{1dB}$, where, as expected, a higher voltage supply results in better $OP_{1dB}$ due to the larger drain voltage swing that can be supported.

Table 5.1 provides a comparison of this 90 nm CMOS PA with previously published mm-wave PAs in silicon in terms of the PA FoM, as defined in section 2.4.1, but using the $P_{sat}$ rather than $OP_{1dB}$ to accomodate the reported data in literature. It can be seen that this implementation represents the highest frequency PA in CMOS reported to date, while also having the lowest area consumption due to the use of area-efficient spiral inductors for on-chip matching. It is also comparable to [50] (40GHz) and [23] in gain and $P_{sat}$.

<table>
<thead>
<tr>
<th>Freq.</th>
<th>Technology</th>
<th>$P_{sat}$</th>
<th>PAE</th>
<th>Gain</th>
<th>Area</th>
<th>FoM</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>60G</td>
<td>0.12μm SiGe</td>
<td>16dBm(D)</td>
<td>4.3%</td>
<td>10.8dB</td>
<td>2.1×0.8mm²</td>
<td>74.3</td>
<td>20</td>
</tr>
<tr>
<td>77G</td>
<td>0.12μm SiGe</td>
<td>17.5dBm(S)</td>
<td>12.8%</td>
<td>17dB</td>
<td>1.35×0.45mm²</td>
<td>2125</td>
<td>49</td>
</tr>
<tr>
<td>77G</td>
<td>0.12μm SiGe</td>
<td>12.5dBm(D)</td>
<td>3.5%</td>
<td>6.1dB</td>
<td>2.1×0.75mm²</td>
<td>9.1</td>
<td>23</td>
</tr>
<tr>
<td>24G</td>
<td>0.18μm CMOS</td>
<td>14.5dBm(S)</td>
<td>14.5%</td>
<td>7dB</td>
<td>0.7×1.8mm²</td>
<td>11.7</td>
<td>51</td>
</tr>
<tr>
<td>27G</td>
<td>0.18μm CMOS</td>
<td>14dBm(S)</td>
<td>8.2%</td>
<td>17dB</td>
<td>1.2×1.7mm²</td>
<td>74.7</td>
<td>50</td>
</tr>
<tr>
<td>40G</td>
<td>0.18μm CMOS</td>
<td>10.4dBm(S)</td>
<td>2.9%</td>
<td>7dB</td>
<td>1.2×1.7mm²</td>
<td>2.6</td>
<td>50</td>
</tr>
<tr>
<td>60G</td>
<td>90 nm CMOS</td>
<td>9.3dBm(S)</td>
<td>7.4%</td>
<td>5.2dB</td>
<td>0.35×0.43mm²</td>
<td>7.5</td>
<td>This Work</td>
</tr>
</tbody>
</table>

*Table 5.1: 90 nm PA performance comparison with state-of-the-art.*
5.1 60GHz PA in 90nm CMOS

Figure 5.8: 90nm CMOS PA $P_{1dB}$ test setup.

Figure 5.9: Measured $OP_{1dB}$ for 90nm CMOS PA (60GHz, $V_{dd}/V_{g1}/V_{g2,3}=1.5/0.55/0.65V$).

Figure 5.10: Measured $OP_{1dB}$ and gain vs. final stage bias for 90nm CMOS PA.
5.1 60GHz PA in 90nm CMOS

Figure 5.11: Measured efficiency and PAE vs. input power for 90nm CMOS PA.

Figure 5.12: Measured $OP_{1dB}$ vs. supply voltage for 90nm CMOS PA.
5.2. 65GHz BPSK Transmitter in 0.18\textmu m SiGe BiCMOS

The die micrograph of the BPSK transmitter is shown in Figure 5.13.

![Die micrograph of the BPSK transmitter](image)

Figure 5.13: Die photo of 65GHz BPSK transmitter (660\textmu m \times 580\textmu m).

The setup of Figure 5.14 was used for the transmitter spectral measurements. The HP83752A Synthesized Sweeper generated sinusoidal inputs in the range of 0.5-2GHz, while the Agilent ParBERT 81250 provided $2^{31} - 1$ PRBS data up to 2.5Gb/s. Spectral measurements using the Agilent E4448A 3Hz-50GHz Power Spectrum Analyzer above 50GHz were facilitated by an external Agilent 11970V waveguide harmonic mixer which uses a 3.5-5.3GHz LO from the spectrum analyzer to downconvert a 50-75GHz RF signal to an IF of 321.4MHz, while operating from the 14th harmonic [60]. Decoupling capacitors and bias-T’s allow for AC-coupled inputs and outputs.

Figures 5.15 - 5.18 are the captured BPSK spectra for different modulation conditions. Figure 5.15 shows the 66GHz carrier signal with no modulating input, while Figures 5.16 and 5.17 show the upconverted sidebands for 1GHz (-8dBm) and 1.5GHz (-6dBm) sinusoidal modulation. The output power is lower than in simulation due to additional losses and parasitics in the layout. Finally, the upconverted spectrum for a 2Gb/s, 200mVppk PRBS input is shown in Figure 5.18. This was found to be the maximum...
amplitude at this data rate for which there was still a modulated output. This may be due to the fact that a sufficiently large input amplitude (where the input no longer qualifies as “small signal”) may result in a relatively large impedance at the output of the emitter followers, which in turn increases the impedance at the emitters of the switching quad, as seen by the oscillator. Since the negative resistance transistors in the oscillator must see a low impedance looking into mixing quad, any increase in the impedance at the emitters of the mixing quad could potentially stop the oscillation. Due to the low input power and losses in the circuit, the output amplitude was significantly lower than expected (by approximately 20dB). The transmitter was tested with a 5V DC supply while drawing 100mA.
5.2 65GHz BPSK Transmitter in $0.18\mu m$ SiGe BiCMOS

Figure 5.15: BPSK transmitter measured spectrum with no modulation.

Figure 5.16: BPSK transmitter measured spectrum with 1GHz, -8dBm modulation.

Figure 5.17: BPSK transmitter measured spectrum with 1.5GHz, -6dBm modulation.

Figure 5.18: BPSK transmitter measured spectrum with 2Gb/s, 200mV differential PRBS modulation.
5.3. 60GHz SSB Transmitter in 0.18µm SiGe BiCMOS

5.3.1. Polyphase Filters

The die photos of the 5GHz and 65GHz polyphase filters are shown in Figures 5.19 and 5.20, respectively. The objectives of the polyphase filter measurements were to first verify the correct operation of the filters in terms of the phase and magnitude responses, and secondly, to examine the accuracy of the input and output matching, thereby validating the sizing and modeling of the spiral inductors at 65GHz. Both objectives were achieved through S-parameter measurements using the Wiltron 360B VNA up to 65GHz (Figure 5.21). The calibration procedure is similar to that used for the CMOS PA S-parameter test, with the only difference being that a higher source power was used for the filter measurements (0dBm vs. -20dBm) to improve the quality of the calibration. This is feasible for a passive circuit since there is no danger of overloading the DUT beyond its input compression point, as may be in the case of an amplifier.

Figure 5.19: Die photo of 5GHz polyphase filter (710µm x 710µm).
5.3 60GHz SSB Transmitter in 0.18μm SiGe BiCMOS

Figure 5.20: Die photo of 65GHz polyphase filter (740μm × 600μm, 200μm × 200μm for filter core).
5.3 60GHz SSB Transmitter in 0.18μm SiGe BiCMOS

Figure 5.21: 5GHz and 65GHz polyphase filters S-parameter test setup.
Since only single-ended S-parameter measurements can be performed, a series of port-to-port measurements were taken and linear superposition was used to derive the differential operation. The phase response of the 65GHz filter can be computed as the difference in phase between ports $1^+$ and $2^+$ when a differential signal is applied at port 3. The following expression, based on the port labels in Figure 5.21, is used to determine the phase difference in both simulation and measurement (Figure 5.22):

$$\text{Phase} = \text{Phase}(S_{(3^-)(2^+)} - S_{(3^+)(2^+)}) - \text{Phase}(S_{(3^-)(1^+)} - S_{(3^+)(1^+)})$$  \hspace{1cm} (5.1)

The magnitude variation due to a differential input at port 3 can be determined by examining the losses at ports $1^+$ and $2^+$, where the factor of $\sqrt{2}$ appears during the single-ended to differential conversion and is due to the normalized (ie. $a_1 = V_{1^+}/\sqrt{50}$) S-parameters used in Cadence.

$$\text{MAG}(1^+) = 20 \times \log \left( \frac{S_{(3^-)(2^+)} - S_{(3^+)(2^+)}}{\sqrt{2}} \right)$$ \hspace{1cm} (5.2)

$$\text{MAG}(2^+) = 20 \times \log \left( \frac{S_{(3^-)(1^+)} - S_{(3^+)(1^+)}}{\sqrt{2}} \right)$$  \hspace{1cm} (5.3)

For the 5GHz filter in Figure 5.21, the outputs at ports $3^-$ and $2^-$ due to a differential input at port 1 should ideally be $90^\circ$ out of phase. The phase difference between ports $3^-$ and $2^-$ for a differential input are found using the following expression:

$$\text{Phase} = \text{Phase}(S_{(3^-)(1^+)} - S_{(3^-)(1^-)}) - \text{Phase}(S_{(2^-)(1^+)} - S_{(2^-)(1^-)})$$  \hspace{1cm} (5.4)

The magnitude variation between ports $2^-$ and $3^-$ due to a differential input at port 1 is found by:

$$\text{MAG}(3^-) = 20 \times \log \left( \frac{S_{(3^-)(1^+)} - S_{(3^-)(1^-)}}{\sqrt{2}} \right)$$ \hspace{1cm} (5.5)

$$\text{MAG}(2^-) = 20 \times \log \left( \frac{S_{(2^-)(1+)} - S_{(2^-)(1^-)}}{\sqrt{2}} \right)$$ \hspace{1cm} (5.6)

The phase and magnitude variation plots for the 5GHz and 65GHz polyphase filters are shown in Figures 5.22 - 5.25. There is good agreement between the measured and simulated phases for the 65GHz filter, while the measured phase for the 5GHz filter...
shows a larger variation from the desired 90°. The discrepancy in the 5GHz case may be caused by the larger, multi-layer stacked inductors used for matching, which is likely to introduce more asymmetrical path delays at the input and output ports. The magnitude responses reflect the power transfer at differential output ports due to a single-ended input. In both filters, the minimum magnitude variation occurs in the operating range for which the filter was designed, confirming the accuracy of the poly resistors and MIM capacitors.

The single-ended matching results at the four ports tested for each filter are shown in Figures 5.26 - 5.29. For the 5GHz filter, the return loss is > 10dB in the 4-6GHz range for all 4 ports tested. For the 65GHz filter, > 25dB return loss is achieved at the output ports. At the input ports, the use of 15µm wide transmission lines which connect the octagonal inductors to the pads results in broadband match (return loss > 10dB) across the 40-65GHz range.

5.3.2. 3-Stage PA in SiGe BiCMOS

The 3-stage SiGe HBT PA breakout structure is shown in Figure 5.30. A DC sweep of \(V_{DD}\) with all current mirror biases tied to the supply was first performed to verify the correct implementation of the on-chip biasing circuitry. The results, shown in Figure 5.31, indicate a good match between simulated and measured DC performance. A single-ended S-parameter measurement was done to verify the operation and input/output matching of the amplifier. The setup for the S-parameter test is similar to that used for the 90nm CMOS PA (Figure 5.2), with 67GHz differential circuit probes instead of the single-ended device probes, and 50Ω terminations for the unused input and output ports. The same Wiltron 360B VNA, calibration software and substrate used for the CMOS PA and polyphase filter testing were also used for the SiGe PA.

The measured S-parameters show a positive \(S_{11}\) from the 3-stage PA and a high \(S_{21}\), both of which indicate the presence of instability caused by positive feedback. Since the biasing for the 3 stages can be controlled independently, each stage was turned on and off by adjusting the \(V_{bias}\) of the reference current mirror while changes in the S-parameter response were observed. It was determined that the oscillation is due to excess ground
5.3 60GHz SSB Transmitter in 0.18µm SiGe BiCMOS

Figure 5.22: 65GHz polyphase filter measured vs. simulated phase variation.

Figure 5.23: 65GHz polyphase filter measured vs. simulated magnitude variation.

Figure 5.24: 5GHz polyphase filter measured vs. simulated phase variation.

Figure 5.25: 5GHz polyphase filter measured vs. simulated magnitude variation.
5.3 60GHz SSB Transmitter in 0.18\(\mu\)m SiGe BiCMOS

Figure 5.26: 65GHz polyphase filter matching at ports 1+ and 3-.

Figure 5.27: 65GHz polyphase filter matching at ports 2+ and 3+.

Figure 5.28: 5GHz polyphase filter matching at ports 1- and 3-.

Figure 5.29: 5GHz polyphase filter matching at ports 1+ and 2-.
inductance in one of the bias decoupling capacitors connected to the cascode of the first stage (Figure 5.32). The 8µm wide, 108µm long ground connection should have been made wider to minimize the parasitic inductance. The ground inductance acts as a common-mode inductance at the bases of the cascodes and, together with the $C_\pi$ of the transistors, produces negative resistance looking into the cascode bases. The amount of inductance (73pH) was verified by simulating the metal 1 interconnect in ASITIC. This inductance was then added in the schematic, where similar oscillations were re-created in simulation.

Figure 5.31: Measured and simulated DC operation of 3-Stage SiGe PA.
5.3 60GHz SSB Transmitter in 0.18µm SiGe BiCMOS

Figure 5.32: Parasitic ground inductance in PA stage 1 layout.

Figure 5.33: Parasitic ground inductance in PA stage 1 schematic.

A final test for the 3-stage PA was to examine its large signal behaviour on the spectrum analyzer. The test setup is shown in Figure 5.34, and is similar to the spectrum test for the BPSK transmitter, with the Agilent E4448A 3Hz-50GHz Power Spectrum Analyzer and the external Agilent 11970V waveguide harmonic mixer.

Figure 5.34: Power amplifier spectrum test setup.

The objectives of the spectrum test were to capture the oscillation at nominal conditions, and to investigate the behaviour of the PA when the bias of the first stage is
5.3 60GHz SSB Transmitter in 0.18µm SiGe BiCMOS

Figure 5.35: SiGe HBT PA output spectrum: oscillation at nominal conditions.

Figure 5.36: SiGe HBT PA output spectrum: no oscillation with lowered $V_{b1}$.

Figure 5.37: SiGe HBT PA gain vs. frequency characteristic.

Figure 5.38: SiGe HBT PA P1dB with lowered $V_{b1}$ at 54.5GHz.

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Terry Yao
independently controlled. Tests performed on two different dice revealed that oscillation occurs at nominal operating conditions ($V_{CC}$ and all $V_{bias}$ set to 3.3V), with an amplitude of about -16dBm at 55-56GHz (Figure 5.35). However, reducing the $V_{bias}$ of the first stage to $\approx$2V eliminated the oscillation (Figure 5.36), and gain was observed in the 54-55GHz range. A plot of the gain vs. frequency characteristic for one of the dice is shown in Figure 5.37. The overall PA linearity degraded with the lowering of the bias for the first stage, as depicted in the $P_{1dB}$ plot of Figure 5.38. The spectrum tests for the PA breakout proved to be a valuable experiment in understanding the specific bias conditions for eliminating the oscillation under large signal test conditions, and for identifying the operation frequency at which maximum PA gain can be extracted.

5.3.3. Full SSB Transmitter

The die photo of the SSB transmitter is shown in Figure 5.39. The transmitter was characterized through a series of spectral tests in which the conversion gain, LO isolation and image rejection under different operating conditions were measured. Characterization of the various breakout structures was crucial to understanding the behaviour and finding the optimal operating condition of the transmitter. Figure 5.40 shows the setup for the transmitter spectral tests. The setup is similar to that for the PA spectral test, with the external Agilent harmonic mixer used to enable measurements up to 70GHz on the PSA. An Agilent RF signal source provided the 5GHz IF input, while the output was monitored on the PSA. The transmitter was verified to be functional on 8 dice tested.
5.3 60GHz SSB Transmitter in 0.18µm SiGe BiCMOS

Figure 5.39: Die photo of 60GHz SSB transmitter (1.8mm × 1mm).

Figure 5.40: SSB transmitter spectrum test setup.
The simulated (nominal) DC operating points and the measured (optimal) DC operating points for the transmitter are summarized in Table 5.2. The optimal bias condition (selected as the typical values for the 8 transmitters tested) represents the maximum PA bias for which no oscillation occurred, as well as the LO frequency that resulted in maximum gain from the PA in the lower side band for a 5GHz IF input. This corresponds to an LO of 61GHz and a lower-sideband transmitter output of 56GHz.

Table 5.2: DC operating points for SSB transmitter.

<table>
<thead>
<tr>
<th>Block</th>
<th>Nominal (In Simulation)</th>
<th>Optimal (In Measurement)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA + Mixer</td>
<td>3.3V (109mA)</td>
<td>3V (81mA)</td>
</tr>
<tr>
<td>EF Buffers</td>
<td>4V (48mA)</td>
<td>4.3V (49mA)</td>
</tr>
<tr>
<td>VCO $V_{CC}$, $V_{BIAS}$</td>
<td>4V (62mA)</td>
<td>4.8V (86mA)</td>
</tr>
<tr>
<td>VCO $V_{CNTRL}$</td>
<td>1V (&lt;1mA)</td>
<td>1V (&lt;1mA)</td>
</tr>
<tr>
<td>Total Power</td>
<td>800mW</td>
<td>868mW</td>
</tr>
</tbody>
</table>

Sample screen shots of the transmitter spectra are shown in Figures 5.41-5.45. In Figure 5.41, the IF input was turned off, and the PA/Mixer bias was reduced to 2.8V to eliminate the oscillation from the PA. Thus, the resulting spectrum only shows the LO feedthrough of -38dBm at 60.9GHz. Figures 5.42 and 5.43 show the output spectra for 5GHz IF input signals of -30dBm and -24dBm, respectively. The resulting spectra from a sweep of the IF input frequency in the 4-6GHz range with an IF amplitude of -15dBm are shown in Figures 5.44 and 5.45. The actual power levels in Figure 5.42 are 4dB higher than shown in the spectral plot to account for the losses in the output decoupling capacitor, 1mm-cable and adaptors. This offset has already been accounted for in the rest of the spectral plots.

The transmitter performance, as characterized in the spectral tests, is summarized in the plots below. Losses in the cables, decoupling capacitors, adaptors, and probes have all been de-embedded from the raw measured data. The transmitter has a measured maximum upconversion gain of 17.5dB and better than 45dB image rejection in its linear operating range. The maximum LO feedthrough is -38dBm at 61GHz. The reduction of the first stage PA bias for eliminating the oscillation resulted in lower than expected output power and linearity. The decrease in image rejection for high IF input powers
Figure 5.41: No oscillation from PA with PA/Mixer bias reduced to 2.8V; no IF input; LO feedthrough of -38dBm at 61GHz.

is also caused by the linearity degradation when lowering the PA bias. The measured performance of the transmitter is summarized in Table 5.3.

Table 5.3: SSB transmitter measured performance summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX Conversion Gain (Single-Ended)</td>
<td>17.5dB</td>
</tr>
<tr>
<td>TX $O_{IP_{dB}}$ Compression @ 56GHz (Single-Ended)</td>
<td>-13dBm</td>
</tr>
<tr>
<td>TX Image Rejection</td>
<td>&gt; 45dB</td>
</tr>
<tr>
<td>LO Feedthrough @ 61GHz</td>
<td>&lt; −38dBm</td>
</tr>
<tr>
<td>IF Range</td>
<td>2-8GHz</td>
</tr>
<tr>
<td>Total Power</td>
<td>868mW</td>
</tr>
</tbody>
</table>
Figure 5.42: Transmitter output spectrum: IF input at 5GHz, -30dBm; LO at 61GHz; image rejection of 47.2dB.

Figure 5.43: Transmitter output spectrum: IF input at 5GHz, -24dBm; LO at 61GHz; image rejection of 48.9dB.

Figure 5.44: Transmitter output spectrum: IF input at 4GHz, -15dBm; LO at 61GHz; image rejection of 33.6dB.

Figure 5.45: Transmitter output spectrum: IF input at 6GHz, -15dBm; LO at 61GHz; image rejection of 40dB.
5.3 60GHz SSB Transmitter in 0.18µm SiGe BiCMOS

![Graph of Output Power vs. IF Power at 5GHz](image1)

Figure 5.46: USB, LSB, LO vs. IF input power with IF at 5GHz and LO at 61GHz.

![Graph of Conversion Gain](image2)

Figure 5.47: Transmitter upconversion gain.

![Graph of Image Rejection vs. IF Input](image3)

Figure 5.48: Image rejection vs. IF input power with IF at 5GHz and LO at 61GHz.
5.4. Summary

The experimental procedure and results for the CMOS PA, BPSK transmitter and SSB transmitter have been presented in this chapter. Both the CMOS PA and BPSK transmitter were verified to be functional, while the individual characterization of the polyphase filter and SiGe PA breakouts greatly aided in the understanding of the system-level operation of the SSB transmitter. The 0.18µm SiGe HBT and the 90nm CMOS devices proved to be very well-modeled, and the various S-parameter tests also validated the suitability of ASITIC for inductor modeling, and hence for the design of narrow-band tuned circuits where accurately designed matching networks are needed.
Conclusion

6.1. Summary

The design and implementation of mm-wave radio transmitters and their building blocks have been presented in this thesis.

This work was motivated by the opportunities and challenges that the 60GHz region presents for short-range, high-density wireless links, and an examination of the current state-of-the-art in 60GHz research, where the focus has only been on building blocks and the receiver. A system-level analysis, based on a link budget calculation for a 60GHz system, was presented in Chapter 2, followed by a look at possible transmitter architectures and device-level considerations for mm-wave radio implementation.

The power amplifier was explored in detail in Chapter 3, through the designs of two 3-stage, 60GHz PAs in 0.18$\mu$m SiGe BiCMOS and 90nm CMOS. While the SiGe HBT implementation has higher gain to compensate for the losses of the polyphase filters in the SSB transmitter, the CMOS PA achieves better efficiency due its common-source topology with a reduced voltage supply.

Chapter 4 presented the designs of a directly-modulated BPSK transmitter and an SSB transmitter with on-chip VCO, both implemented in 0.18$\mu$m SiGe BiCMOS. The integration of a differential cascode Colpitts oscillator and a mixing quad results in a compact BPSK transmitter suitable for low-cost, low-power mm-wave sensor applications. The SSB transmitter offers a more sophisticated approach for the radio application, and demonstrates the use of polyphase filters at 5GHz and 65GHz in the image reject mixer. In addition to the polyphase filters, the transmitter also integrates two upconvert Gilbert
6.2 Contributions

Contributions from this thesis include a 60GHz PA in 90nm CMOS which, to the best of the author’s knowledge, represents the highest frequency PA in CMOS to date\textsuperscript{1}; a novel and compact 65GHz BPSK transmitter for mm-wave sensor applications; and the first 60GHz SSB transmitter which demonstrates the use of a 65GHz polyphase filter for on-chip image rejection.

6.3. Improvements and Future Work

An improvement that can made in this work is the re-design of the 3-stage SiGe HBT PA to eliminate the oscillation problem, and hence the need to reduce the first stage bias which degrades linearity. The output linearity should also be improved, since the PA should ideally deliver at least 10dBm rather than the 7dBm that resulted from the cascading of the 3 stages. This can be more easily accomplished by using a 2-stage cascade. Additionally, the gain of the 90nm CMOS PA can be increased by employing

\textsuperscript{1}The next highest frequency CMOS PA is a 40GHz implementation in 0.18\,\mu m CMOS [50]
the cascode topology rather than the CS for the first and second stages, while still using a CS final stage for maximum output drive capability.

At the system level, the next step would be the full integration of a 60GHz receiver and transmitter, along with a 60GHz PLL for VCO frequency stabilization. Frequency dividers in SiGe operating beyond 70GHz with 3.3V supply have already been demonstrated here at U of T. On-chip microstrip patch antennas can also be integrated on the transmit and receive sides, forming a complete transceiver front-end. Yet another unexplored area is packaging design and modeling for the mm-wave transceiver.

As interest in low-cost 60GHz radio continues to drive research in industry and academia, it is only a matter of time before an all-CMOS transceiver front-end is realized, which can be integrated with the baseband DSP and IF processing functions to form a full radio SoC. The 90nm CMOS PA presented in this thesis can serve as a starting point for a 60GHz CMOS transmitter. However, due to stringent requirements on tank swing, the feasibility of using CMOS for low-phase noise VCOs with sufficient output power at 60GHz to drive upconvert mixers on-chip remains unproven and, together with a 60GHz frequency divider in CMOS, will no doubt be one of the biggest challenges in an all-CMOS implementation.


[41] ———, “RF and millimeter-wave IC design in the nano-(Bi)CMOS era,” in Si-Based RF IC. Transworld Research Publisher, 2006.


A total of 49 spiral inductors were used in this thesis for on-chip impedance matching and degeneration. These include 9 in the 90\textit{nm} CMOS PA, fabricated in a 9-metal layer backend, 6 in the BPSK transmitter in 0.18\textit{µm} SiGe BiCMOS, with a 6-metal layer backend, and 34 in the SSB transmitter in 0.18\textit{µm} SiGe BiCMOS. The structure of the inductors vary from the most common rectangular spirals implemented in the top metal layer, to the octagonal spirals used for reducing on-chip antenna effects caused by radiation from the sharp corners, to finally, the multi-metal stacked spirals used in the 5GHz polyphase filter for area efficiency. The sections below provide examples on the design and implementation of each type of inductor structure, including a rectangular spiral inductor in 90\textit{nm} CMOS, an octagonal spiral inductor in 0.18\textit{µm} SiGe BiCMOS and a rectangular multi-metal stacked inductor in 0.18\textit{µm} SiGe BiCMOS.

### A.1. Inductor Design and Layout

Below are some useful techniques for designing inductors with high Q and high SRF:

- small footprint to minimize electric coupling to substrate for high SRF, PQF
- narrow metal, wide spacing and minimum diameter for high SRF
- wide, thick metal and shunted metal layers for high Q
- large diameter, narrow metal, multi-layer series-connected metal layers for large L
- substrate contacts placed 30\textit{µm} – 50\textit{µm} away from inductor to reduce eddy currents in substrate
A.2 Inductor Modeling

All inductors are modeled using the 2-\(\pi\) network shown in Figure A.4. Table A.1 summarizes the design and modeled parameters for each inductor example.
Table A.1: Inductor sizing and modeling parameters for rectangular (90nm CMOS), octagonal (0.18µm SiGe) and multi-metal (0.18µm SiGe) inductors.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rectangular 60pH</th>
<th>Octagonal 160pH</th>
<th>Multi-Metal 1.4nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90nm CMOS</td>
<td>0.18µm SiGe</td>
<td>0.18µm SiGe</td>
</tr>
<tr>
<td>ASITIC Type</td>
<td>sq spiral</td>
<td>sq spiral</td>
<td>sq spiral</td>
</tr>
<tr>
<td>Metal Layer</td>
<td>9</td>
<td>6</td>
<td>5.6</td>
</tr>
<tr>
<td>Length (µm)</td>
<td>24</td>
<td>50</td>
<td>52</td>
</tr>
<tr>
<td>Turns</td>
<td>1.5</td>
<td>1.75</td>
<td>2.5</td>
</tr>
<tr>
<td>Width (µm)</td>
<td>2</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Spacing (µm)</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>L (pH)</td>
<td>25</td>
<td>72.6</td>
<td>627.5</td>
</tr>
<tr>
<td>Cp (fF)</td>
<td>8</td>
<td>1</td>
<td>10.7</td>
</tr>
<tr>
<td>Rm (Ω)</td>
<td>0.4</td>
<td>1.3</td>
<td>13.6</td>
</tr>
<tr>
<td>Rf (Ω)</td>
<td>0.7</td>
<td>0.7</td>
<td>3.7</td>
</tr>
<tr>
<td>Lf (pH)</td>
<td>5.6</td>
<td>8.1</td>
<td>69.7</td>
</tr>
<tr>
<td>Cox11 (fF)</td>
<td>1.3</td>
<td>2.1</td>
<td>3.1</td>
</tr>
<tr>
<td>Cox12 (fF)</td>
<td>2.5</td>
<td>3.9</td>
<td>8.0</td>
</tr>
<tr>
<td>Cox22 (fF)</td>
<td>1.2</td>
<td>1.8</td>
<td>5</td>
</tr>
<tr>
<td>Cs11 (fF)</td>
<td>2</td>
<td>1.8</td>
<td>1.1</td>
</tr>
<tr>
<td>Cs12 (fF)</td>
<td>4.3</td>
<td>4</td>
<td>2.1</td>
</tr>
<tr>
<td>Cs22 (fF)</td>
<td>2.3</td>
<td>1.8</td>
<td>1</td>
</tr>
<tr>
<td>Rsub11 (kΩ)</td>
<td>7.5</td>
<td>6.4</td>
<td>15.6</td>
</tr>
<tr>
<td>Rsub12 (kΩ)</td>
<td>2.9</td>
<td>3.3</td>
<td>2.2</td>
</tr>
<tr>
<td>Raub22 (kΩ)</td>
<td>4.8</td>
<td>7</td>
<td>2.6</td>
</tr>
</tbody>
</table>
A.3. Matlab Script

The following is the Matlab script used to generate the inductor model parameters based on 2-port Y-parameters provided by ASITIC:

```matlab
%==================================================
%Inductor Modeling Script (Matlab)
%==================================================
clear all
close all
clc
[freq, y11r, y11i, y12r, y12i, y21r, y21i, y22r, y22i]=textread('ind160p.txt', '%f %f %f %f %f %f %f %f %f %f %f');

defreq=(freq)*1e9;
w=2*pi*freq;
y11=y11r+i*y11i;
y12=y12r+i*y12i;
y21=y21r+i*y21i;
y22=y22r+i*y22i;
Qeff=imag(-y11)./real(y11);
Leff=imag(1./y11)./w;
Ltot=0;
for a=1:10
L(a)=imag((-1./y12(a)))/w(a);
Ltot=Ltot+L(a);
end
L=Ltot/10
R=real((-1./y12(1)));
Cox1=(-1/(imag(1/(y11(1)+y12(1)))))/w(1);
Cox2=(-1/(imag(1/(y22(1)+y12(1)))))/w(1);
Rsub1=1/(y11(1)+y12(1));
zsub1=1/(y11(1)+y12(1));
xc1=1/(i*w(1)*Cox1); line1=1/(zsub1-zcox1);
Rsub1=1/real(line1);
zsub2=1/(y22(1)+y12(1));
zcox2=1/(i*w(1)*Cox2);
line2=1/(zsub2-zcox2);
```

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Rsub2 = 1/real(line2);

% High Freq Extraction
range = 10:1:40;
%Cp
jwcp = (-y12(range)-1./(R+i*w(range)*L));
p = polyfit(w(range)/1e9, imag(jwcp), 1);
Cp = p(1)/1e9
Cp = 1e-15

%Cs
zsub1 = 1./(y11(range)+y12(range));
line1 = 1./(zsub1-(1./(i*w(range)*Cox1)));
pcs = polyfit(w(range)/1e9, imag(line1), 1);
Cs1 = pcs(1)/1e9;

zsub2 = 1./(y22(range)+y12(range));
line2 = 1./(zsub1-(1./(i*w(range)*Cox2)));
pcs = polyfit(w(range)/1e9, imag(line2), 1);
Cs2 = pcs(1)/1e9;

%=================================================
%Pi model
%Skin Effect
%Cp = 1.1e-15;
Rm = 4*R;
Rf = 3.7*R;
Lf = 0.04*L;
Ls = 0.88*L;
%[freq2, y11r, y11i, y12r, y12i, y21r, y21i, y22r, y22i] = textread('bb.txt', '%f %f %f %f %f %f %f %f %f %f %f %f %f %f');
%freq2 = (freq2)*1e9;
%w = 2*pi*freq2;
Zskin = Rm.*(Rf+i*w*Lf)./(Rm+Rf+i*w*Lf);
Zcp = 1./(i*w*Cp);
Zcox1 = 1./(i*w*Cox1);
Zcox2 = 1./(i*w*Cox2);
Zsub1 = Rsub1./(1+i*w*Rsub1*Cs1);
Zsub2 = Rsub2./(1+i*w*Rsub2*Cs2);
Z1 = Zcox1 + Zsub1;
Z2 = Zcox2 + Zsub2;
Z3a = (i*w*Ls) + Zskin;
\[ Z3 = Z3a \cdot Zcp / (Z3a + Zcp) \]
\[ y_{11s} = (1/Z1) + (1/Z3); \quad \% y_{11} = y_1 + y_2 \]
\[ y_{21s} = -1/Z3; \]
\[ y_{12s} = -1/Z3; \]
\[ y_{22s} = (1/Z3) + (1/Z2); \]
\[ Q_{effs} = \text{imag}(-y_{11s}) / \text{real}(y_{11s}); \]
\[ L_{effs} = \text{imag}(1/y_{11s}) / w; \]
\[ \text{if (0==1)} \]
\[ \% \text{plot(freq/1e9, Q_{effs}, '-', freq/1e9, Q_{eff}, 'x')} \]
\[ \text{plot(freq2/1e9, Q_{effs}, '-')} \]
\[ \text{hold on} \]
\[ \text{grid on} \]
\[ \text{plot(freq/1e9, Q_{eff}, 'x')}; \]
\[ \text{set(gca,'FontSize',14)} \]
\[ \text{legend ('Model', 'Measured',2)}; \]
\[ \text{title ('ASITIC Inductor - Q_{eff} (Pi Model with Skin Effect')}); \]
\[ \text{ylabel ('Q_{eff}')}; \text{xlabel('Frequency (GHz)')}]; \]
\[ \text{figure} \]
\[ \% \text{plot (freq/1e9, L_{effs}, '-', freq/1e9, L_{eff}, 'x')} \]
\[ \text{plot(freq2/1e9, L_{effs}, '-')} \]
\[ \text{hold on} \]
\[ \text{grid on} \]
\[ \text{plot(freq/1e9, L_{eff}, 'x')}; \]
\[ \text{set(gca,'FontSize',14)} \]
\[ \text{legend ('Model', 'Measured',2)}; \]
\[ \text{title ('ASITIC Inductor - L_{eff} (Pi Model with Skin Effect')}); \]
\[ \text{ylabel ('L_{eff} (H)'); xlabel('Frequency (GHz)')}]; \]
\[ \text{end} \]
\[ \% \text{2-Pi Model} \]
\[ \text{if (1==1)} \]
\[ Z_{cp} = 1/(i*\text{w*Cp}); \]
\[ L2 = L/2; \]
\[ R2 = R/2 \]
\[ \% \text{Skin Effect} \]
\[ Rm2 = 3*R2 \]
\[ Rf2 = 0.5*Rm2 \]
\[ Lf2 = 0.1*L2 \]
\begin{verbatim}
   L2=0.9*L2
   Zskin2=Rm2.*(Rf2+i*w*Lf2)./(Rm2+Rf2+i*w*Lf2);
   Cox12=Cox1/2
   Cox22=Cox2/2
   Rsub12=Rsub1*2
   Rsub22=Rsub2*2
   Cs12=Cs1/2
   Cs22=Cs2/2
   Cox3=Cox12+Cox22
   Cs3=(Cs1+Cs2)/2
   Rsub3=2*(Rsub1*Rsub2)/(Rsub1+Rsub2)
   newZsub1=Rsub12./(1+i*w*Rsub12*Cs12);
   newZcox1=1./(i*w*Cox12);
   newZ1=newZcox1+newZsub1;
   newZsub2=Rsub3./(1+i*w*Rsub3*Cs3);
   newZcox2=1./(i*w*Cox3);
   newZ3=newZcox2+newZsub2;
   newZ2=(i*w*L2)+Zskin2;
   Zeq1=newZ1.*Zcp./(newZ1+Zcp);
   Zeq2=newZ2.*newZ3./(newZ2+newZ3);
   Zeq3=newZ2+Zeq2;
   Zeq=Zeq1.*Zeq3./(Zeq1+Zeq3);
   newy11s=1./Zeq;
   newQeffs=imag(-newy11s)./real(newy11s);
   newLeffs=imag(1./newy11s)./w;
   plot (freq/1e9, newQeffs, '-', freq/1e9, Qeff, 'x');
   set(gca,'FontSize',14)
   legend ('Model', 'Measured',2);
   title ('ASITIC Inductor - Qeff (2 Pi Model with Skin Effect)');
   ylabel ('Qeff'); xlabel('Frequency (GHz)');
   figure
   plot (freq/1e9, newLeffs, '-', freq/1e9, Leff, 'x');
   set(gca,'FontSize',14)
   legend ('Model', 'Measured',2);
   title ('ASITIC Inductor - Leff (2 Pi Model with Skin Effect)');
   ylabel ('Leff (H)'); xlabel('Frequency (GHz)');
end
\end{verbatim}