

# ECE 1718 Special Topics in Computer Hardware Design: Modern and Emerging Architectures

## Instructor

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- Office: EA321 (Engineering Annex)
- Meetings anytime, by appointment

## Admin Assistant

- Luna Boodram
- EA316 (Engineering Annex)

## Summary

The focus of this course will be on computer architecture, with an emphasis on real life modern and emerging microprocessor architectures. The course is divided into two phases. The first phase will provide a thorough (but speedy) background in modern microprocessor architecture, covering instruction-sets, pipelining, multiple and out-of-order instruction issue, the memory system and caching, and parallel architectures; this phase will include several homeworks which provide hands-on experience with architectural simulation of the mechanisms described in class, as well as preparation for the project. The second phase of the course will switch gears: we will study current research and development of emerging architectures including simultaneous multithreading, reconfigurable/programmable hybrids, grid processors, network processors, thread-level speculation, and architectures for nanotechnology; in this phase we will read research papers, and through the class project implement and evaluate new ideas. Students are welcome to suggest topics for class discussion and/or projects.

## Topics Covered (subject to change based on experience of class)

1. Introduction to Computer Architecture
  - A brief history of architecture
  - Current issues
  - Where are we headed?
2. Uniprocessor Architecture
  - ISAs and compilers
  - Single-issue processors
  - Pipelining
  - Superscalar processors (wide-issue, out-of-order issue, speculation and prediction)
3. Memory Systems
  - Memory hierarchies, caching, and the importance of data layout
  - Virtual vs physical memory
  - Latency tolerance
4. Parallel Programming and Architectures
  - Shared-memory vs message passing
  - Synchronization
  - Interconnection networks
  - Coherence and consistency
5. Emerging Architectures (research readings)
  - Helper Threads
  - Thread-level speculation
  - Reconfigurable hybrids
  - Network processors
  - Streaming processors
  - Grid processors
  - Nanotechnology?
  - Other suggestions?

## Administrivia

- Lectures: Wednesdays 2-4pm, TBA
- Course web page: <http://www.eecg.toronto.edu/~steffan/teaching/ece1718S>

## Prerequisites/Conditions

- Basic knowledge of computer architecture and organization is required
- Solid experience in C/unix programming required, experience with C++, perl, RCS/CVS, is an asset
- It is highly recommended that students have taken ECE341/352 (computer organization), ECE385 (microprocessor systems) or equivalent
- ECE552 (computer architecture) is an asset but not required.
- You may not take this course for credit if you have already taken ECE1773-Computer Architecture (except by permission of the instructor)

## Materials

- Recommended textbook: “Computer Architecture: A Quantitative Approach”, J. L. Hennessy and D. A. Patterson, Morgan Kaufmann Publishers.
- The second phase of the course will consist of several readings of current research in computer architecture.
- See the course web page for more information.

## Homeworks

There will be homeworks (during the first phase of the course) which provide hands-on experience with architectural simulation of the mechanisms described in class, as well as preparation for the project.

## Project

Implement and evaluate new ideas or compose a survey based on topics suggested by student or the instructor. Grading will be based on a brief proposal, interim and final reports, and a short presentation at the end of the semester.

## Grading

- Homework: 30%
- Project: 40%
- Reviews: 10%
- Lecture: 10%
- Class participation: 10%