

# ECE 1755: Parallel Computer Architecture and Programming

## Instructor

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- Office: EA321 (Engineering Annex)
- Meetings anytime (by appointment is best for longer discussions)

## Admin Assistant

- Luna Boodram
- EA316 (Engineering Annex)

## Summary

Computer architectures that exploit thread-level parallelism are becoming increasingly commonplace. This course explores the evolution of modern parallel architectures, and is divided into two phases. The first phase will provide a brief background and history of modern microprocessor architecture. We will then investigate in detail the design and operation of modern parallel architectures, with a brief look at how they are programmed. This phase will include several homeworks which provide hands-on experience with architectural simulation of the mechanisms described in class, and evaluation using real parallel machines.

The second phase of the course will switch gears: we will study current research and development of emerging parallel architectures including simultaneous multithreading, reconfigurable/programmable hybrids, grid processors, network processors, thread-level speculation, and architectures for nanotechnology; in this phase we will read research papers, and through the class project implement and evaluate new ideas. Students are welcome to suggest topics for class discussion and/or projects.

## Topics Covered

1. Introduction and Background
  - Basic compiler concepts
  - Performance Analysis
2. Uniprocessor Architecture and Memory Systems
  - Pipelining
  - Superscalar processors (wide-issue, out-of-order issue, speculation and prediction)
  - Memory hierarchies, caching, and the importance of data layout
  - Latency tolerance
3. Trends
  - A brief history of architecture
  - Current issues
  - Where are we headed?
  - The IBM Cell processor
4. Parallel Programming
  - Shared-memory vs message passing
  - Synchronization
5. Conventional Parallel Architectures
  - Interconnection networks
  - Coherence and consistency
6. Emerging Parallel Architectures (research readings)
  - Helper Threads
  - Thread-level speculation
  - Reconfigurable hybrids
  - Network processors
  - Streaming processors
  - Grid processors
  - Nanotechnology?
  - Other suggestions?

## Administrivia

- Lectures: Wednesdays 2-4pm, BA2130
- Course web page: <http://www.eecg.toronto.edu/~steffan/teaching/ece1755F>

## Prerequisites/Conditions

- Basic knowledge of computer architecture and organization is required
- Solid experience in C/unix programming required, experience with C++, perl, RCS/CVS, is an asset
- It is highly recommended that students have taken ECE341/352 (computer organization), ECE385 (microprocessor systems) or equivalent
- ECE552 (computer architecture) is an asset but not required.
- You may not take this course for credit if you have already taken ECE1773-Computer Architecture (except by permission of the instructor)

## Materials

- Recommended textbook: *Parallel Computer Architecture, A Hardware/Software Approach* David Culler, J.P. Singh, Anoop Gupta; Morgan Kaufmann Publishers.
- The second phase of the course will consist of several readings of current research in computer architecture.
- See the course web page for more information.

## Homeworks

There will be homeworks (during the first phase of the course) which provide hands-on experience with architectural simulation of the mechanisms described in class, as well as preparation for the project.

## Project

Implement and evaluate new ideas or compose a survey based on topics suggested by student or the instructor. Grading will be based on a brief proposal, interim and final reports, and a short presentation at the end of the semester.

## Grading

- Homework: 30%
- Project: 40%
- Reviews: 10%
- Lecture: 10%
- Class participation: 10%