Reconfigurable Computing with the Partitioned Global Address Space model

Cascadia 2012

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August 14, 2012
Parallelizing computation: How to partition, communicate and synchronize data?
Parallel Programming Models

- Process or Thread
- Address Space

- Message Passing
  e.g. MPI

- Shared Memory
  e.g. OpenMP

- PGAS
  e.g. UPC
Partitioned Global Address Space

• Any thread can access any memory location, but:
  
• There is a visible difference between local and remote memory locations
  
• One-sided communication (remote read and write without local thread involvement)
Language Level PGAS: Unified Parallel C (UPC) example

```c
#define N 100*THREADS

shared int [*] v1[N], v2[N], sum[N];

void main()
{
    int i;
    upc_forall(i=0; i<N; i++; &v1[i])
        sum[i]=v1[i]+v2[i];  // all work is local
}
```

Others: Co-Array Fortran, Titanium (Java), Chapel (Cray), X10 (IBM)
Application Library Level PGAS: Global Arrays
Communication Level PGAS:
GASNet (Global Address Space Networking)

Others: ARMCI (Global Arrays), SHMEM (App level)
Network Level PGAS: Remote DMA (RDMA)

Examples: Infiniband, Myrinet, iWARP, RoCE
CPUs+FPGAs: Co-processor Style
CPUs+FPGAs: Symmetric Style
What does „symmetric“ mean?

• CPU code and FPGA components can both initiate data sends and requests
• Both use a similar or identical API to ease migration
• For distributed-memory/message-passing, TMD-MPI / ArchES-MPI implement this
• Our work strives to build a symmetric PGAS system based on GASNet
GASNet Active Messages

Remote Write: Long Request Message
GASNet Active Messages

Remote Read: Long Reply Message
GAScore FPGA component
GAScore FPGA system
BEE3 multi-FPGA system
Next steps: Hardware

• External DRAM support (caching...?)

• Strided and scatter/gather transfers

• Messaging management for custom hardware cores
Next steps: Hardware
Programmable Active Message Sequencer

• Programmable/re-programmable through GASNet messages
• Controls/synchronizes custom hardware
• Handles reception and transmission of GASNet active messages
• Sequences based on: custom hardware state, timer, amount of received data, number of received messages of a specific type
Next steps: Toolchain challenges for FPGAs in HPC

- PGAS languages without heterogeneity support (UPC, CAF, Titanium)

- PGAS languages without clear HLL-to-FPGA path (Chapel, X10)

- Lack of FPGA programming experts in HPC
Next Steps: Toolchain

CPU-based Host

GASNet Library

C++ generated code

Heterogeneous C++ PGAS Library

DSL application

Compile

GASNet

Dynamic generation

Static generation

manually or C-to-gates

PAMS

Custom FPGA Hardware

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Heterogenous C++ PGAS library

- Concepts stolen from Global Arrays, Chapel, X10
- Specialized data classes for multi-dim. arrays, etc.
- Location and subgroup classes
- Distribution and layout types; assigned to arrays to define storage and computation patterns
- Can at compile-time as well as runtime generate and distribute PAMS code
- Can be used as a runtime library for code generation from Domain-Specific Languages (DSLs)
Thank you for attention!

Questions?