Outline

- Bridge Fault Model
- Bridge Fault Simulation
- Test Generation for Bridge Fault

Bridge Fault Model

- After single stuck-at faults, bridge faults are the most important class of faults.
- Most commonly occurring type of fault.
- Simplified model assumes 0\(\Omega\) resistance (short) between two lines (dotted line in the figure)
Bridge Fault Model

- Wired-AND
  - $y=0 \rightarrow x$ is s-a-0
  - Test for bridge fault:
    - Set $y$ to 0 and test for $x$ s-a-0
    - Set $x$ to 0 and test for $y$ s-a-0

- Wired-OR
  - $y=1 \rightarrow x$ is s-a-1
  - Test for bridge fault:
    - Set $y$ to 1 and test for $x$ s-a-1
    - Set $x$ to 1 and test for $y$ s-a-1

- Dominant driver
  - $x$ always outdrives $y$
  - $y$ always outdrives $x$

Assumes 0Ω resistance
Bridge Fault Model

- Need to consider drive strengths of bridged nodes to determine voltage level.

Gates driven by the bridged nodes may interpret the voltage level differently, depending on their logic threshold voltages.

- Byzantine Generals Problem
**Feedback Bridge Faults**

- In a feedback bridge fault, there exists at least one path between the two bridged nodes.
  - The back line \( b \) is the line closest to the PI's.
  - The front line \( f \) is the line closest to the PO's.

- **AND:**
  - set \( b=0 \) and test for \( f \rightarrow a \rightarrow 0 \) (no logical feedback)
  - set \( f=0 \) and test for \( b \rightarrow a \rightarrow 0 \), but not through \( f \) (i.e., \( f \) is not sensitive to \( b \)).

- If a feedback loop involves an odd number of inversions, the circuit may oscillate.
  - **AND-bridge**
  - **OR-bridge**
Bridge Faults

- **Output-to-Output**
  - Between metal lines in routing channels
  - Outputs of different gates.
- **Input-to-Input**
  - Between inputs of the same gate in polysilicon
- **Input-to-Output**
  - Between an input and output of the same gate
- **Source-to-Drain**
  - Between source and drain of the same transistor in diffusion.
- **BART** [Patel et al., 1996]: Bridge Fault Test Generator

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Input-to-Output Short

- In a simple CMOS gate, if the short causes an error, then input value is forced upon the output [Vierhaus, Meyer, Glaser, ITC’93]
- This is also true for complex CMOS gates such as And-Or-Invert (AOI) and Or-And-Invert (OAI) gates
  - [Cusey, M.S. Thesis, 1993]
- Test vectors for input and output stuck-at faults cover Input-to-output shorts.
- Input-to-Output shorts not targeted in BART
Source-to-Drain Short

- Also called transistor stuck-on fault.
  - Not strictly a logic fault.
  - However, any test vector that detects such a fault must always detect some structurally related logic stuck-at fault.
- Source-drain shorts not targeted in BART.

Logic Model for a Bridge

```
A
B
C
D

0
1
0

G,H = 0,0
G,H = 1,1
G,H = 0,1
G,H = 1,0

FAULT-FREE       FAULTY       MODEL
G,H = 0,1        G,H = 0,0    H s-a-0
              G,H = 1,1    G s-a-1
G,H = 1,0        G,H = 0,0    G s-a-0
              G,H = 1,1    H s-a-1
```
One of Four Possible Error Manifestations

Circuit Modification for ATPG

- All four possible manifestations of a bridge are simultaneously addressed in a single circuit modification:
  - Adds about 10 gates per bridge.
- Four single stuck-at faults in the modified circuit represent the four error manifestations.
- ATPG can be used to generate four possible test vectors.
- Test generation complexity is the same as a stuck-at fault test generation.
Strong and Weak Logic Values

A
1
weak 1
G
?

B
0

C
1
weak 0
H
?

D
0


A
0
strong 1
G
1

B
0

C
1
weak 0 -> 1
H
1 (error)

D
0


Generalized Bridge Model

A
B

C
D

Bridge Function

MUX
0

MUX
1

MUX
0

MUX
1

H
G

F
X
s-a-1

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BART Test Generation

- Faults extracted by a randomly generated list
- Site of the target bridge modified according to the strength model.
- ATPG generates tests for the 4 stuck-at faults.
- If strength values cannot be justified, BART reverts to the normal logic value model.
- BART generates vectors for 10 target bridges before invoking a fault simulator