University of Toronto

Term Test 1

Date - Oct 23, 2015 (1:10pm to 2:00pm)

Duration: 50 min

ECE331 — Analog Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Equation sheet is on last page of test.

2. Unless otherwise stated, use transistor parameters on equation sheet and assume $g_m r_o \gg 1$.

3. Non-programmable calculator allowed; No other aids allowed

4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

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<th>Question</th>
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Last Name: _______________________

First Name: _____________________

Student #: _____________________  (max grade = 24)
[6] Question 1:

a) Find the intrinsic gain of a transistor with \( L = 0.25\mu m \) and \( V_{ov} = 0.2V \) (based on the 0.18\( \mu m \) parameters given on the equation sheet)

b) If \( g_m = 2\text{mA/V} \) is required for the transistor in a), what must \( I_D \) and \( W \) be?
[6] **Question 2:** Assume an nmos transistor (based on the 0.18um parameters given on the equation sheet) with $W = 4\mu m$, $L = 0.25\mu m$ is biased with $V_{ov} = 0.3\,V$ and $V_{DS} = 0.8\,V$.

a) Find the $r_o$ for this device.

b) If $V_{DS}$ is decreased by 0.1V, what is the corresponding change in $I_D$?

c) If a cascode current mirror makes use of two nmos transistors biased with the same current as in a), find $r_o$ and the change in $I_D$ for a 0.1V change in the mirror output voltage. (assume both transistors remain in the active region).
[6] Question 3:
   a) Given 2 current sources from $V_{DD}$ where each are $10 \mu A$, design a wide-swing cascode current-mirror circuit (including bias voltage generation) that gives an nmos output of $30 \mu A$. Assume all transistor lengths are $0.18 \mu m$ and the nmos current mirror output transistors have $W = 3 \mu m$. Show the widths of all transistors on your schematic. (Hint: there should be 5 nmos transistors and 2 current sources on your schematic).

   b) Assuming $V_{tn} = 0.3 V$ and $V_{ov} = 0.2 V$, show on your circuit above, the values for the 2 bias voltages.

\[ V_{DD} \]

\[ R_D \]
\[ 1k\Omega \]

\[ M_1 \]

\[ R_S \]
\[ 1k\Omega \]

\[ I \]
\[ (\text{ideal}) \]

\[ R_2 \]
\[ 10k\Omega \]

\[ M_2 \]

\[ R_{out} \]

\[ g_{m1} = g_{m2} = 2mA/V \]

\[ r_{o1} = r_{o2} = 20k\Omega \]

a) Find \( R_{in} \) and \( R_{out} \).

b) Find \( \frac{v_o}{v_s} \)
**Analog Electronics**

**Equation Sheet**

**Constants:** $k = 1.38 \times 10^{-23}$ JK$^{-1}$; $q = 1.602 \times 10^{-19}$ C; $V_T = kT/q = 26$ mV at 300 °K; $e_0 = 8.854 \times 10^{-12}$ F/m; $\kappa_{ox} = 3.9$; $C_{ox} = (\kappa_{ox} e_0)/\lambda$

**NMOS:**
- $k_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} > 0$; $V_{GS} = -V_{tn}$
- (triode) $V_{DS} \leq V_{tn}$
- (active) $V_{DS} \geq V_{tn}$
  - $i_D = 0.5k_n a_n^2 (1 + \lambda V_{DS})$; $g_m = k_n V_{tn}$; $i_D = 2I_D/V_{tn}$

**PMOS:**
- $k_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} > 0$; $V_{GS} = V_{tn}$
- (triode) $V_{DS} \leq V_{tn}$
- (active) $V_{DS} \geq V_{tn}$
  - $i_D = 0.5k_p a_p^2 (1 + \lambda V_{DS})$; $g_m = k_p V_{tn}$; $i_D = 2I_D/V_{tn}$

**BJT:**
- $i_C = I_C e^{qV_C/V_T}$; $g_m = \omega/\tau_r = I_C/V_T$; $r_e = [V_T I_E]^2$; $r_h = \omega/g_{m}$; $r_o = [V_T I_C]$; $i_C = \beta I_E$; $i_E = (\beta + 1)/\beta$; $r_C = (\beta + 1)(r_e + R_B)/\beta$; $R_T = (R_B + R_E)/\beta$

**Cascode:**
- $R_D = (1 + g_m R_s) r_o$
- $i_C = (1 + g_m R_s)^{-1} i_E$
- $v_{GS} = v_I$

**Diff Pair:**
- $A_D = g_m R_D A_{CM} = -2R_D ((\Delta R_D)/R_D)$;
- $A_{CM} = -(R_D/2R_S) ((\Delta g_m)/g_m)$
- $V_{ox} = \Delta V_i$; $v_{os} = (V_{os}/2)((\Delta R_D)/R_D)$;
- $v_{os} = (V_{os}/2)((\Delta W/L))/(W/L)$

1st order step response $y(t) = (Y_m - Y_0)e^{-t/\tau}$

**Freq:**
- for real axis poles/zeros $T(s) = k_{dc} (1 + \omega^2 / \omega_0) (1 + \omega / \omega_1)(1 + \omega / \omega_2)$

**OTC estimate** $f_B = 1/(2\pi \omega_0)$

**Miller:** $Z_1 = Z/(1 - K)$; $Z_2 = Z/(1 - 1/K)$

**MOS cap:**
- $C_{gs} = (2/3)WL_{ox} C_{ox}$; $C_{gd} = WL_{ox} C_{ox}$
- $f_t = f_{Tox} (2\pi C_{gs} + C_{gd})$

**Feedback:**
- $A_f = A/(1 + A\beta)$; $x_1 = (1/(1 + A\beta x_1)$; $dA/dA_f = (1/(1 + A\beta))dA/A$; $\omega_{HF} = \omega_f (1 + A\beta)$; $\omega_{LF} = \omega_L (1 + A\beta)$

**Loop Gain:** $L = -A_f / \omega_{HF}$

**PM:** $Z_{port} = Z_{po} (1 + L_D)/(1 + L_D)$

**Pole Splitting:** $\omega_0^2 = \omega^2 C + \omega^2 (C_1 + C_2)$

**Pole Pair:** $s_1 = (\omega_0 / \omega_0 + \omega_0^2 = 0$; $Q \geq 0.5$ ⇒ real poles; $Q > 1/\sqrt{2}$ ⇒ freq resp peaking

**Power Amps:**
- Class A: $\eta = (1/4)(V_{ds}/I_m) (V_{cc}/V_{cc})$
- Class B: $\eta = (\pi/4)(V_{cc}/V_{cc})$

**2-stage CMOS opamp:**
- $\eta_{cm} = (1/(IC_1R_2C_2))$; $\eta_{ps} = G_m2/C_2$
- $\eta = (1/(C_1(1/G_m2 - R)))$

**SR = 1/C_1; \eta = \eta_{vao}$; will not SR limit if $\eta < \eta_{vao}$

### MOS Transistor

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<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
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<tr>
<td>$V_t$ (V)</td>
<td>0.4</td>
<td>-0.4</td>
</tr>
<tr>
<td>$\mu C_{ox}$ (µA/V$^2$)</td>
<td>240</td>
<td>60</td>
</tr>
<tr>
<td>$\lambda'$ (µm/V)</td>
<td>0.05</td>
<td>-0.05</td>
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<tr>
<td>$C_{ox}$ (fF/µm$^2$)</td>
<td>8.5</td>
<td>8.5</td>
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<tr>
<td>$t_{ox}$ (nm)</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>$L_{ov}$ (µm)</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>$C_{db0}$ / W ($fF$/µm)</td>
<td>0.3</td>
<td>0.3</td>
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