Motherboard PCB
Surface Mount PCB
Surface Mount Package
Chip Manufacturing

Wafer

Single die
Transistors and wires are defined by *masks*.

Cross-section taken along dashed line.
Inverter Cross Section

- Substrate must be tied to GND and n-well to $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps
Six masks

- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal
Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size $f = \text{distance between source and drain}$
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3 \ \mu m$ in $0.6 \ \mu m$ process
Simplified Design Rules

- Conservative rules to get you started

Diagram showing design rules for different layers and features in CMOS VLSI design.
Transistor dimensions specified as Width / Length
- Minimum size is $4\lambda / 2\lambda$, sometimes called 1 unit
- In $f = 0.6\, \mu m$ process, this is $1.2\, \mu m$ wide, $0.6\, \mu m$ long
Inverter (2nd example)
Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 $V_{DD}$ rail at top
- Metal1 GND rail at bottom
- 32 $\lambda$ by 40 $\lambda$
Stick Diagrams

- Stick diagrams help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

(a) \[ V_{DD} \] A \[ GND \] Y

(b) \[ V_{DD} \] A B C \[ GND \] Y

Contact:
- Metal 1
- pdiff
- ndiff
- Polysilicon
A wiring track is the space required for a wire
- 4 $\lambda$ width, 4 $\lambda$ spacing from neighbor = 8 $\lambda$ pitch
- Transistors also consume one wiring track
Well spacing

- Wells must surround transistors by 6 \( \lambda \)
  - Implies 12 \( \lambda \) between opposite transistor flavors
  - Leaves room for one wire track
Example: O3Al

- Sketch a stick diagram for O3Al

\[ Y = \overline{(A + B + C)}D \]