University of Toronto

Final Exam

Date - Apr 28, 2009

Duration: 2.5 hrs

ECE334 — Digital Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Assume the parameters on the parameter sheet (last page) unless otherwise stated (mosfets are from a 0.25um CMOS technology)


3. Only tests written in pen will be considered for a re-mark.

4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

<table>
<thead>
<tr>
<th>Question</th>
<th>Mark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>

Total

Last Name: ______________________

First Name: ____________________

Student #: ____________________

(max grade = 41)
[5] **Question 1:** Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

**T**  **F**  Trench capacitors in DRAM memory arrays are implemented differentially to reduce noise effects.

**T**  **F**  In clock distribution using both grid and H-trees, a grid is used for global clocking while H-trees are used for local clock distribution.

**T**  **F**  Bond wires used in IC packaging connect the bond pad to the lead frame of the package.

**T**  **F**  Although through-hole pin packages result in less PCB density than SMT packages, through-hole pin packages are good for high speed due to less inductance.

**T**  **F**  Phase-locked-loops are commonly used to build clock multipliers through the use of a clock divider in the feedback portion of the PLL.

**T**  **F**  NOR flash memory is generally more dense than NAND flash memory.

**T**  **F**  DRAM memory is normally built in standard CMOS technology.

**T**  **F**  SRAM memory is normally built in standard CMOS technology.

**T**  **F**  When the clock is routed in the same direction as data signals in sequential logic, race conditions are more likely than when the clock is routed in the opposite direction.

**T**  **F**  The purpose of using $V_{DD}/2$ for the trench capacitors back bias is to reduce voltage stress on the trench capacitors.
[6] **Question 2:** Implement the equation $X = (A \cdot \overline{B}) + C$ using CMOS logic assuming that $A, B, C$ are all available as inputs. Assume that the transistors have been sized to give an output resistance of 10k for the worst-case input pattern (in both the high output and low output cases). Find the input pattern, $ABC$, that gives the lowest output resistance when the output is LOW. Also find the value of that resistance, $R_{out}$ when the output is LOW.

\[
\begin{array}{c}
\text{ABC} = \\
\text{R}_{\text{out}} = 
\end{array}
\]
[6] **Question 3:** a) Add the NMOS transistors in the shown 4x4 MOS NAND ROM to store the following data:

<table>
<thead>
<tr>
<th></th>
<th>BL3</th>
<th>BL2</th>
<th>BL1</th>
<th>BL0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

b) What is the main advantage of a MOS NAND ROM over a MOS NOR ROM and why does it occur?
[6] **Question 4:** Find the propagation delay of each inverter \((t_{p1}, t_{p2}, t_{p3})\) in the ring oscillator below (only account for gate capacitance \((WLC_{ox})\) and the shown 5pF capacitance. Also find the oscillation frequency, \(f_{osc}\). Assume n-channel transistors are sized 0.5um/0.25um while p-channel transistors are sized 1.5um/0.25um. (use transistor values on last page)

\[
\begin{align*}
\text{inv 1} & \quad \text{2.5V} \quad \text{inv 2} & \quad \text{2.5V} \quad \text{inv 3} & \quad \text{2.5V} \\
\text{5pF} & \\
\end{align*}
\]

\[
\begin{align*}
t_{p1} &= \\
t_{p2} &= \\
t_{p3} &= \\
f_{osc} &= \\
\end{align*}
\]
[6] Question 5:
   a) Explain the mechanism of Fowler-Nordheim tunneling.

   b) Explain the mechanism of hot carrier injection.

   c) Which mechanism causes more damage to the oxide and therefore limits the number of
      programs/erase cycles of non-volatile memories?

   d) What mechanism is used to erase EPROM memory? (not EEPROM or Flash but only
      EPROM).
[6] **Question 6:** Consider the “d” register shown below.

![Diagram of the register](image)

Assuming that $CK$ and $\overline{CK}$ occur at the same time, and defining the following delays:
- $T_{I_i}$ is the delay through the $i$ \textsuperscript{th} inverter
- $T_{G_i}$ is the delay through the $i$ \textsuperscript{th} T-gate from its clock input to its output
- $T_{Ti}$ is the delay through the $i$ \textsuperscript{th} T-gate from its “data” input to its output

a) Find $T_{\text{setup}}$ in terms of $T_{I_i}$, $T_{G_i}$, and $T_{Ti}$ (be specific in terms of $i$).

\[
T_{\text{setup}} =
\]

b) Find $T_{\text{pcq}}$ in terms of $T_{I_i}$, $T_{G_i}$, and $T_{Ti}$ (be specific in terms of $i$).

\[
T_{\text{pcq}} =
\]
[6] **Question 7:** It is required to transfer a 16 bit bus across 2 asynchronous clock domains. Show how this is achieved using a 2 phase handshake. (Draw block diagrams, clock timing diagrams and words to make it clear).
(blank sheet for scratch calculations)
**Physical Constants:**

\[
\phi_T = \frac{kT}{q} = 26\text{mV (at 300K)}; \quad k = 1.38 \times 10^{-23} \text{ J/K}; \quad T = 300 \text{ K (at 27°C)}; \quad q = 1.6 \times 10^{-19} \text{ C};
\]

\[
e_o = 8.854 \times 10^{-12} \text{ F/m}; \quad k_{ox} = 3.9; \quad \phi_s = 2|\phi_F| = 0.6 \text{V}
\]

**MOS Transistor:** CMOS basic parameters. Channel length = 0.25µm, \(m_j = 0.5\), \(\phi_o = 0.9\text{V}\)

<table>
<thead>
<tr>
<th></th>
<th>(V_{T0}) (V)</th>
<th>(\gamma) (V(^{-0.5}))</th>
<th>(\mu C_{ox}) ((\mu A/V^2))</th>
<th>(\lambda) (V(^{-1}))</th>
<th>(C_{ox}) (fF/(\mu m^2))</th>
<th>(C_o) (fF/(\mu m))</th>
<th>(C_j) (fF/(\mu m^2))</th>
<th>(C_{jsw}) (fF/(\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.4</td>
<td>0.4</td>
<td>120</td>
<td>0.06</td>
<td>6</td>
<td>0.3</td>
<td>2</td>
<td>(see below)</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>0.4</td>
<td>30</td>
<td>0.1</td>
<td>6</td>
<td>0.3</td>
<td>2</td>
<td>(see below)</td>
</tr>
</tbody>
</table>

\(V_{T0}\) is the threshold voltage with zero bulk-source voltage.

\(\gamma\) is used to account for non-zero bulk-source voltage.

\(\mu C_{ox}\) is the transistor current gain parameter.

\(\lambda\) is to account for the transistor finite output impedance (channel length modulation).

\(C_{ox}\) is the gate capacitance per unit area.

\(C_o\) is the gate overlap capacitance per unit length.

\(C_j\) is the drain/source junction capacitance per unit area.

\(C_{jsw}\) is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters except under the gate.

\[
C_{jsw} = 0.3 \text{ fF/\(\mu m\)} \quad \text{for both NMOS and PMOS}
\]

\(C_{jswg}\) is the drain/source junction capacitance per unit length under the gate.

\[
C_{jswg} = 0.15 \text{ fF/\(\mu m\)} \quad \text{for both NMOS and PMOS}
\]