University of Toronto

Term Test 1

Date - Feb 11, 2009

Duration: 7:15pm - 9pm

ECE334 — Digital Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Assume the parameters on the parameter sheet (last page) unless otherwise stated (mosfets are from a 0.25um CMOS technology)


3. Only tests written in pen will be considered for a re-mark.

4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

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<th>Question</th>
<th>Mark</th>
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Last Name: SOLUTIONS

First Name: ______________________

Student #: ______________________  (max grade = 29)
[5] Question 1: Answer the True [T] or False [F] questions below by circling the correct answer. Each correct answer is worth 0.5 marks.

T  F  CMOS microchips typically consist of both PMOS and NMOS transistors

T  F  The “C” in CMOS stands for Complete

T  F  A 2-input NOR gate is designed to have the same worst-case rise and fall times. The best-case fall time is smaller than the best-case rise time in this gate.

T  F  The Body effect causes the threshold of an NMOS transistor to decrease when the \( V_{SB} \) is decreased.

T  F  A chain of identical minimum sized inverters can achieve an overall delay smaller than that of a single minimum sized inverter assuming both drive the same load capacitance.

T  F  A chain of three inverters has a total delay equal to the sum of delays of its individual inverters in the same chain.

T  F  Two NMOS transistors in series with their gates both tied to \( V_{DD} \) can pull the source of the bottom transistor up to but not exceeding \( V_{DD} - 2V_{on} \).

T  F  For the same driving capability, a two-input NAND gate has a smaller layout than a two-input NOR gate.

T  F  The capacitance of a reversed biased junction increases as the reverse bias voltage is increased.

T  F  Velocity saturation is more common in modern technologies as a result of the very thin gate oxide.
Consider the RTL inverter shown above. Using the transistor values on the last page, find values for $R$ and $\left(\frac{W}{L}\right)_n$ such that the logic low output value, $V_{OL} = 0.2\,V$ and the average power dissipated by the inverter, $P_{\text{diss}} = 1\,\text{mW}$ when the output has an equal probability of being either high or low. Ignore any capacitance in this question.

\[
I_{DD\text{-AVE}} = \frac{I_{DD-H} + I_{DD-L}}{2} \quad \text{(AVERAGE } I_{DD})
\]

\[
P_{\text{diss}} = V_{DD} \cdot I_{DD\text{-AVE}} \Rightarrow I_{DD\text{-AVE}} = \frac{1\,\text{mW}}{2\,V} = 0.5\,\text{mA}
\]

\[
I_{DD-H} = 0 \Rightarrow I_{DD-L} = 2 \cdot I_{DD\text{-AVE}} = 1\,\text{mA}
\]

\[
I_{DD-L} = \frac{V_{DD} - V_{OL}}{R} \Rightarrow R = \frac{1.8\,V}{1\,\text{mA}} = 1.8\,k\Omega
\]

\[
I_{ON} = MN_C \cdot \left(\frac{W}{L}\right)_n \left(\left(V_{GS} - V_{TN}\right)V_{OL} - \frac{V_{OL}^2}{2}\right) = I_{DD-L}
\]

\[
\left(\frac{W}{L}\right)_n = \frac{I_{ON}}{(MN_C) \cdot \left(\left(V_{GS} - V_{TN}\right)V_{OL} - \frac{V_{OL}^2}{2}\right)}
\]

\[
= \frac{1\,\text{mA}}{\left(120 \cdot e^{-6}\right) \left[2 - 0.4(0.2) - \frac{0.2^2}{2}\right]}
\]

\[
= 27.8
\]
[6] Question 3:

\[ V_{DD} = 2V \]

\[ \lambda = 0.125 \mu m \]

All transistor lengths are \(2\lambda\)

a) Find the input capacitance of the input C (include overlap capacitance but no Miller effect)

\[
\begin{align*}
W_N &= 6\lambda = 0.75 \mu m \\
L_N &= 2\lambda = 0.25 \mu m \\
W_P &= 8\lambda = 1 \mu m \\
L_P &= 2\lambda = 0.25 \mu m
\end{align*}
\]

\[
C_{ox} = 6 \text{ fF/}\mu\text{m}^2 \\
C_0 = 0.3 \text{ fF/}\mu\text{m}
\]

\[
C_{in-C} = C_{ox} \left[ (1 \times 0.25) + (0.75 \times 0.25) \right] \\
+ C_0 \left[ (2 \times 1) + (2 \times 0.75) \right]
\]

\[
C_{in-C} = 2.625 + 1.05 = 3.68 \text{ fF}
\]
b) Identify on the layout above the drain of the PMOS connected to the output and find the output capacitance due to this drain when the output equals 2V.

\[ C_j = 2 \frac{fF}{(\mu m)^2} \quad \lambda = 0.125 \mu m \]
\[ C_{iss} = 0.3 \frac{fF}{\mu m} \]
\[ C_{issq} = 0.15 \frac{fF}{\mu m} \]
\[ C_{dp} = C_j (8\lambda \times 6\lambda) + C_{iss} (6\lambda + 6\lambda + 8\lambda) + C_{issq} (8\lambda) \]
\[ = 1.5 \text{fF} + 0.75 \text{fF} + 0.15 \text{fF} \]
\[ = 2.4 \text{fF} \]

\[ C_{dp} = 2.4 \text{fF} \]

\[ C_{dp} = 1.33 \text{fF} \]

\[ C_j = \frac{C_j}{\left(1 + \frac{\nu_R}{\Phi_0}\right)^{0.5}} = \frac{C_j}{\left(1 + \frac{2}{0.9}\right)^{0.5}} = \frac{C_j}{1.8} \]

\[ C_{dp} = \frac{2.4 \text{fF}}{1.8} = 1.33 \text{fF} \]
[6] Question 4: Consider a CMOS inverter with $V_{DD} = 2V$, $(W/L)_n = 4$, $(W/L)_p = 8$ and the output capacitance equal to 100fF.

a) Find $t_{df}$.

$$R_{eq} = \frac{2.5}{mnCOX \left(\frac{W}{L}\right) \left(V_{DD} - V_{TN}\right)}$$

$$= 3.25 \, k\Omega$$

$$t_{df} = 1.2 \times R_{eq} \times C_L = (1.2)(3.25k)(100f)$$

$$= 0.39 \, ms$$

\[t_{df} = 0.39 \, ms\]

b) For a step input voltage (with zero rise time) from 0 to $V_{DD}$, sketch the current, $I_{Dn}$, through the NMOS transistor vs time. Label the points on your sketch where the transistor is in cutoff, active and/or triode and show the current and time values at the transitions of the different regions.

\[I_{Dn} = \frac{C}{\Delta V} \frac{\Delta V}{\Delta t}\]

\[I_{Dn, SAT} = C \frac{\Delta V}{\Delta t}\]

**Active**

$$I_{Dn} = \frac{(mnCOX)}{2} \left(\frac{W}{L}\right) \left(V_{DD} - V_{TN}\right) = 614 \, mA$$

Leaves active when $\Delta V = 0.4 \, V \\Rightarrow V_O = V_{DD} - V_{TN}$

$$\Delta t = \frac{C \Delta V}{I_{Dn, SAT}} = \frac{(100fF)(0.4)}{614mA} = 65 \, ps$$
[6] Question 5: For the n portion of a complex CMOS gate shown below, find the slowest case, $t_{df_{\text{slow}}}$ and fastest case, $t_{df_{\text{fast}}}$ corresponding to different input patterns.

$V_{DD} = 2.5\text{V}$

$$t_{df_{\text{slow}}} = 600\text{ps}$$

$$t_{df_{\text{fast}}} = 178\text{ps}$$

**Diagram:**

- p network
- C = 1
- A = 1
- B = 1
- D = 1
- 1um widths shown
- all lengths = 0.25um

$$t_{df_{\text{slow}}} \quad \text{EITHER} \quad C(A+B)=1 \quad \text{OR} \quad D=1$$

$$\frac{1}{\sqrt{\frac{1}{2}}} = \frac{1}{\sqrt{0.5}}$$

$$\text{AND}$$

$$C(A+B)=1 \quad \text{IS SLOWER}$$

$$\text{REAN} = \frac{2.5}{(120 \times 10^{-6})(0.5)(2.5-0.4)}$$

$$= 5k$$

$$t_{df_{\text{slow}}} = (1.2)(5k)(100f) = 600\text{ps}$$

**Diagram:**

- 1um widths shown
- all lengths = 0.25um

$$t_{df_{\text{fast}}} \quad \text{ALL} \quad A=B=C=D=1$$

$$\frac{1}{\sqrt{\frac{1}{2}}} = \frac{1}{\sqrt{0.5}}$$

$$\text{AND}$$

$$\text{REAN} = \frac{2.5}{(120 \times 10^{-6})(\frac{1.67}{0.25})(2.1)}$$

$$= 1.49k$$

$$t_{df_{\text{fast}}} = (1.2)(1.49k)(100f) = 178\text{ps}$$
ECE334F  Digital Electronics  Parameter Sheet

**Physical Constants:**

\[ \phi_T = kT/q = 26 \text{mV (at 300K)}; \quad k = 1.38 \times 10^{-23} \text{ J/K}; \quad T = 300 \text{ K (at 27°C)}; \quad q = 1.6 \times 10^{-19} \text{ C}; \]

\[ \varepsilon_0 = 8.854 \times 10^{-12} \text{F/m}; \quad k_{ox} = 3.9; \quad \phi_s = 2|\phi_F| = 0.6 \text{V} \]

**MOS Transistor:** CMOS basic parameters. Channel length = 0.25\(\mu m\), \(m_j = 0.5\), \(\phi_o = 0.9 \text{V}\)

<table>
<thead>
<tr>
<th></th>
<th>(V_{T0}) (V)</th>
<th>(\gamma) (V(^{0.5}))</th>
<th>(\mu C_{ox}) ((\mu A/\text{V}^2))</th>
<th>(\lambda) (V(^{-1}))</th>
<th>(C_{ox}) (fF/(\mu m^2))</th>
<th>(C_o) (fF/(\mu m))</th>
<th>(C_j) (fF/(\mu m^2))</th>
<th>(C_{jsw}) (fF/(\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.4</td>
<td>0.4</td>
<td>120</td>
<td>0.06</td>
<td>6</td>
<td>0.3</td>
<td>2</td>
<td>(see below)</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>0.4</td>
<td>30</td>
<td>0.1</td>
<td>6</td>
<td>0.3</td>
<td>2</td>
<td>(see below)</td>
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\(V_{T0}\) is the threshold voltage with zero bulk-source voltage.

\(\gamma\) is used to account for non-zero bulk-source voltage.

\(\mu C_{ox}\) is the transistor current gain parameter.

\(\lambda\) is to account for the transistor finite output impedance (channel length modulation).

\(C_{ox}\) is the gate capacitance per unit area.

\(C_o\) is the gate overlap capacitance per unit length.

\(C_j\) is the drain/source junction capacitance per unit area.

\(C_{jsw}\) is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters except under the gate.

\[ C_{jsw} = 0.3 \text{ fF/\(\mu m\)} \text{ for both NMOS and PMOS} \]

\(C_{jswg}\) is the drain/source junction capacitance per unit length under the gate.

\[ C_{jswg} = 0.15 \text{ fF/\(\mu m\)} \text{ for both NMOS and PMOS} \]