University of Toronto

Term Test 2

Date - Mar 17, 2010

Duration: 1.5 hrs

ECE334 — Digital Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Equation sheet is on last page of test.

2. Only tests written in pen will be considered for a re-mark.

3. Calculator type unrestricted

4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

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_Last Name: **SOLUTIONS**_

_First Name: _______________________

(Student #): _______________________

(max grade = 29)
[5] Question 1: Answer the True [T] or False [F] questions below by circling the correct answer. Each correct answer is worth 0.5 marks.

T   F   When creating metal wires on a chip, first silicon dioxide is grown and photoresist is used to etch where wires should exist. Next, aluminum is sprayed on using silicon dioxide as a mask.

T   F   When creating metal wires on a chip, first aluminum is sprayed on the entire micro-chip, then photoresist and silicon oxide is used to mask where wires should exist and the rest is etched off.

T   F   In a self-aligned process, the drain/source junctions are first formed and then the gate is formed above the drain/source junctions so that it is self-aligned.

T   F   The silicon dioxide layer formed under the gate region is grown using wet oxidation instead of dry oxidation.

T   F   Tungsten is used in via and contact holes due to its low resistance.

T   F   P-type silicon is made by doping pure silicon with boron.

T   F   The dynamic power of a digital chip is due to the energy being dissipated across capacitors in the chip.

T   F   In CMOS circuits, to keep all the drain/source diodes reverse biased, the substrate (or bulk) of all NMOS transistors should be tied to $V_{dd}$ while the substrate (or bulk) of all PMOS transistors should be tied to ground.

T   F   A pseudo-NMOS gate with power supplies 0 and $V_{dd}$ has it’s output high level equal to $V_{dd}$ while it’s output low level is a value greater than 0.

T   F   $V_{TH}$ for an inverter is defined to be the input voltage where the inverter’s gain is largest.
[6] Question 2: Consider the following cross-section of a p-well process (not n-well)

![Diagram of a p-well process](image)

a) On the above diagram, label all the "??" signs with the material name (i.e. polysilicon, silicon dioxide, metal, p+, n+, p-, n-, etc.).

b) What is the purpose of the p+ in the p-well and the n+ in the n- substrate?

   These are substrate contacts to bias the p-well and n- substrate. If metal directly connected to lightly doped material, Schottky diode is formed so heavily doped material is used.

c) What is the purpose of field-implants?

   So that the substrate does not invert due to voltages above it.

d) Explain clearly why metal is not used as the gate material in a self-aligned process.

   It would melt during annealing process step. Polysilicon can withstand higher temperatures.
[6] **Question 3:** Find the dynamic power dissipation, $P_{\text{dyn}}$, for the following CMOS circuit assuming the clock is 1GHz, $V_{\text{DD}} = 2.5V$ and the inputs have the following probability values that change on the rising edge of the clock.

$P(A=1) = 0.5$, $P(B=1) = 0.4$, $P(C=1) = 0.7$

\[ P_{\text{dyn}} = 23.4 \text{ mW} \]

\[ P_{\text{dy}n-1} = P_{1 \rightarrow 0} + C_1 V_{00}^2 \]

\[ P_{x=1} = P_{A=0} P_{B=0} = (0.5)(0.6) = 0.3 \]

\[ P_{x=0} = 1 - P_{x=1} = 0.7 \]

\[ P_{x(1 \rightarrow 0)} = (0.3)(0.7) = 0.21 \]

\[ P_{0y\bar{n}-1} = (0.21)(1e9)(5e-15)(2.5)^2 = 6.6 \text{ mW} \]

\[ P_{\text{dy}n-2} = P_{1 \rightarrow 0} + C_2 V_{00}^2 = (0.3)(0.7)(1e9)(5e-15)(2.5)^2 \]

\[ = 6.6 \text{ mW} \]

\[ P_{0y\bar{n}-3} = P_{1 \rightarrow 0} + C_3 V_{00}^2 \]

\[ P_{\bar{z}=0} = P_{x=1} P_{y=0} = (0.3)(0.3) = 0.09 \]

\[ P_{\bar{z}=1} = 1 - P_{\bar{z}=0} = 0.91 \]

\[ P_{0y\bar{n}-3} = (0.91)(0.09)(1e9)(2e-15)(2.5)^2 \]

\[ = 10.2 \text{ mW} \]

\[ P_{\text{dy}n} = P_{0y\bar{n}-1} + P_{0y\bar{n}-2} + P_{0y\bar{n}-3} = 6.6 + 6.6 + 10.2 \]

\[ = 23.4 \text{ mW} \]
**[6] Question 4:** Consider a metal 1 (first layer of metal) aluminum wire that is 0.8 μm above the substrate, is 0.5 μm in height and has a width of 0.25 μm and has a length of 5 mm. Recall that the resistivity of aluminum is 2.8 μΩ cm.

a) Find the resistance per μm, \( R_w \), and the capacitance per μm, \( C_w \).

\[
R_w = \frac{R_0}{t} = \frac{2.8 \times 10^{-8} \Omega \cdot m}{0.5 \times 10^{-6} \ m} = 0.056 \ \Omega/\mu m
\]

\[
R_w = R_0 \frac{1 \ \mu m}{0.25 \ \mu m} = 4 \ R_0 = 0.224 \ \Omega/\mu m
\]

\[
C_w = \varepsilon_0 [((\frac{W}{h}) + 0.77 + 1.06 (\frac{W}{h})^{0.25} + 1.06 (\frac{t}{h})^{0.5}] \\
= 3.9 \times 8.85 \times 10^{-12} \ [2.71] \\
= 9.7 \ \text{pF/μm} = 0.094 \ \text{pF/μm}
\]

b) Estimate the delay, \( t_d \), of this wire assuming the delay is 1.2τ.

\[
\tau = \frac{R_w}{2} = \frac{(0.224)(5000)(0.094)(5000)}{2} \\
= \frac{(1120)(470 \ \text{pF})}{2} = 263 \ \text{ps}
\]

\[
t_d = 1.2 \tau = 316 \ \text{ps}
\]

b) Estimate the delay of this wire if the width is increased to 1 μm and other parameters are unchanged.

\[
W_2 = 4W \Rightarrow R_2 = \frac{R}{4} = 280 \ \Omega
\]

\[
C_{w2} = \varepsilon_0 [((\frac{W}{h}) + 0.77 + 1.06 (\frac{W}{h})^{0.25} + 1.06 (\frac{t}{h})^{0.5}] \\
= \varepsilon_0 [3.98] = 0.138 \ \text{pF/μm}
\]

\[
C_2 = C_{w2}(5000) = 690 \ \text{pF}
\]

\[
t_{d2} = 1.2 \frac{R_2 C_2}{2} = 116 \ \text{ps}
\]
[6] **Question 5:** It is desired to drive a 1pF capacitive load given that a minimum size inverter has a gate capacitance of 4fF and it's inherent delay is 15ps.

a) Find the delay if a single inverter is used.

\[
    t_d = T_{\text{inv}} \cdot \frac{C_{\text{out}}}{C_{\text{in}}} = (15\text{ps}) \left( \frac{1\text{pF}}{4\text{fF}} \right)
    \]

\[
    = 3.75\text{ns}
    \]

b) Find the delay if an inverter chain is used where a fanout factor of 4 is used for inverter sizing.

\[
    t_d = 3 \cdot \tau_{\text{inv}} (4) + \tau_{\text{inv}} \left( \frac{1\text{pF}}{256\text{fF}} \right) = 12 \cdot \tau_{\text{inv}} + 3.9 \cdot \tau_{\text{inv}}
    \]

\[
    = 15.9 \cdot \tau_{\text{inv}} = (15.9)(15\text{ps}) = 238\text{ ps}
    \]

c) Explain why a fanout factor of 4 is generally used for inverter sizing in an inverter chain instead of a factor of \( e \) which was derived in class to be optimum. (hint: what was overlooked in the class derivation?)

**Class Derivation Did Not Account For Output Capacitance of An Inverter Which Roughly Scales With Size Of Inverter. Also Factor Of 4 Is Simple To Do.**
ECE334  

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Equation Sheet

Constants: \( k = 1.38 \times 10^{-23} \text{JK}^{-1} \); \( q = 1.602 \times 10^{-19} \text{C} \); \( V_T = kT/q = 26 \text{mV at } 300 \degree \text{K} \);  
\( e_0 = 8.854 \times 10^{-12} \text{F/m} \); \( \kappa_{ox} = 3.9 \); \( \text{cap} \): \( C_{ox} = (\kappa_{ox} e_0)/\varepsilon_{ox} \); \( C_j = C_{ps}/(1 + V_R/\Phi_0) \);  

NMOS:  
\( \beta_n = \mu_n C_{ox} (W/L) \); \( V_{th} > 0 \); \( V_{GS} \geq 0 \); (triode) \( I_D = \beta_n (V_{GS} - V_{th}) V_{DS} (1 - V_{DS}/2) \); (active) \( I_D = 0.5 \beta_n (V_{GS} - V_{th})^2 \);  

(triode) \( V_{DS} \leq (V_{GS} - V_{th}) \); (active) \( V_{DS} \geq (V_{GS} - V_{th}) \); \( V_{in} = V_{in0} + \gamma (\sqrt{2} + \Phi_1 - \sqrt{2}) \);  

(subthreshold) \( I_D = I_{DS0} e^{(V_{GS} - V_{th})/(\Phi_0/2)} (1 - e^{-V_{DS}/V_T}) \);  

PMOS:  
\( \beta_p = \mu_p C_{ox} (W/L) \); \( V_{th} < 0 \); \( V_{GS} \leq 0 \); (triode) \( I_D = \beta_p (V_{GS} - V_{th}) V_{DS} (1 - V_{DS}/2) \); (active) \( I_D = 0.5 \beta_p (V_{GS} - V_{th})^2 \);  

(triode) \( V_{DS} \geq (V_{GS} - V_{th}) \); (active) \( V_{DS} \leq (V_{GS} - V_{th}) \);  

Simple cap model: \( C_e = C_{ox} W/L \); if \( L_{min} \leq C_{pe} \leq C_{ox} W/L \); \( C_e = C_{pe} W \); \( C_d = C_{sd} W \);  

CMOS inverter: \( V_{TH} = (V_{DD} + V_{th})/(1 + r) \); \( r = \sqrt{(V_{th}/W/L)_p}(V_{DD} - V_{th})/(1 + \sqrt{(V_{th}/W/L)_n}) \);  

RC delay est: \( t_{dr} = 1.2 t \); \( \tau = R \sqrt{C} \); \( R_{eq} = 2.5/\mu N C_{ox} (W/L) (V_{DD} - V_{th}) \); \( R_{eq} = 2.5/\mu N C_{ox} (W/L) (V_{DD} + V_{th}) \);  

\( (W/L)_{opt} = \sqrt{\mu_n/\mu_p} \) Unit delay est: \( t_{dd}/(t_{in}) = (C_{L2}/C_{L1}) \times (W/L)_{th}/(W/L)_{min} \)  

Min delay: \( t_{del} = t_{inv}(C_{out}/C_{in}) \); \( \text{total delay} = N f_{inv} \); \( f = C_{out}/C_{in} \); usually \( f = 4 \)  

Power diss: \( P_{dyn} = P_1 + \theta L V_{DD} \); \( P_{peak} = 0.5 P_1 + \theta L V_{DD}/\sqrt{2} \); \( t_{peak} = 0.5 \beta_n (V_{TH} - V_{th})^2 \);  

Elmore Delay: \( \tau = \sum C \tanh(k) \); dist RC, \( \tau = RC/2 \);  

Interconnect: \( R = \rho L \); \( R_{in} = \rho / t \); \( C = (e_{ox} W L) / t \); \( C = e_{ox} (w + 0.77 + 1.06(w/h)^{0.23})^2 + 1.06(t/h)^{0.5} \)