**USE OF COMPOUND DEVICES**

**BJT**

**CURRENT GAIN** \( \beta = \frac{I_C}{I_B} \)

(BJTs in the active region)

**TO INCREASE CURRENT GAIN**

**USE A DARLINGTON CONFIGURATION**

\( \beta \approx \beta_1 \beta_2 \)

\( V_{BE} = V_{BE1} + V_{BE2} \)

**IF USED AS SHOWN ABOVE Q_1 RIASED WITH ONLY I_B2 (MAY BE TOO SMALL A BIAS CURRENT)**
Usually add bias current to Q1. Also helps turn off Q2 if Q1 turned off.

For PNP, often use NPN together with PNP to improve PNP

NPN usually have better performance than PNP

(Higher β and higher ft)

Especially if PNP built as lateral device rather than vertical device.
\[ I_F = \beta N \cdot I_{SP} \]

Where \( I_{SP} \) is the collector current of PNP \( Q_1 \).

\[ I_C = \beta N \cdot I_{SP} \cdot e^{-\frac{\Delta V_{EB}}{V_T}} \]

**Note:** There is a feedback loop around \( Q_1 \) and \( Q_2 \) here so stability must be considered.
USE IN AN OUTPUT STAGE

\[ \text{MIN } V_o \Rightarrow V_{o-min} + V_{EB3} \]

(SIMILAR TO PNP ALONE)

\[ \text{MAX } V_o = V_{CC} - V_{Bias} - V_{BE1} - V_{BE2} \]

(EXTRA VBE DROP)
CMOS

SUPER SOURCE FOLLOWER

\[ V_{DD} \]

\[ V_{I2} \]

\[ V_{I1} \]

\[ M_1 \]

\[ M_2 \]

\[ P_{MOS} \]

\[ N_{MOS} \]

COMBINATION

SMALL-SIGNAL

\[ q_{m1}N_{q1} \]

\[ r_{01} \]

\[ r_{02} \]
IMPEANCE SEEN TO LEFT OF BREAK \( \Rightarrow \)

\[
\frac{v_{q22}}{v_t} = (1 + qm_1 R_{01}) \approx qm_1 R_{01}
\]

\[
\frac{v_r}{v_{q22}} = -qm_2 R_{02}
\]

\[
L = \frac{v_r}{v_t} \approx qm_1 qm_2 R_{01} R_{02}
\]

\[
R_{p0} = R_{02}
\]

\[
R_{out} = R_{p0} \left[ \frac{1 + L_5}{1 + L_0} \right]
\]

\[
L_5 = 0 \quad L_0 = L
\]

\[
R_{out} = \frac{R_{02}}{qm_1 qm_2 R_{01} R_{02}} = \frac{1}{qm_2 (qm_1 R_{01})}
\]

\[
R_{out} \ll \frac{1}{qm_2}
\]