University of Toronto

Term Test 1

Date - Feb 10, 2014 (9:10am to 10:00am)

Duration: 50 min

ECE354 — Analog Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Equation sheet is on last page of test.

2. Unless otherwise stated, use transistor parameters on equation sheet.

3. Non-programmable calculator allowed; No other aids allowed

4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

<table>
<thead>
<tr>
<th>Question</th>
<th>Mark</th>
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Last Name: _______________________

First Name: _______________________

Student #: _______________________

(max grade = 24)
[6] **Question 1:** Assume an nmos transistor (based on the 0.18um parameters given on the equation sheet) with $W = 4 \mu m$, $L = 0.5 \mu m$ is biased with $V_{ov} = 0.4 V$ and $V_{DS} = 1 V$.

a) Find the $r_o$ for this device.

b) If $V_{DS}$ is increased by 0.5V, what is the corresponding change in $I_D$?

c) If a cascode current mirror makes use of two nmos transistors biased with the same current as in a), find $r_o$ and the change in $I_D$ for a 0.5V change in the mirror output voltage. (assume both transistors remain in the active region).
[6] **Question 2:** Given 2 current sources from $V_{DD}$ where each are $10\mu A$, design a wide-swing cascode current-mirror circuit (including bias voltage generation) that gives an nmos output of $40\mu A$. Assume all transistor lengths are $0.18\mu m$ and the nmos current mirror output transistors have $W = 4\mu m$. Show the widths of all transistors on your schematic. (Hint: there should be 5 nmos transistors and 2 current sources on your schematic).

\[ \text{a) Find the small-signal short-circuit current gain, } \frac{i_{sc}}{v_i} \text{ assuming all } r_o \rightarrow \infty. \]

\[ g_{m1} = 1 \text{mA/V} \]
\[ g_{m2} = 0.5 \text{mA/V} \]
\[ g_{m3} = 1 \text{mA/V} \]

\[ \frac{i_{sc}}{v_i} = \frac{1}{20k} \]

\[ b) \text{Find the small-signal gain, } i_{sc}/v_i \text{ assuming } r_o = 20k \text{ for all transistors (current source is still ideal) and make no approximations. Compare this result with that found in part a) in terms of percentage error.} \]
[6] Question 4: Consider the circuit shown below.

![Circuit Diagram]

- $V_{DD}$
- $R_D = 10k$
- $I_C = \frac{0.5\text{mA}}{V}$
- $g_m = 0.5\text{mA/V}$
- $C_L = 1\text{pF}$
- $C_3 = 1\text{pF}$
- $R_L = 40k$
- $R_G = 1M$
- $R_S = 10k$
- $V_s$
- $v_o$
- Ignore $r_0$
- Current source output impedance = 10k

a) Given that the low frequency poles should occur at 0.1Hz, 1Hz and 100Hz, and it is desired to minimize capacitor sizes, find the value of $C_1$ (explain your reasoning).

$$C_1 = \text{[Blank]}$$

b) Estimate the gain for a 10Hz input signal (explain your reasoning).
Analog Electronics

Constants: $k = 1.38 \times 10^{-23}$ J K$^{-1}$; $q = 1.602 \times 10^{-19}$ C; $V_T = kT/q = 26$ mV at 300 °C ; $e_0 = 8.854 \times 10^{-12}$ F/m; $k_{ox} = 3.9; C_{ox} = (k_{ox}e_0)/l_{ox}$

NMOS: $k_m = k_mC_{ox}(W/L)$; $V_{th} > 0$; $V_{DS} \geq 0$; $V_{GS} = V_{th}$

PMOS: $K_p = K_pC_{ox}(W/L)$; $V_{ip} < 0$; $V_{DS} \geq 0$; $V_{GS} = V_{th}$

MOS Transistor:

<table>
<thead>
<tr>
<th>$V_t$ (V)</th>
<th>$\mu C_{ox}$ ($\mu A/V^2$)</th>
<th>$\lambda'$ ($\mu m/V$)</th>
<th>$C_{ox}$ (pF/µm$^2$)</th>
<th>$t_{ox}$ (nm)</th>
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</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.4</td>
<td>240</td>
<td>0.05</td>
<td>8.5</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>60</td>
<td>-0.05</td>
<td>8.5</td>
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