8.1 For an NMOS differential pair with a common-mode voltage $V_{CM}$ applied, as shown in Fig. 8.2, let $V_{DD} = V_{SS} = 1.0 \text{ V}$, $k'_n = 0.4 \text{ mA/V}^2$, $(W/L)_{Q_1} = 12.5$, $V_{gs} = 0.5 \text{ V}$, $I = 0.2 \text{ mA}$, $R_D = 10 \text{ k\Omega}$, and neglect channel-length modulation.

(a) Find $V_{GP}$ and $V_{GS}$ for each transistor.
(b) For $V_{CM} = 0$, find $V_{S_1}, I_{D_1}, I_{D_2}, V_{D_1}$, and $V_{D_2}$.
(c) Repeat (b) for $V_{CM} = +0.3 \text{ V}$.
(d) Repeat (b) for $V_{CM} = -0.1 \text{ V}$.
(e) What is the highest value of $V_{CM}$ for which $Q_1$ and $Q_2$ remain in saturation?
(f) If current source $I$ requires a minimum voltage of 0.2 V to operate properly, what is the lowest value allowed for $V_S$ and hence for $V_{CM}$?

8.2 For the PMOS differential amplifier shown in Fig. P8.2 let $V_p = -0.8 \text{ V}$ and $k'_p W/L = 4 \text{ mA/V}^2$. Neglect channel-length modulation.

(a) For $v_{G1} = v_{G2} = 0 \text{ V}$, find $V_{GP}$ and $V_{GS}$ for each of $Q_1$ and $Q_2$. Also find $V_{S_1}, V_{D_1}$, and $V_{D_2}$.
(b) If the current source requires a minimum voltage of 0.5 V, find the input common-mode range.

8.3 For the differential amplifier specified in Problem 8.1 let $v_{G1} = 0$ and $v_{G2} = v_{ap}$. Find the value of $v_{ap}$ that corresponds to each of the following situations:

(a) $I_{D_1} = I_{D_2} = 0.1 \text{ mA}$; (b) $I_{D_1} = 0.15 \text{ mA}$ and $I_{D_2} = 0.05 \text{ mA}$; (c) $I_{D_1} = 0.2 \text{ mA}$ and $I_{D_2} = 0$ ($Q_2$ just cuts off); (d) $I_{D_1} = 0.05 \text{ mA}$ and $I_{D_2} = 0.15 \text{ mA}$; (e) $I_{D_1} = 0 \text{ mA}$ ($Q_1$ just cuts off) and $I_{D_2} = 0.2 \text{ mA}$. For each case, find $V_{S_1}, V_{D_1}, V_{D_2}$, and $(v_{D2} - v_{D1})$.

D 8.6 Design the circuit in Fig. P8.6 to obtain a dc voltage of +0.2V at each of the drains of $Q_1$ and $Q_2$ when $v_{G1} = v_{G2} = 0 \text{ V}$. Operate all transistors at $V_{DD} = 0.2 \text{ V}$ and assume that for the process technology in which the circuit is fabricated, $V_{th} = 0.5 \text{ V}$ and $\mu_n C_{ox} = 250 \mu\text{A/V}^2$. Neglect channel-length modulation. Determine the values of $R, R_D$, and the $W/L$ ratios of $Q_1, Q_2, Q_3$, and $Q_4$. What is the input common-mode voltage range for your design?
8.9 An NMOS differential amplifier utilizes a bias current of 400 μA. The devices have $V_t = 0.5$ V, $W = 20$ μm, and $L = 0.5$ μm, in a technology for which $\mu_n C_{ox} = 200$ μA/V². Find $V_{GS}$ and $g_m$ in the equilibrium state. Also find the value of $v_{id}$ for full-current switching. To what value should the bias current be changed in order to double the value of $v_{id}$ for full-current switching?

D 8.10 Design the MOS differential amplifier of Fig. 8.5 to operate at $V_{OV} = 0.25$ V and to provide a transconductance $g_m$ of 1 mA/V. Specify the $W/L$ ratios and the bias current. The technology available provides $V_t = 0.8$ V and $\mu_n C_{ox} = 100$ μA/V².

D 8.14 It is required to design an NMOS differential amplifier to operate with a differential input voltage that can be as high as 0.1 V while keeping the nonlinear term under the square root in Eq. (8.23) to a maximum of 0.05. A transconductance $g_m$ of 1 mA/V is needed. Find the required values of $V_{OV}$, $I$, and $W/L$. Assume that the technology available has $\mu_n C_{ox} = 200$ μA/V². What differential gain $A_d$ results when $R_D = 10$ kΩ? Assume $\lambda = 0$. What is the resulting output signal corresponding to $v_{id}$ at its maximum value?

D 8.16 Design a MOS differential amplifier to operate from ±1-V supplies and dissipate no more than 2 mW in its equilibrium state. Select the value of $V_{OV}$ so that the value of $v_{id}$ that steers the current from one side of the pair to the other is 0.4 V. The differential voltage gain $A_d$ is to be 5 V/V. Assume $k_t = 400$ μA/V² and neglect the Early effect. Specify the required values of $I$, $R_D$, and $W/L$.

8.21 Find the differential half-circuit for the differential amplifier shown in Fig. P8.21 and use it to derive an expression for the differential gain $A_d = \frac{v_{od}}{v_{id}}$ in terms of $g_m$, $R_D$, and $R_s$. Neglect the Early effect. What is the gain with $R_s = 0$? What is the value of $R_s$ (in terms of $1/g_m$) that reduces the gain to half this value?
8.25 A design error has resulted in a gross mismatch in the circuit of Fig. P8.25. Specifically, $Q_2$ has twice the $W/L$ ratio of $Q_1$. If $v_{ad}$ is a small sine-wave signal, find:

(a) $I_{Q1}$ and $I_{Q2}$.
(b) $V_{OE}$ for each of $Q_1$ and $Q_2$.
(c) The differential gain $A_d$ in terms of $R_D$, $I$, and $V_{OE}$.

8.28 For the differential amplifier shown in Fig. P8.2, let $Q_1$ and $Q_2$ have $k''_n(W/L) = 4 \text{ mA/V}^2$, and assume that the bias current source has an output resistance of 30 kΩ. Find $|V_{OVP}|$, $g_m$, $|A_d|$, $|A_{cm}|$, and the CMRR (in dB) obtained with the output taken differentially. The drain resistances are known to have a mismatch of 2%.

8.73 An NMOS differential pair operating at a bias current $I$ of 100 μA uses transistors for which $k''_n = 250 \mu\text{A/V}^2$ and $W/L = 10$. Find the three components of input offset voltage under the conditions that $\Delta R_D / R_D = 5\%$, $\Delta(W/L)/(W/L) = 5\%$, and $\Delta V_t = 5 \text{ mV}$. In the worst case, what might the total offset be? For the usual case of the three effects being independent, what is the offset likely to be?

8.91 An active-loaded NMOS differential amplifier operates with a bias current $I$ of 100 μA. The NMOS transistors are operated at $V_{OVP} = 0.2$ V and the PMOS devices at $|V_{OVP}| = 0.3$ V. The Early voltages are 20 V for the NMOS and 12 V for the PMOS transistors. Find $G_m$, $R_o$, and $A_d$. For what value of load resistance is the gain reduced by a factor of 2?

8.111 Consider the input stage of the CMOS op amp in Fig. 8.41 with both inputs grounded. Assume that the two sides of the input stage are perfectly matched except that the threshold voltages of $Q_3$ and $Q_4$ have a mismatch $\Delta V_t$. Show that a current $g_m \Delta V_t$ appears at the output of the first stage. What is the corresponding input offset voltage? Given parameters below and $\Delta V_t = 2 \text{ mV}$.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>$Q_3$</th>
<th>$Q_4$</th>
<th>$Q_5$</th>
<th>$Q_6$</th>
<th>$Q_7$</th>
<th>$Q_8$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W/L$</td>
<td>20/8</td>
<td>20/8</td>
<td>5/6</td>
<td>5/6</td>
<td>5/6</td>
<td>40/8</td>
<td>40/8</td>
<td>40/8</td>
</tr>
</tbody>
</table>

Let $I_{REF} = 90 \mu\text{A}$, $V_p = 0.7$ V, $V_n = -0.8$ V, $\mu C_{ox} = 160 \mu\text{A/V}^2$, $\mu C_{ox} = 40 \mu\text{A/V}^2$. Neglect Early voltage.