A 100MHz Partial Analog Adaptive Equalizer for use in Wired Data Transmission

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ABSTRACT

This paper describes a 3 volt partial analog adaptive equalizer that is intended to be used with a digital decision feedback equalizer (DFE). The analog filter was realized in a 0.5um CMOS process and has a bandwidth of 100MHz while consuming 23mW of power. It has one tuning parameter and eliminates precursor intersymbol interference in a 311 Mbits/second system encoded as a 4-level PAM signal over 0 to 300 meters of coaxial cable.

1. Introduction

The transmission channel considered is a coaxial cable and is modeled as a transmission line having a transfer-function described by an exponential function [1]

\[ C(s) = e^{-La_o s} \]  

(1)

where \( L \) is the cable length and \( a_o \) is the cable constant. Due to the transfer-function of the cable, a transmitted data signal experiences phase and magnitude variations that result in intersymbol interference (ISI) [2]. The presence of ISI causes the eye diagram of the receive signal, \( r(t) \), to close, and the original transmitted symbols cannot be correctly recovered. To combat ISI, equalization is required at the receiver.

Traditionally, an analog adaptive equalizer is implemented as a linear equalizer which removes all ISI as shown in Figure 1(a). One difficulty with this equalizer arrangement is the well-known problem of noise enhancement. Specifically, high-frequency noise within the signal bandwidth is enhanced due to the high frequency gain of the equalizer which is used to combat the attenuation of the cable. Another difficulty is the challenge of fully removing the ISI due to variations in the cable channel and possible dc offsets.

As an alternative, the equalization system shown in Figure 1(b) can be used and is the subject of this paper. It contains a partial analog equalizer followed by an analog-to-digital converter and a DFE. In this paper, the analog equalizer is designed in such a way that it eliminates precursor ISI and most of the postcursor ISI. Unlike the traditional analog equalizer, this partial analog equalizer allows some residual postcursor ISI to remain and therefore requires less high-frequency boost. As a result, this partial analog equalizer has less noise enhancement than the traditional analog equalizer.

The residual postcursor ISI will be corrected by the DFE. The DFE operates on the slicer output and does not cause any noise enhancement. Also, it should be noted that the multipliers in the DFE are simple to build because their input is represented by a small number of bits as opposed to a digital feedforward equalizer. In addition, a few taps of adaptive DFE which clear up residual postcursor ISI allows a great deal of flexibility in designing the partial analog equalizer as well as allowing the system to track a wider channel variation and cancel dc offset. Also, the order of the partial analog equalizer is lower than that of the traditional analog equalizer because the traditional analog equalizer has to remove all ISI, while the partial analog equalizer does not. Finally, the ADC can have a lower resolution (i.e. a fewer number of bits) than in a pure digital equalization since the signal has been partially equalized.

![Figure 1 Equalization Systems](image-url)
2. Partial Analog Equalizer Design

As discussed above, we require an analog equalizer to remove precursor ISI such that a simple DFE can be used to remove remaining postcursor ISI. Since this filter is intended for use in a 4-level PAM system operating at 311 Mbits/second, the required bandwidth of the analog equalizer is roughly 100 MHz.

Figure 2 shows the magnitude response of the nominal analog equalizer which is used to provide partial equalization for the maximum cable length of 300 meters. The impulse response of the system consisting of an NRZ transmit filter, a 300-m cable and the nominal analog equalizer is shown in Figure 3. Note that there is no precursor ISI, and the postcursor ISI can be corrected with only a 3-tap DFE.

The block diagram for this analog equalizer is shown in Figure 4 and consists of a second-order bandpass filter together with a unity-gain feedforward path. The gain of the bandpass filter, \( k_{BP} \), can be varied to provide equalization for different cable lengths. As the cable length is longer, \( k_{BP} \) is tuned to a larger value to provide more boost. On the other hand, when the cable length is close to 0 meters, no equalization is needed. In this case, \( k_{BP} \) is tuned to zero to turn off the bandpass section such that only the unity-gain feedforward path remains. It should be noted that this structure is similar to other cable equalizers but with reduced filter order and reduced high frequency gain [3][4].

3. Circuit Description

The top-level schematic of the analog equalizer is shown in Figure 5. It is constructed from transconductors and Miller integrators.

The transconductor cells in the unity-gain feedforward path, \( G_m \) cells E and F, have small \( G_m \). Hence, they are built using the conventional transconductors as shown in Figure 6(a). However, those in the bandpass filter, \( G_m \) cells A, B, C and D, have large \( G_m \), and linear transconductors with feedback are used [5][6][7]. The schematic of the linear transconductor is shown in Figure 6(c). Miller integrators, the schematic of which is
depicted in Figure 6(b), are employed because they allow the Gm-cells to have low output impedance and reduce the nonlinear parasitic capacitances at the output nodes of the Gm-cells [8][9].

The gain of the bandpass filter is tuned by varying the transconductance of Gm-cell D. This is achieved by using a digital control word to switch in and out an array of triode transistors that replaces M3 in Figure 6(c). The widths of the triode transistors are scaled in powers of two so that digital control is acheived.

While the gain of the bandpass filter is varied to provide equalization for different cable lengths, the center frequency is kept constant. A frequency tuning circuit based on charge balancing is used to set a single time-constant [10]. Figure 7 shows a simplified schematic of the tuning circuit. The control voltage, V_C, generated by the tuning circuit is used to set the gate voltage of the triode transistor, M3, in all the Gm-cells inside the analog equalizer.

4. TEST RESULTS

The analog equalizer and tuning circuit were realized using a 0.5μm CMOS process. The layout is shown in Figure 8 and the core circuitry occupies an area of 0.6 mm². The circuit operates from a 3V power supply and consumes 23mW excluding output buffers.

An intermodulation test on the analog equalizer was performed while placing the center frequency of the bandpass filter at 100MHz. With input sinusoids at 40MHz and 80MHz, the third-order distortion product at 120MHz dominates and was seen to be -29dB below the applied signals when the output amplitude was at 0.6 Vpp. Although, this distortion level is not impressive, it satisfies the requirements for this application.

To see the equalization performance of this filter, a repeated sequence of short impulses was applied to an NRZ transmit filter, a 300m Belden 8281 coaxial cable and the partial analog equalizer. Figure 9 shows the
resulting impulse response. Note that there is no precursor ISI and the postcursor ISI can be corrected by a 3-tap DFE. Although the shape of the impulse response is different from the simulated result (shown in Figure 3) due to process variations, the postcursor ISI can still be removed by a 3-tap DFE. This further illustrates that the addition of a few taps of adaptive DFE results in an equalization system that is more tolerant to variations in the transfer-function of the partial analog equalizer.

An eye diagram of the partial analog equalizer output is shown in Figure 10 with the input driven by a 2-level signal at a rate of 155 MSymbols/second (a 4-level signal was not possible due to test equipment limitations). Note that the eye is only partially opened as expected and will be corrected by a DFE as discussed earlier.

5. CONCLUSION

Design details and experimental results were presented for a partial analog adaptive equalizer. It is intended for use in an equalization system where the analog equalizer removes precursor and most of the postcursor ISI. A 3-tap adaptive DFE can be used to remove the residual postcursor ISI. A few taps of adaptive DFE simplifies the design of the analog equalizer and allows the equalization system to be more tolerable to changes in the transfer-function of the analog equalizer as well as channel variations.

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7. REFERENCES


