SIGMA-DELTA BASED IIR FILTERS

D.A. Johns and D.M. Lewis
Dept. of Electrical Engineering,
University of Toronto,
Toronto, Ontario CANADA M5S 1A4

Abstract

A design methodology for realizing IIR filters on sigma-delta modulated signals is proposed. It is shown that only 3N adders together with minor logic are required to implement an Nth order filter. With the use of examples, it is also shown that a linear noise analysis gives an excellent prediction of noise performance over the frequency band of interest. This type of filtering should prove useful in VLSI technologies where interfaces to analog signals are required.

Introduction

The use of sigma-delta (Σ-Δ) modulation has been shown to be an effective method for building high resolution analog-to-digital (A/D) and digital-to-analog (D/A) converters [1,2]. Thus, performing signal processing on Σ-Δ modulated signals is desirable as this type of processing could be integrated with other systems in VLSI where interfaces to analog signals are required. Towards this goal, a recent publication describes a method of realizing finite-impulse-response (FIR) filters operating on such signals [3], however, there is presently no method for realizing equivalent infinite-impulse-response (IIR) filters. The purpose of this paper is to propose such an IIR filter design methodology. We will show that to realize an Nth order filter using second-order Σ-Δ modulators, only 3N adders are required together with some minor logic. This IIR approach should result in smaller VLSI implementations than their FIR counterparts in applications where the oversampling ratio is high and a low-order FIR response can replace a high-order FIR response. It should be mentioned here that a technique for realizing IIR filters operating on delta modulated signals has been previously published [4], however, since most A/D and D/A implementations are implemented as sigma-delta realizations, there is a strong motivation to extend that work for sigma-delta modulated signals.

Before proceeding, some terms relating to oversampling need to be defined. Throughout this paper, we shall assume the baseband frequency of interest to be from 0 to \( f_s \). The oversampling ratio, OSR, is defined to be the ratio of the sampling frequency, \( f_s \), to the Nyquist frequency, \( 2f_s \). Specifically,

\[
\text{OSR} = \frac{f_s}{2f_s}
\]

For simplicity, throughout this paper we shall normalize \( f_s \) to unity.

Design Approach

The method proposed here makes use of standard IIR filter structures except that filter states exist both multi-bit and one-bit signals. The one-bit signal is obtained by modulating the multi-bit signal using a fully digital Σ-Δ modulator. A digital second-order Σ-Δ modulator is shown in figure 1 where the input and output signals are multi-bit and one-bit, respectively [3]. The block \( q(*) \) is a one-bit quantizer implemented by simply taking the most significant bit. The implementation complexity of this modulator can be simplified to two adders if 2's complement arithmetic is used. This low complexity is due to the first and third adders being realized by simply changing the sign-bit of the multi-bit signal because the value added is either the positive or negative maximum value. The transfer-function of this modulator within the frequency of interest is simply \( z^{-1} \) (ie. a single delay stage at the oversampled rate). This fact is used in the design of the IIR filters to be described.

To illustrate the proposed approach, consider first the circuit shown in figure 2(a). A one-bit input signal, \( u(n) \), operating at the oversampled rate is multiplied by a multi-bit fixed coefficient, \( a_1 \), and the resulting multi-bit signal, \( y(n+1) \), is applied to a digital Σ-Δ modulator giving the output one-bit signal, \( \hat{y}(n) \). Over the frequency of interest, it is clear that this circuit behaves as an attenuator circuit, although the modulator does add extra noise. The modulator in figure 2(a) can be modelled as a single delay plus some additive noise, \( e(n) \), as shown in figure 2(b). The spectral density of this noise source, \( e(n) \), is described in the Noise Performance section. In terms of hardware complexity, since \( u(n) \) is a one-bit signal, the multipliers can be efficiently realized as a 2-input multiplexor (simply changing the sign-bit is not sufficient as 2's-complement arithmetic is assumed in order to realize efficient adders). This multiplexor approach results in the 1xk multiplexor requiring about 4k transistors in CMOS technology for a k-bit coefficient. For comparison, a kxk multiplexor requires about 20k^2 transistors. All multipliers shown in this paper are of this multiplexor type - a critical requirement since they must operate at the oversampled rate.

![Double loop sigma-delta modulator](image1)

Fig. 1. Double loop sigma-delta modulator. \( q(*) \) denotes the one-bit nonlinear quantization function.

\[
u(n) \xrightarrow{\Sigma-\Delta \text{ Mod}} y(n+1) \xrightarrow{\hat{y}(n)} \]

\[
= a_1 \cdot y(n+1) + e(n)
\]

\[
h(n) + \hat{y}(n)
\]

![Sigma-Delta attenuator](image2)

Fig. 2. Σ-Δ attenuator.

(a) Circuit implementation.

(b) Equivalent model at baseband

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As mentioned above, the \( \Sigma-\Delta \) IIR filtering proposed here can be applied to standard IIR filter structures. However, structures with good performance for oversampled transfer-functions should be used since these types of functions are a natural consequence of using \( \Sigma-\Delta \) modulation. Specifically, consider the two possible realizations for a first-order lowpass filter as shown in figure 3. It is not difficult to see that for large oversampled transfer-functions, the coefficient \( a_1 \) is close to zero. Therefore, modelling the \( \Sigma-\Delta \) modulator as in figure 2(b), the realization in figure 3(a) is impractical because its noise gain to \( x(n) \) is much greater than the equivalent noise gain in figure 3(b). One possible structure with good performance for oversampled transfer-functions is a recently developed quasi-orthonormal state-space structure [6]. Making use of this structure and the attenuator circuit, described above, results in the \( N \)-th order \( \Sigma-\Delta \) filter shown in figure 4. Each multi-bit state signal, \( x_i(n) \), is applied to a \( \Sigma-\Delta \) modulator resulting in a one-bit signal \( \hat{x}_i(n-1) \) that closely approximates \( x_i(n-1) \) over the baseband frequency. Note that all the additions shown in figure 4 need not be realized as adders. For example, the signal at node A takes on only one of \( 8 \) possible values and is therefore more efficiently realized as an \( 8 \)-input multiplexer rather than two adders. In fact, the only adders required are the two in each modulator and one for each filter state. With these simplifications, it is clear that for an \( N \)-th order filter using second-order \( \Sigma-\Delta \) modulators, only \( 3N \) adders are required together with some minor logic. This low amount of complexity should make this type of filtering very economical in a VLSI technology.

**Design Examples**

To demonstrate the validity of this approach, a fifth-order prototype filter was simulated for three different oversampling ratios; OSR = 32, 64, and 128. The coefficient values for these three filters are given in Table 1 where it is clear that the coefficients approach zero as the oversampling ratio is increased.

To measure the frequency responses, sine waves at varying frequencies were first passed through a \( \Sigma-\Delta \) modulator, then the filter, and finally an FFT and Hanning window of the resulting one-bit stream indicated the magnitude response at the sine wave’s frequency. Although this method of measurement is much more computationally intensive than using an impulse response (as in [3]), it allows more power at each frequency and therefore gives a more realistic estimate of the signal-to-noise performance of the filter. In figure 5, the frequency responses for the three filters are shown as well as the response for an eighth-order bandpass filter with an OSR of 128. The signal-to-noise ratio (SNR) was found through simulation as the ratio of the output power of a single sinusoid (peak values of \( \pm 1/4 \) for quantizer output levels of \( \pm 1 \)) at the upper passband edge of the filter to the total output noise power over the
To model the noise source, $e(n)$, in figure 2(b), the quantizer in figure 1 is modeled as adding white noise uniformly distributed in [-1,+1] resulting in a power spectral density of $\frac{1}{3}$. With this assumption, it is not difficult to show that the power spectral density, $S_e(f)$, of $e(n)$ is found by shaping this white noise source by the error transfer function of the modulator, $(1-z^{-1})^2$. Mathematically,

$$S_e(f) = \frac{1}{3} \left| 1 - e^{-j2\pi f} \right|^2$$

Finally, the power spectral density of the output, $S(f)$, is easily shown to be given by,

$$S(f) = |W(f)|^2 S_e(f)$$

A comparison between the expected and simulated noise curves are shown in figure 6 for the $\Sigma$-$\Delta$ lowpass filter with OSR = 32. The simulated noise curves were obtained by averaging 256 periodograms each of length 4096 resulting in 64 FFT bins over the frequency of interest. Note that the output signal can be considered to be either the one-bit signal, $y(n)$, or the multi-bit signal, $N(n)$. While in the frequency band of interest, the noise for these two output signals is approximately the same, out-of-band noise is significantly higher for $y(n)$ as shown in figure 7. The lower out-of-band noise on $y(n)$ is due to all the one-bit modulated signals being filtered by the last integrator that forms $y(n)$. Noise comparisons were also performed for the eighth-order filter and gave similar agreement.

**Conclusions**

A design methodology for realizing IIR filters on $\Sigma$-$\Delta$ modulated signals was proposed. The method makes use of standard IIR filter structures except that multi-bit filter states also exist as one-bit signals obtained by modulating the multi-bit signals. It was shown that only 3N adders together with some minor logic are required to implement an Nth order filter using second-order modulators. Noise analysis and simulated results show that a linear noise analysis gives an excellent prediction of noise performance over the frequency band of interest. This type of filtering should prove useful in VLSI technologies where interfaces to analog signals are required.

**References**


Fig. 6. Power spectral density of the output noise for frequency of interest for the lowpass filter with OSR = 32. Input was a dc signal of value 0.3047590684736. (solid - simulation; dotted - expected noise via linear analysis)

Fig. 7. Power spectral density of the output noise over all frequencies for the lowpass filter with OSR = 32. Input was a dc signal of value 0.3047590684736.