A High-Quality Analog Oscillator Using Oversampling D/A Conversion Techniques

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Abstract

This paper describes a high-quality analog oscillator designed specifically for audio applications. Except for a rather imprecise low-pass filter and a 1-bit D/A, the proposed circuit is entirely digital, providing accurate control over its oscillation frequency and amplitude. Experimental results have indicated an effective dynamic range of approximately 70 dB, equaling the behaviour of a Hewlett-Packard HP3245A high-performance signal generator.

1 Introduction

Oversampled delta-sigma digital-to-analog converters (DACs) are rapidly gaining in popularity due to their high linearity [1]. This paper demonstrates how the concept of delta-sigma modulation can be combined with a digital resonator [2] to produce high-quality analog waveforms with minimal silicon overhead.

The realisation is based on a recently developed filtering approach known as delta-sigma based IIR filtering [3]. This scheme achieves significant hardware savings by operating the entire circuit at the oversampled rate. In doing so, the need for an interpolation filter is completely eliminated. Furthermore, multi-bit multiplications are avoided by re-modulating an internal multi-bit state using a fully digital delta-sigma modulator.

The outline of this paper is as follows. Section 2 more fully describes the fundamental theory supporting the proposed oscillator. Here, parallels are drawn to the analog LC-tank circuit. Section 3 discusses the physical components of the circuit as well as the practical issues of implementation. In this section, techniques which work to minimise the total circuit area are discussed. Equations relating the oscillation frequency and amplitude to circuit parameters are presented. Section 4 contains simulation and experimental results.

2 General Theory

A complete synthesis procedure exists for designing digital filter circuits based on LC-ladder networks [4]. The structure of the digital filter that results is generally formed from a set of coupled second-order resonators. These resonators are formed by cascading two discrete-time integrators of the form \( z^{-1}/(1-z^{-1}) \) and \( 1/(1-z^{-1}) \) in a loop with the sign of one integrator being positive and the other negative, such as that shown in Fig. 1. As a result of this approach, digital filter circuits with some of the lowest noise behavior and best sensitivity properties are known to exist.

![Figure 1: A second-order digital resonator circuit.](image)

As a special case of this synthesis procedure, a digital oscillator circuit can also be realized by simply eliminating the effect of damping in the filter circuit. Thus, the resonant circuit of Fig. 1 can be used to create a digital oscillator circuit with good noise and sensitivity properties. It is useful to consider the analog of this second-order digital oscillator circuit, the parallel LC-tank circuit, as it reveals some of its interesting properties. Since the LC-tank circuit is lossless, it follows that once the circuit is excited, no energy is lost but instead alternates between the capacitor and inductor. The result is a capacitor voltage and inductor current whose waveforms are ideal sinuosoids with
frequency \( \omega_o = 1/\sqrt{LC} \).

Two facts are important to note about the energised LC-tank circuit: (1) variations in either the capacitor or inductor values do not prevent the circuit from oscillating, but only shift the frequency of oscillation; (2) the amplitude of oscillation is determined by the initial conditions imposed on the capacitor and inductor.

Returning to the second-order digital resonator of Fig. 1, we can conclude from the above two observations that finite register length effects will not prevent the resonator from oscillating, only alter its precise frequency of oscillation. In fact, from the characteristic equation of the resonator circuit in Fig. 1, one finds that the frequency of oscillation is given by the following equation.

\[
\omega_o = \frac{1}{T} \tan^{-1} \left( \frac{\pm \sqrt{a_{21}a_{12}(4-a_{21}a_{12})}}{a_{21}a_{12} - 2} \right), \quad T = \frac{1}{f_{sa}}
\]

(1)

This is true provided \( 0 \leq a_{21}a_{12} \leq 4 \). This constraint is necessary in order to maintain complex poles. Secondly, the amplitude of oscillation can easily be controlled by loading the appropriate initial conditions into the registers of the digital circuit. If \( z_1 \) and \( z_2 \) are the initial values of registers 1 and 2 respectively, it is believed that the amplitude of the oscillating tone can be calculated from the equation below.

\[
A = \frac{z_1}{\sin \left( \tan^{-1} \left( \frac{\sin(\omega_o T)}{z_1 + \frac{1}{a_{21}}a_{12} - \cos(\omega_o T)} \right) \right)}, \quad z_1 \neq 0
\]

(2)

If \( z_1 \) is to be initialized at 0, a similar equation can be derived with the constraint \( z_2 \neq 0 \). Note that, in the ideal case, initializing both registers at 0 corresponds to \( A=0 \) or no oscillation.

Realisation of a digital oscillator in this manner has recently been demonstrated by Turner [2]. The goal of this paper is to utilize this digital resonator principle in the design of a low-frequency analog oscillator. In this way, an analog oscillator with precise control over its oscillation frequency and amplitude can be realised without trimming techniques or adaptive adjustment schemes.

A rather straightforward way to convert the digital signal to analog form is to make use of a digital-to-analog converter (DAC). Since the frequency range of operation is limited to less than 20 kHz, oversampling techniques can be used. A typical single-bit oversampling DAC consists of a digital interpolation filter, followed by a digital delta-sigma modulator and finally an imprecise analog low-pass reconstruction filter. The interpolator receives an N-bit digital word at rate \( f_a \) and upsamples it to a rate \( f_{sa} \), maintaining the N-bit word length. The delta-sigma modulator then converts this N-bit word to a single-bit data stream at the same rate \( f_{sa} \). This data stream contains both the low-frequency analog information and shaped quantisation noise. The low-pass filter then removes the high-frequency quantisation noise and reconstructs the analog signal. Unfortunately, this approach requires much silicon area. Therefore, an alternative approach is desirable. As will be shown below, the interpolation filter is unnecessary. Additionally, the two N-by-N bit multipliers in the resonator circuit may also be eliminated, simplifying the design substantially.

3 An Area-Efficient Oscillator Circuit

Utilizing the concept of the delta-sigma attenuator circuit [3] shown in Fig. 2, we can replace an N-by-N bit multiplier in series with a unit delay by a delta-sigma modulator followed by a 1-by-N bit multiplier. Although they are not exactly equivalent as illustrated by the output spectrums shown in Fig. 2, they act on the bandlimited input spectrum in exactly the same way. Therefore, if we limit ourselves to low-frequency inputs relative to \( f_{sa} \), we can assume that the delta-sigma attenuator circuit will behave in much the same way as the N-by-N bit multiplier with a unit delay. This is easily accomplished by limiting the oscillation frequency of the resonator circuit to low frequencies.

With the in-band model of the delta-sigma attenuator circuit in mind, the digital resonator circuit of
Fig. 1 can be rearranged using a simple signal-flow-graph manipulation. Referring to the top integrator in Fig. 1, the unit delay in the feedforward path may be moved into the feedback path by placing another unit delay in series with the output. Immediately, we can replace the unit delay in series with the N-by-N bit multiplier by the delta-sigma attenuator. It is worthwhile to note that the output of the resonator can be taken directly from the output of the delta-sigma modulator. Digital-to-analog conversion of the one-bit signal may be carried out very simply by low-pass filtering the output bit stream. If the oscillator is designed such that a high SNR is maintained well above the frequency range of interest (20 kHz), a low-order filter will be sufficient to filter the output.

To further reduce the complexity of the digital resonator, we recognize from Eqn. (1) that the oscillation frequency is dependent on the product of the two coefficients $a_{12}a_{21}$. Therefore, by assigning a value of unity to $a_{21}$, the corresponding N-by-N bit multiplier may be eliminated while maintaining complete control over the oscillation frequency $\omega_c$. Finally, because the delta-sigma output can only take on the values +1 and -1, it follows that the output of the 1-by-N bit multiplier must be either $+a_{12}$ or $-a_{12}$. Therefore, the 1-by-N bit multiplier can be realized more efficiently as a 2-input multiplexer. The final circuit is shown in Fig. 5. While simulations have shown that Eqns. (1) and Eqn. (??) may be applied to the modified circuit in many cases, the validity of this assumption is the topic of further investigation.

4 Simulation and Experimental Results

To investigate the behavior of the digital resonator shown in Fig. 3, digital simulations were performed with the digital signal processing software package, Comdisco [5]. This software package allows the modeling of DSP operations with the effects of finite register lengths included. The delta-sigma modulator was assumed to be a second-order modulator of the type shown in Fig. 4 and clocked at a rate $f_{\text{c}} = 2.62$ MHz. A two's complement number system was used with numbers ranging from -1 to +1. The register lengths were set at 32 bits. The resonator was designed to oscillate at 2560 Hz (corresponding to $a_{12} = 0.000037690832$), much lower than the oversampling clock rate ($f_{\text{c}}$). The reader should note that the oversampling clock rate is not an integer multiple of the oscillation frequency, as this is an important advantage of the design. Arbitrary oscillation frequencies can be created within the precision of the register lengths. With the state of the first register set at zero and the second register initialized to 0.002, a transient analysis was run for approximately 39 ms. On completion, a 65536-point FFT was performed on the last 64 periods of the output tone. To avoid spectral smearing, the samples on which the FFT was performed were from the output signal in steady-state. Fig. 5 shows the output signal on two different scales. The upper graph displays the spectrum over a 20 kHz bandwidth. In this figure, the presence of the 2560 Hz tone is clearly evident. The background noise can be seen approximately 70 dB below the level of the 2560 Hz tone. The lower graph displays the spectrum over a 1 MHz bandwidth. Here, the noise-shaping characteristics of the second-order modulator can be observed. Note that the quantization noise has been pushed up to frequencies well above the range of interest (20 kHz).

To further explore the practicality of this resonator circuit, 1024 points of the steady-state output bitstream computed by Comdisco were downloaded to a Hewlett-Packard data generator. The output from the data generator was then applied in repetition to a continuous-time HP spectrum analyzer. Fig. 6 illustrates the output spectrum seen directly on the spectrum analyzer. The upper graph displays the output spectrum over a 20 kHz bandwidth and the lower graph displays the output spectrum over a 1 MHz bandwidth. From the upper graph, the spectral pu-
Figure 5: Output spectrum associated with the simulated periodic bit-stream generated by the digital resonator circuit: (a) In-band spectrum up to 20 kHz; (b) Out-of-band spectrum up to 1 MHz.

Figure 6: Measured spectrum of the output bit-stream from the resonator circuit of Fig. 3 (a) In-band spectrum up to 20 kHz; (b) Out-of-band spectrum up to 1 MHz.

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References


