Millimetre-Wave Voltage Controlled Oscillators

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August 2005

Abstract

This thesis describes a systematic design procedure for millimetre-wave voltage controlled oscillators (VCOs) based on a comprehensive investigation of SiGe HBT VCOs. In unison with the design procedure, 13 differential Colpitts test circuits were implemented in a 0.18 \(\mu\)m SiGe HBT BiCMOS process which resulted in some of the lowest phase noise and widest tuning integrated VCOs reported to date. VCOs at 35 GHz and 60 GHz had measured phase noise of -112.7 dBc/Hz and -104 dBc/Hz at 1-MHz offset, respectively. Major contributions include a validated design procedure based on original analytical phase noise derivations that account for noise correlation, design techniques for optimizing accumulation-mode nMOS varactors, and a novel push-push VCO architecture. Although this design procedure is specific to the Colpitts topology, it shares general design techniques that are applicable to all types of VCO architectures.
Acknowledgments

My sincere gratitude to Professor Sorin Voinigescu for granting me the opportunity to participate in this exciting field of research, in addition to his guidance and support throughout my time of study at the University of Toronto.

I would also like to express my thanks to all family and friends, and colleagues at the University of Toronto for making it easier.
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Acronyms

ACC: automotive cruise control
AGC: automatic gain control
ADC: analog-to-digital converter
AMOS: accumulation-mode nMOS (nMOS in n-well)
BiCMOS: bipolar and CMOS devices
BPF: band pass filter
CMOS: complementary metal oxide semiconductor
DAC: digital-to-analog converter
DR: dielectric resonator
FMCW: frequency modulation continuous wave
GaAs: gallium arsenide
Gbps: gigabit per second
GHz: gigahertz, $10^9$ hertz
HBT: heterojunction bipolar transistor
IC: integrated circuit
IF: intermediate frequency
InP: Indium Phosphide
LAN: local area network
LDMS: local multi-point distribution service
LNA: low noise amplifier
LOS: line of sight
MIM: metal-insulator-metal
mm-wave: millimetre-wave
MMIC: monolithic microwave integrated circuit
MOSFET: metal oxide semiconductor field effect transistor
n-MOS: n-channel MOSFET
PA: power amplifier
PLL: phase-locked loop
p-MOS: p-channel MOSFET
PSA: power spectrum analyzer
Q-factor: quality factor
RF: radio frequency
SiGe: silicon germanium
SOI: silicon over insulator
SRF: self resonant frequency
SSB: single side band
VCO: voltage controlled oscillator
WAN: wide area network
WLAN: wireless local area network
WPAN: wireless personal area network
Symbols

\( \beta \): bipolar collector-base current ratio

\( \omega_{\text{osc}} \): oscillation frequency in radians

\( \omega_m \): offset frequency from fundamental oscillation frequency

\( \tau \): base/collector transit time

\( C_{1\text{ext}} \): external capacitance located across base-emitter

\( C_{\text{be}} \): base-emitter junction capacitance

\( C_{\mu} \): base-collector junction capacitance

\( C_{\text{cs}} \): collector-substrate junction capacitance

\( C_j \): p-n junction capacitance

\( C_{\text{je0}} \): depletion capacitance across base-emitter junction

\( f_T \): unity current gain frequency

\( f_{\text{MAX}} \): unity power gain frequency

\( G_m \): large signal transconductance

\( g_m \): small signal transconductance

\( I_{\text{DC}} \): DC bias current

\( \overline{i_{\text{nb}}^2} \): mean squared noise current representing the shot noise in emitter-base space-charge layer

\( \overline{i_{\text{nc}}^2} \): mean squared noise current representing the shot noise in base-collector space-charge layer

\( J_c \): current density

\( l_E \): emitter length

\( L_{\text{tank}} \): resonant tank inductance
$P_{DC}$: DC power consumed by circuit in mW

$P_{OUT}$: Single-ended output power in dBm

$q$: electron charge

$Q$: quality factor

$R$: series resistive losses of tank inductor

$R_p$: equivalent parallel resistance of tank inductor

$S_{\Delta \text{in}}$: input phase noise

$S_{\Delta \text{out}}$: output phase noise

$T_{\text{osc}}$: oscillation period

$t_{\text{gate}}$: gate propagation delay

$V_{DD}$: positive DC supply voltage

$V_{\text{osc}}$: voltage swing amplitude across LC-resonant tank

$\overline{v_{nL}^2}$: mean squared noise voltage associated with ohmic losses in base inductor

$\overline{v_{nb}^2}$: mean squared noise voltage associated with the base resistance thermal noise

$\overline{v_{ne}^2}$: mean squared noise voltage associated with the emitter resistance thermal noise

$V_T$: thermal voltage

$Z_o$: characteristic impedance of transmission line
Chapter 1

Introduction

1.1 Millimetre-Wave Applications

Mainstream commercial technology is predominant at microwave frequencies, but will soon reach into the mm-wave spectrum to take advantage of the looser regulations and the progressively faster and cost-effective silicon-based IC processes. The future heralds many promising mm-wave commercial applications as described in Table 1.1.

Communication service providers are deploying Local Multipoint Distribution Services (LDMS) to act as a relatively inexpensive and quick last mile broadband solution for providing interactive video, Internet and voice services through a fixed wireless link. The next step in long-haul fiber-optic communications is 40-80 Gbps to increase spectral efficiency, thereby enabling higher bandwidth services at lower costs [1]. 60 GHz radio targets the wireless personal area network (WPAN) market, but may also engage in line-of-sight (LOS) LANs with greater distances up to 1 km [2]. 60 GHz radio is appealing due to its ability to accommodate the well known heterodyne architecture, the vast unlicensed bandwidth, and loose transmit power regulations. The 57-64 GHz band is unlicensed in North America, but sub-bands have already been allocated in Japan and Europe. Automotive cruise control (ACC) at 77-GHz is being...
quickly adopted as the next luxury feature in automobiles. There already exists a few first generation ACC systems for luxury passenger automobiles such as BMW’s “Active Cruise Control”, Jaguar’s “Adaptive Cruise Control”, and Daimler-Benz’s “Distronic” system. Another foreseeable application is imaging near 100 GHz and beyond. Millimetre-wave imaging is a very open field with minimal regulation since the atmospheric absorption properties at these frequencies are heavily adverse to signal propagation.

<table>
<thead>
<tr>
<th>Application</th>
<th>Description</th>
<th>Frequency Band</th>
</tr>
</thead>
<tbody>
<tr>
<td>Local Multipoint Distribution Service (LDMS)</td>
<td>Terrestrial communications (1-4 miles)</td>
<td>20-40 GHz</td>
</tr>
<tr>
<td>Fiber-optic communications</td>
<td>Long-haul terrestrial WAN communication networks (&gt;40 Gbps)</td>
<td>20-40 GHz</td>
</tr>
<tr>
<td>60 GHz Radio</td>
<td>WPANs: short haul high capacity traffic (&gt; 1 Gbps)</td>
<td>57-64 GHz</td>
</tr>
<tr>
<td>Automotive Radar</td>
<td>Automotive cruise control (ACC)</td>
<td>76-77 GHz</td>
</tr>
<tr>
<td>Imaging</td>
<td>Image scanning/detection systems</td>
<td>100+ GHz</td>
</tr>
</tbody>
</table>

Table 1.1: Next generation mm-wave markets and applications

These applications have recently caught the attention of corporations and researchers worldwide primarily due to the progress made in conventional silicon-based integrated circuit processes such as CMOS and SiGe BiCMOS. The main economic impasse for most mm-wave applications is the high production cost associated with the required discrete components and MMICs that are typically fabricated in low-yield III-V semiconductor processes. Modern silicon-based processes offer solid-state devices with sufficient speed to enable the possibility of highly integrated lower-cost solutions to compete in high-volume mm-wave markets.
1.2 VCO Design Criteria for mm-Wave Applications

It is difficult to show explicit VCO specifications for each application as it strongly depends on the overall system design. Nonetheless, designers should expect stringent specifications on the VCO, which is a fundamental block in both mm-wave sensor and wireless communications systems (Figures 1.1 and 1.2 [3]). Based on current wireless communications systems, the 3 most important performance requirements of a mm-wave VCO in ultrawideband radio systems (LDMS, 60-GHz WPAN) are:

a) Low VCO phase noise, which is often the most difficult and confounding property to optimize. A spectrally pure VCO is required for a dense channel spacing to efficiently utilize the available bandwidth.

b) Sufficient output power to drive the mixer. For instance, the Gilbert Cell topology is a popular choice for integrated mixer designs, which requires the VCO to supply a minimum of approximately -6 dBm to effectively switch the mixing quad.

c) Sufficiently wide tuning range to cover process variations, temperature variations, and frequency hopping schemes. A rough estimate of the required tuning range is at least 20 percent of the carrier frequency: 10 percent to cover temperature and process variation, and 10 percent to cover frequency hopping schemes.

The same three VCO criteria: wide tuning range, low phase noise, and output power are required in mm-wave sensor systems. Although frequency hopping schemes are not used in most sensor systems, wide tuning range is still crucial for handling process variations and the extreme temperatures that a sensor may experience. Sensor and radar systems rely on changes in frequency of the transmitted VCO signal reflecting off an object to deduce its location and velocity. Hence, the phase noise
of the VCO will directly impact the overall system sensitivity. For example, it has been suggested, based on experimentation that ACC systems require VCOs with $<-80$ dBc/Hz phase noise at 100 kHz offset to have satisfactory velocity discrimination [3]. Furthermore, the low transmit power required by ACC systems (only 0-13 dBm) allows the VCO to drive the antenna without a power amplifier as depicted in Figure 1.2.

![Figure 1.1: Block diagram of heterodyne RF front-end for 60 GHz radio.](image)
CHAPTER 1. INTRODUCTION

1.3 Objective of Thesis

The objective is to provide a thorough analysis of mm-wave VCOs through theoretical and experimental means. This analysis should be the basis of a design procedure for building reliable and optimized mm-wave VCOs.

1.4 Contributions From This Work

VCO design can be arcane to RF designers not familiar with this fundamental block. It can become a game of arbitrarily varying design parameters in the circuit simulator to achieve a VCO design that may not necessarily be optimized. Even though there are a few well known design practices for improving VCO phase noise, such
as maximizing the resonant tank quality factor (Q-factor), maximizing the voltage tank swing, and choosing devices with low $\frac{1}{f}$ noise [4,5], there is currently no systematic study and design methodology for robust, wide tuning and lowest phase noise VCOs. To that end, this thesis presents an algorithmic VCO design methodology and contributes new design insight through original theoretical phase noise analysis.

In addition to high integration and yield, another benefit of CMOS and BiCMOS processes is the availability of accumulation-mode n-MOS (AMOS) varactors, which are used to tune the VCO frequency. This work has developed AMOS design methods for maximizing Q-factor based on an experimental study of the varactor at mm-wave frequencies. Also, the feasibility of multi-turn spiral inductors and AMOS varactors at mm-wave frequencies is demonstrated in VCOs operating up to 122 GHz.

Finally, a novel push-push VCO topology is presented in this thesis. The main enhancement over previous topologies is that it inherently isolates the output from the resonant tank, thereby improving phase noise and mitigating load pulling.
Chapter 2

Background

2.1 Popular Types of Oscillators

2.1.1 Ring Oscillators

Ring oscillators are generally implemented as a chain of inverters without the use of LC-resonant elements (Figure 2.1). The oscillation period \( T_{osc} \), which is approximated by Expression 2.1 is limited by the gate delay \( t_{gate} \) of the inverting element.

\[
T_{osc} = 2n \times t_{gate}
\]  

(2.1)

This type of VCO is good for low power designs requiring multi-phase sampling. The absence of inductors and capacitors allows for a small area and easy integration.

Figure 2.1: Block diagram of ring oscillator with \( n \) inverting stages.
in current CMOS and SiGe BiCMOS processes. The shortcomings of this VCO are poor spectral purity and relatively low frequency of oscillation.

### 2.1.2 LC Oscillators

LC oscillators consist of two energy storage elements operating in resonance to stabilize the oscillation frequency. Figure 2.2 is a simple block diagram of an LC-resonant oscillator, where the oscillation frequency is given by \( \frac{1}{2\pi\sqrt{LC}} \).

![Figure 2.2: Block diagram of LC resonant VCO.](image)

The LC-resonant VCO is most suitable for integrated high frequency designs that demand low phase noise and moderate tuning range. Low power designs are possible with certain LC topologies such as the cross-coupled topology. One drawback is the high area consumption by inductors and capacitors, but this becomes a non-issue at mm-wave frequencies as the inductors and capacitors scale down in value and physical size. Additionally, integrated inductors are well controlled over process and temperature (less than 5% variation) consequently improving the VCO sensitivity to process variation.

### 2.1.3 Dielectric Resonator Oscillators

Dielectric resonator oscillators (DRO) are based on the same concept as the LC oscillator with the exception that a dielectric resonating (DR) puck acts as the frequency
stabilizing element. DR pucks are discrete components that use transmission lines to magnetically couple the resonator (Figure 2.3 [6]).

Figure 2.3: DRO using a transmission line to magnetically couple the dielectric resonating puck.

The prime advantage of the DRO is very low phase noise owing to the extremely high (> 1000) Q-factor of the resonator. Its limitations include a narrow tunable bandwidth and the inability to integrate the resonator making it expensive to produce. DROs are used in measurement devices and military applications where unit volume is small.

2.2 LC-Resonant VCO topologies

2.2.1 Cross-coupled Fundamental Mode VCO

A literature review on mm-wave integrated VCOs reveals that the two most common topologies are the cross-coupled and the selective feedback. As the name implies, the former uses cross-coupling transistors as positive feedback to sustain oscillation at a frequency given by Expression 2.2, where $C_{tot}$ is the total capacitance at the
output node (Figure 2.4). The startup condition requires that the negative resistance equal the total losses in the resonant tank at the frequency of oscillation, resulting in Condition 2.4 [7].

\[ f_{osc} = \frac{1}{2\pi \sqrt{L_{tank} C_{tot}}} \]  

(2.2)

**Negative Resistance**

\[ \text{Negative Resistance} = -\frac{2}{G_m} \]  

(2.3)

\[ (g_m R_p)^2 \geq 1 \]  

(2.4)

The maximum achievable oscillation frequency can be derived by removing the variable capacitor \( C_{\text{var}} \) to minimize the total capacitance. For a bipolar implementation, this would lead to Expression 2.5, where \( C_{\text{be}}, C_{\mu}, \) and \( C_{cs} \) represent the base-emitter, base-collector and collector-substrate junction capacitance, respectively.

\[ C_{tot} = (C_{\text{be}} + 4C_{\mu} + C_{cs} + C_{\text{load}}) \]  

(2.5)
CHAPTER 2. BACKGROUND

If the Q-factor of the inductor is assumed constant irrespective of size, then the effective parallel tank resistance \( R_p \) can be written as:

\[
R_p \approx \omega_{osc} L_{tank} Q = \frac{Q}{\omega_{osc} C_{tot}} \tag{2.6}
\]

The maximum oscillation frequency can now be solved by combining Expressions 2.4 - 2.6, resulting in Expression 2.7. The fastest reported cross-coupled integrated VCO is 103 GHz implemented in 130-nm CMOS [8].

\[
\omega_{osc} \leq Q \frac{g_m}{C_{be} + 4C_\mu + C_{cs} + C_{load}} \tag{2.7}
\]

2.2.2 Selective Feedback Fundamental Mode VCO

There are four original selective feedback arrangements each named after their inventors: Clapp, Armstrong, Hartley and Colpitts. This thesis will focus on the common-collector Colpitts VCO because of its inherent low phase noise [5], robustness and ease of realizing negative resistance at high frequencies. A simplified schematic of the topology is shown in Figure 2.5.

![Figure 2.5: Single-ended common-collector Colpitts VCO.](image)
The capacitor $C_2$ is required to realize negative resistance (Equation 2.8) that must exceed the losses in the resonant tank at the frequency of oscillation (Equation 2.9). Notice that the output load capacitance ($C_{\text{load}}$) does not add to the equivalent tank capacitance ($C_{eq}$) because it is buffered from the LC-resonant tank.

$$\text{NegativeResistance} = -\frac{g_m}{\omega^2(C_1 + C_{be})C_2} \quad (2.8)$$

$$f_{osc} = \frac{1}{2\pi \sqrt{L_{\text{tank}}C_{eq}}} = \frac{1}{2\pi \sqrt{L_{\text{tank}} \left( \frac{(C_1+C_{be})C_2}{C_1+C_{be}+C_2} + (1 + g_m Z_{\text{load}})C_{\mu} \right)}} \quad (2.9)$$

The maximum frequency of oscillation can be derived by first removing the external capacitor $C_1$, and by setting the transistor gain ($g_m Z_{\text{load}}$) to a realistic value of 1. Next, the losses in the resonant tank is approximated with a constant tank inductor Q-factor (Expression 2.10). Finally, solving the system of equations 2.8 - 2.10 for $\omega_{osc}$ gives the maximum frequency of oscillation (Expression 2.11).

$$R_{\text{losses}} \approx \frac{\omega_{osc} L_{\text{tank}}}{Q} \quad (2.10)$$

$$\omega_{osc} \leq Q g_m \left[ \frac{1}{(C_{be} + C_2)} + \frac{2C_{\mu}}{C_{be} C_2} \right] \quad (2.11)$$

One last simplification can be made by the fact that for achieving highest oscillation frequency, the external capacitor $C_2$ is designed to be as small as possible ($C_2 \ll C_{be}$). Thus, the oscillation frequency limit can be approximated as:

$$\omega_{osc} \leq Q \frac{g_m}{C_{be}} \quad (2.12)$$

In comparison to the cross-coupled topology (Expression 2.7), the oscillation frequency of the Colpitts is higher because it is not hampered by the large loading capacitance ($C_{\text{load}} + C_{cs}$). The current state-of-art implementation of a fundamental
2.2.3 2nd Harmonic (Push-Push Mode) VCO

All fundamental mode VCOs with an integrated LC-resonant tank suffer from low Q-factors at high frequencies. This is attributed to the greater losses caused by skin effect, eddy currents induced in the substrate, and parasitic capacitances. A low resonator Q-factor translates to poor phase noise. This shortcoming is addressed by the push-push mode VCO, which is essentially two fundamental frequency VCOs oscillating differentially at one half the output frequency. This allows for higher passive component Q-factors. For proper operation of the push-push VCO, the even-mode oscillation of the differential circuit must be suppressed while promoting the odd-mode (Figure 2.6). In odd-mode, the fundamental frequency ($f_{osc}/2$) and all odd harmonics cancel themselves at the output load $R_L$, whereas all even harmonics add in phase. Differential (odd-mode) oscillation is guaranteed by satisfying the start-up Conditions 2.13 - 2.16, where $Z_{osc}$ is the impedance seen looking into the base inductor ($L_b$).

Figure 2.6: Push-push Colpitts oscillator.
CHAPTER 2. BACKGROUND

\[
\text{Re} \left[ \frac{Z_{osc} \, f_{osc}}{2} \right] < 0 \quad (2.13)
\]

\[
\text{Re} \left[ \frac{Z_{osc} \, f_{osc}}{2} \right] + 2R_L > 0 \quad (2.14)
\]

\[
\text{Im} \left[ \frac{Z_{osc} \, f_{osc}}{2} \right] = 0 \quad (2.15)
\]

\[
\frac{\partial \text{Im} \left[ \frac{Z_{osc} \, f_{osc}}{2} \right]}{\partial f} > 0 \quad (2.16)
\]

- Condition 2.13 ensures odd-mode oscillation by having sufficient negative resistance to overcome the losses in the resonator (Figure 2.7a).

- In even-mode, the voltages add constructively at \( R_L \), which appears as a load with double the resistance (Figure 2.7b). Thus, Condition 2.14 ensures that even-mode oscillation is quenched by having the total even-mode resistance greater than the negative resistance.

- Condition 2.15 and 2.16 ensures a stable resonance at the desired frequency.

The fastest reported silicon-based integrated VCOs are Colpitts push-push VCOs. The state-of-the-art in CMOS and SiGe HBT is 114 GHz and 150 GHz, respectively [10,11].
2.3 Integrated Passive Components

2.3.1 Variable Capacitors

An LC-oscillator is typically converted into a VCO by replacing the fixed capacitance of the resonant tank with a variable counterpart, such as a varactor. Varactors are realized by pn-junction diodes or Metal-Oxide-Semiconductor (MOS) devices. The former works in reverse bias and relies on the depletion capacitance formed across the space-charge region, whereas the latter is based on the capacitance across the gate oxide. A MOS varactor can be either a p-MOS, n-MOS, or an accumulation-mode n-MOS (AMOS), which is effectively an n-MOS formed inside an n-well (Figure 2.8a). The AMOS is the best of the three because it has the lowest channel and source/drain resistance. MOS varactors should be used in the accumulation mode to exploit the linear C-V characteristics, and to avoid the abrupt behaviour in the inversion region, as shown in Figure 2.8b.

It has been found that the MOS varactor, especially the AMOS, is advantageous over the pn-junction diode because of its higher Q-factors and subsequently lower phase noise VCOs [12]. AMOS varactors have also been shown to produce some of
CHAPTER 2. BACKGROUND

2.3.2 Fixed Capacitors

Metal-insulator-metal (MIM) fixed capacitors consist of two metal planes sandwiching a thin dielectric layer formed high above the bulk substrate. The distance from substrate minimizes the parasitic bottom-plate capacitance, and the exclusive use of metal equates to a high Q-factor. This merits the use of MIM capacitors to implement on-chip capacitors such as $C_1$ in Figure 2.5 and 2.6.

the widest tuning mm-wave VCOs [13,14].

Figure 2.8: a) AMOS cross-section. b) General MOS varactor C-V characteristics. c) AMOS cross-section when operating in region 1. d) AMOS cross-section when operating in region 2.
2.3.3 Inductors

At mm-wave frequencies, inductance is realized by either a transmission line or a multi-turn spiral inductor. The latter results in a more compact design, but are more difficult to model. As with the capacitors in the LC tank, it is important for the inductor to have a high Q-factor, and a self-resonant frequency (SRF) at least three times the operating frequency. The design and optimization of multi-turn inductors at mm-wave frequencies have already been well examined by T. Dickson, et al. [15].
Chapter 3

VCO Circuit Concepts

3.1 Bipolar Transistor Model

The first step to phase noise optimization begins with a definition of the major noise sources within a bipolar transistor (Figure 3.1).

A bipolar transistor has four major noise sources. The two thermal noise sources, $v_{nb}^2$ and $v_{ne}^2$, represent the mean squared noise voltage of the base and emitter resistances. The two shot noise sources, $i_{nb}^2$ and $i_{nc}^2$, represent the mean squared noise voltage of...
the base and collector pn-junctions. The cross correlation between the two shot noise sources is represented by $i_{nbi_{nc}}^*$ [16].

\[
\begin{align*}
\overline{v_{nb}^2} &= 4kTR_b \Delta f \\
\overline{v_{ne}^2} &= 4kTR_e \Delta f \\
\overline{i_{nc}^2} &= 2qI_c \Delta f \\
\overline{i_{nb}^2} &= \frac{2qI_c}{\beta} \Delta f \\
\overline{i_{nbi_{nc}}^*} &= 2qI_c \left(e^{j\omega \tau} - 1\right)
\end{align*}
\]

where,

$R_b =$ base resistance

$R_e =$ emitter resistance

$I_c =$ DC collector current

$\beta =$ collector/base current ratio

$\tau =$ collector/base transit time

$\omega =$ frequency of operation

### 3.2 Fundamental Mode Colpitts VCO

The VCO schematic shown in Figure 3.2 is based on a differential Colpitts architecture first integrated in silicon at 1.5 GHz [17] and later scaled to mm-wave frequencies both in fundamental and in push-push VCOs [10,11,18–21]. To further improve noise and design robustness, a number of developments borrowed from LNA designs are simultaneously applied. These circuit techniques include:

i) a differential cascode topology for improved tank isolation and power gain at mm-wave frequencies [18],
ii) inductive emitter degeneration \((L_E)\) to increase the linearity of transistors [18],

iii) inductors used to isolate the half-circuits \((L_{EE})\), thereby allowing for a single tail bias [18],

iv) the current source is replaced with a resistor to minimize noise at DC [22],

v) a shunting capacitor inserted across the resistor bias to prevent the injection of high frequency noise into the resonant tank [22].

![Differential common-collector Colpitts VCO.](image)

Figure 3.2: Differential common-collector Colpitts VCO.

It can be easily demonstrated that a resistor bias contributes less noise than a current source by first considering the spectral noise densities of the two biasing circuits shown in Figure 3.3. For the spectral noise density of the resistor \((S_R)\) to be
lower than spectral noise density of the current source \( S_{cs} \), Condition 3.6 must be satisfied.

\[
\frac{S_R}{4KT} < S_{cs} \\
\frac{4KT}{R} < 2qI_{bias} \\
\frac{4KTI_{bias}}{V_R} < 2qI_{bias} \\
\frac{2KT}{q} < V_R \\
2V_T < V_R
\] (3.6)

\( V_R \), the voltage drop across the bias resistor, is typically greater than 150 mV to provide sufficient headroom for tuning the varactors. However, it should be noted that the use of a resistor instead of a current source will increase sensitivity to process variation since the manufacturing tolerance on a resistor is worse than that of a transistor.

Figure 3.4 shows the complete schematics of fundamental frequency VCOs implemented at 35 GHz and 60 GHz. Cadence Spectre™ simulated output match to 50 Ω is shown in Figure 3.5.
$L_B$, $L_E$ and $L_{EE}$ in both 35-GHz and 60-GHz VCOs were designed as multi-turn spiral inductors modeled using the Asitic\(^1\)EM simulator. The self-resonant frequency (SRF) and Q-factor of each inductor were optimized by reducing the inductor capacitance to ground, which involves using the minimum width of the top-most metal to minimize the diameter of the inductor for a given inductance [15]. Lastly, the varactor ($C_2$) is implemented as an AMOS device and is tuned by an externally adjustable voltage $V_{tune}$.

The detailed VCO design and optimization is described in chapter 4.

\(^1\)http://rfic.eecs.berkeley.edu/\ niknejad/doc-05-28-01/asitic.html
3.3 2\textsuperscript{nd}-Harmonic Push-Push Mode Colpitts VCO

The 2\textsuperscript{nd}-harmonic push-push VCO schematic shown in Figure 3.6 employs an original configuration which suppresses the fundamental oscillation and reinforces the second harmonic signal. The output is collected from the bias node of the common-base output transistors, thereby providing improved isolation between the resonant tank and the load while permitting differential tuning voltage to be applied to the varactor. In comparison, previously published push-push mm-wave VCOs [10, 11, 21, 23] draw the 2\textsuperscript{nd} harmonic directly from the AC ground at \( L_B \), or from the AC ground above the current source. Their approach is susceptible to load pulling, and detrimental to the resonant tank Q-factor which takes away the main benefit of using a push-push configuration.

This differential topology is nearly identical to the fundamental mode Colpitts VCO, and uses the same noise reducing techniques discussed in the previous section. Figure 3.7 reproduces the complete circuit schematics of 70-GHz and 120-GHz push-push VCOs. The 70-GHz VCO is effectively the 35-GHz VCO operating on the 2nd harmonic, and the 120-GHz VCO is based on the 60-GHz fundamental mode VCO.
Figure 3.6: Novel differential Colpitts push-push VCO.
Figure 3.7: VCO circuit schematics implemented with HBTs and MOS varactors a) 70-GHz push-push VCO design. b) 120-GHz push-push VCO design.
Chapter 4

VCO Analysis and Design

Methodology

This chapter begins with a brief history of phase noise analysis followed by original phase noise derivations based on the Colpitts topology. The resulting analytical expressions lead to phase noise optimization design techniques that were verified by Spectre simulations. With regards to varactor design, a brief section is dedicated to explaining the method used to maximize the quality factor while maintaining an adequate tuning range. Linking together all these design techniques is the systematic design methodology presented in the final section of this chapter.

4.1 Previous Work On Phase Noise Analysis

The phase noise of a resonant-tank VCO was first modeled by D.B. Leeson [24]. He described the phase noise in a feedback loop with a low-pass filter transfer function to emulate the frequency stabilization characteristics of the resonator (Figure 4.1). Leeson’s feedback model gave rise to the single-sideband (SSB) output phase noise in Expression 4.1, also known as the Leeson Formula [4,6].
Figure 4.1: D.B. Leeson’s feedback phase noise model.

\[
S_{\Delta out}(f_m) = \frac{FkTB}{2P_{av}} \left( 1 + \frac{f_c}{f_m} \right) \left[ 1 + \frac{f_0^2}{4Q^2f_m^2} \right] \tag{4.1}
\]

\(F\) represents the noise factor of the amplification circuit and \(f_c\) is the corner frequency at which the \(\frac{1}{f}\) noise is equal to the white noise floor. Equation 4.1 reveals two important design goals for minimizing phase noise:

1. maximize oscillation power \(P_{av}\),

2. maximize loaded resonant tank quality factor (Q-factor).

While very insightful, the simplicity of this expression makes it insufficient for the design of a specific VCO topology because it hides all of the active device design knowledge under the noise factor \(F\). Taking the Colpitts as an example, Leeson’s formula provides no direct insight into the optimal bias condition \((J_c)\), transistor size \((A_e)\), tank inductance \((L_B)\), or capacitor ratio \((C_1:C_2)\). These design parameters are embedded in the noise factor, which must be minimized.
CHAPTER 4. VCO ANALYSIS AND DESIGN METHODOLOGY

In a recent review of Leeson’s formula, J.-C. Nallatamby, et al. [25] applied it to the Colpitts topology resulting in:

\[
S_{\Delta \text{out}}(\omega_m) = 2 \frac{|I_n|^2}{|V_{\text{osc}}|^2} \frac{1}{C_1^2 \left( \frac{C_1}{C_2} + 1 \right)^2} \omega_m^2
\]  

(4.2)

\(|I_n|^2\) represents (in a simplified way) the equivalent noise current of the negative resistance transistor, and \(V_{\text{osc}}\) is the voltage swing across the resonant tank. According to this revised Leeson’s formula, both the \(C_1:C_2\) ratio and \(C_1\) should be maximized in order to minimize phase noise. However, the accuracy of the revised formula is limited by the fact that a single equivalent noise source was used to represent the noise of the transistor. It is well known that two partially correlated equivalent noise sources are required to fully characterize a noisy transistor. In response, the following section recasts the Leeson’s formula with two equivalent noise sources.

4.2 New Theoretical Phase Noise Analysis

In this section, the objective is to derive an accurate phase noise expression as a function of the principal VCO design parameters. This analysis focuses on the single-ended, common-collector Colpitts oscillator. The approach is similar to the one used in the derivation of Expression 4.2 with the exception that two equivalent noise sources are included for an accurate representation of the transistor. Figure 4.2 illustrates all the noise sources considered in this derivation, where \(\bar{\mu}_{nb}^2\) and \(\bar{\mu}_{nc}^2\) were defined in Expressions 3.3 - 3.5 and \(\overline{v_{nL}^2}\) is the tank inductor mean squared thermal noise (Expression 4.3).

\[
\overline{v_{nL}^2} = 4kTR\Delta f
\]  

(4.3)
Figure 4.2: Common-collector Colpitts oscillator with all noise sources featured in this analysis.

A few circuit simplifications are made to the chosen VCO topology of Figure 3.2 to allow for tractable hand derivations. First, the VCO consists of a single bipolar transistor, as opposed to a cascode. Second, the thermal noise contribution due to the emitter and base resistors are ignored. The base resistance is admittedly quite significant and becomes a limitation of this analytical derivation. However, both the base and emitter resistors are included in the phase noise simulations that are presented in the next section.

The first step of the derivation is to evaluate the equivalent input referred noise sources ($V_A$ and $I_A$) of the amplifier circuit (Figure 4.3a). As mentioned earlier, these two partially correlated noise sources fully characterize the noise of the transistor, which is analyzed as a two port network. The next step is to evaluate $V_{A2}$ and $I_{A2}$ to include the external capacitor ($C_{ext}$) into the noiseless two port network as shown in Figure 4.3b. This allows the tank inductor noise ($v_{nL}$) to be added directly to $V_{A2}$ since they are in series. The third step is to evaluate the equivalent noise voltage ($V_{nEQ}$) appearing at the input of the amplifier. Lastly, the output phase noise ($S_{\Delta out}$) is solved based on Leeson’s phase noise model.
CHAPTER 4. VCO ANALYSIS AND DESIGN METHODOLOGY

The theoretical analysis is carried out in detail in the succeeding subsections. In addition, derivations for the tank voltage swing and a proof of an optimal current density bias for lowest phase noise are presented.

![Amplifier circuit with input referred equivalent noise sources](image)

Figure 4.3: Amplifier circuit with input referred equivalent noise sources: a) $V_A$ and $I_A$, b) $V_{A2}$ and $I_{A2}$.

### 4.2.1 Input Referred Equivalent Noise Sources $I_A$ and $V_A$

The approach is to first derive the equivalent noise sources in admittance formalism ($I_{n1}$ and $I_{n2}$ in Figure 4.4 and 4.5), then apply a transformation to convert them into input referred sources ($I_A$ and $V_A$). $I_{n1}$ and $I_{n2}$ is given by:

\[
I_{n1} = -I_1 |_{V_1=V_2=0} = i_{nb}
\]

\[
I_{n2} = -I_2 |_{V_1=V_2=0} = i_{nc}
\]
The admittance formalism y-parameters are defined as:

\[ I_1 = y_{11}V_1 + y_{12}V_2 \]
\[ I_2 = y_{21}V_1 + y_{22}V_2 \]
$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0} = s \left( C_{be} + C_{\mu} \right)$

$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0} = -sC_{\mu}$

$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0} = g_m - sC_{\mu}$

$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0} = s \left( C_2 + C_{\mu} \right)$

Transforming $I_{n1}$ and $I_{n2}$ into input referred sources $I_A$ and $V_A$:

$V_A = -I_{n2} y_{21} = -i_{nc}$

$I_A = I_{n1} - I_{n2} y_{11}/y_{21} = i_{nb} - i_{nc} y_{11}/y_{21}$

As an additional step, the mean squared noise and cross correlation between $V_A$ and $I_A$ is given by:

$$V_A^2 = V_A V_A^* = \frac{\overline{i_{nc}^2}}{|y_{21}|^2} \quad (4.4)$$

$$I_A^2 = I_A I_A^* = \frac{\overline{i_{nb}^2}}{|y_{21}|^2} + \frac{\overline{i_{nc}^2}}{|y_{21}|^2} |y_{11}|^2 - 2 \text{Re} \left[ \langle i_{nb} i_{nc}^* \rangle \frac{y_{11}^*}{y_{21}^*} \right] \quad (4.5)$$

$$V_A^* I_A = -\langle i_{nb} i_{nc}^* \rangle \frac{y_{11}}{y_{21}} + \frac{\overline{i_{nc}^2}}{|y_{21}|^2} \frac{y_{11}}{|y_{21}|^2} \quad (4.6)$$

### 4.2.2 Equivalent Noise Sources $V_{A2}$ and $I_{A2}$

The intention is to evaluate $V_{A2}$ and $I_{A2}$ to include $C_{1ext}$ in the two-port network. This is accomplished by equating the short-circuit currents and open-circuit voltages of the two circuits in Figure 4.3 and 4.3.

(A) Short circuit inputs and outputs of both circuits in Figure 4.3:

Circuit 1: $I_{SC1} = I_2|_{V_2=0} = y_{21} V_1 = y_{21} V_A \quad (4.7)$

Circuit 2: $I_{SC2} = I_2|_{V_2=0} = y_{21} V_1 = y_{21} V_{A2} \quad (4.8)$
(B) Open circuit inputs and outputs of both circuits in Figure 4.3:

Circuit 1: use superposition on $V_A$ and $I_A$

$$V_{1,V_A} = \frac{y_{1e}}{y_{1e} + (y_{11} + y_{12})} V_A$$

$$V_{1,I_A} = \frac{1}{y_{1e} + (y_{11} + y_{12})} I_A$$

$$V_{ON1} = V_2|_{I_2=0} = \left. \frac{I_2 - y_{21} V_1}{y_{22}} \right|_{I_2=0} = \frac{-y_{21} V_1}{y_{22}} = -\frac{y_{21}}{y_{22}} (V_{1,V_A} + V_{1,I_A})$$

$$= -\frac{y_{21}}{y_{22}} \left[ \frac{1}{y_{1e} + (y_{11} + y_{12})} \right] (I_A + y_{1e} V_A)$$  \hspace{1cm} (4.9)

Circuit 2: $V_{A2}$ has no contribution to $I_{SC2}$ when input is open circuit.

$$V_1 = \frac{1}{y_{1e} + (y_{11} + y_{12})} I_{A2}$$

$$V_{ON2} = V_2|_{I_2=0} = -\frac{y_{21} V_1}{y_{22}} = -\frac{y_{21}}{y_{22}} \left[ \frac{1}{y_{1e} + (y_{11} + y_{12})} \right] I_{A2}$$  \hspace{1cm} (4.10)

(C) Setting $I_{SC1} = I_{SC2}$, i.e. combining Equations 4.7 and 4.8:

$$V_A = V_{A2}$$  \hspace{1cm} (4.11)

(D) Setting $V_{ON1} = V_{ON2}$, i.e. combining Equations 4.9 and 4.10:

$$I_{A2} = I_A + y_{1e} V_A$$  \hspace{1cm} (4.12)

$v_{nL}$ can now be directly added to $V_{A2}$. This is illustrated in Figure 4.6, resulting in a single voltage noise source $V_{A2L}$.  

Figure 4.6: Illustrating how $v_{nL}$ is embedded into $V_{A2L}$.

4.2.3 Mean Squared Equivalent Input Noise Voltage $V_{nEQ}^2$

The input noise voltage at the base of the bipolar transistor is found by superposition of $V_{A2L}$ and $I_{A2}$ in Figure 4.7. Before doing so, first let the two port network in Figure 4.7 be characterized by the following y-parameters, which is differentiated from previous y-parameters by the superscript symbol $^n$.

\[
y^n = \begin{bmatrix} y_{11}^n & y_{12}^n \\ y_{21}^n & y_{22}^n \end{bmatrix}
\]

\[
y_{11}^n = \left. \frac{I_1}{V_1} \right|_{V_2=0} = s(C_\mu + C_{be} + C_{1ext}) = s(C_\mu + C_1)
\]

\[
y_{12}^n = y_{12} = -sC_\mu
\]

\[
y_{21}^n = \left. \frac{I_2}{V_1} \right|_{V_2=0} = -sC_\mu
\]

\[
y_{22}^n = y_{22} = s(C_2 + C_\mu)
\]
Also, the inductor admittance is given by:

\[ y_L = (R + sL_B)^{-1} \]

(A) Using superposition, evaluate \( V_1 \) with only \( V_{A2L} \) and set \( I_{A2} = 0 \). This results in three equations with three unknown variables:

\[
\begin{align*}
V_1 &= \frac{I_1 - y_{12} V_2}{y_{11}'} \\
V_1 &= \frac{I_1 + y_{22} V_2}{-y_{21}'} \\
I_1 &= y_L (V_2 - V_1 + V_{A2L})
\end{align*}
\]

Solving for \( V_1 \) results in:

\[
V_{1, V_{A2L}} = \frac{y_{22} y_L (y_{12} + y_{22}) V_{A2L}}{\det[y^n] (y_{22} + y_L) + y_L (y_{21}' + y_{22}) (y_{12} + y_{22})}
\] (4.13)

(B) Continuing with superposition, evaluate \( V_1 \) with only \( I_{A2} \) and set \( V_{A2L} = 0 \). This
results in four equations with four unknown variables:

\[
\begin{align*}
V_1 &= \frac{I_1 - y_{12}V_2}{y_{11}^n} \\
V_1 &= \frac{I_2 - y_{22}V_2}{y_{21}^n} \\
I_1 &= I_{A2} + (V_2 - V_1) y_L \\
I_2 &= (V_1 - V_2) y_L
\end{align*}
\]

Solving for \(V_1\) results in:

\[
V_{1,I_{A2}} = \frac{(y_{22} + y_L) I_{A2}}{(y_L - y_{21}^n) (y_{12} - y_L) + (y_{11}^n + y_L) (y_{22} + y_L)}
\]

(C) Combining Equations 4.13 and 4.14 to find \(V_{n,\text{EQ}}\):

\[
V_{n,\text{EQ}} = V_{1,I_{A2}} + V_{1,V_{A2L}} = \frac{(y_{22} + y_L) I_{A2}}{(y_L - y_{21}^n) (y_{12} - y_L) + (y_{11}^n + y_L) (y_{22} + y_L)} + \frac{\det [y^n] (y_{22} + y_L) + y_L (y_{21}^n + y_{22}) (y_{12} + y_{22})}{y_{22} y_L (y_{12} + y_{22}) V_{A2L}} = I_{A2}X_1 + V_{A2L}X_2
\]

where \(X_1\) and \(X_2\) are functions of \(y\)-parameters and \(y_L\):

\[
\begin{align*}
X_1 &= \frac{y_{22} + y_L}{(y_L - y_{21}^n) (y_{12} - y_L) + (y_{11}^n + y_L) (y_{22} + y_L)} \\
X_2 &= \frac{y_{22} y_L (y_{12} + y_{22})}{\det [y^n] (y_{22} + y_L) + y_L (y_{21}^n + y_{22}) (y_{12} + y_{22})}
\end{align*}
\]
(D) The mean square equivalent input noise voltage ($V_{nEQ}^2$) is given by:

$$V_{nEQ}^2 = V_{nEQ}(V_{nEQ}^*) = |I_{A2}|^2 |X_1|^2 + |V_{A2L}^2| |X_2|^2 + 2\text{Re}(I_{A2}V_{A2L}^*X_1X_2^*)$$

Sub-in $V_{A2L} = V_A + v_{nL}$ (Equation 4.11) and $I_{A2} = I_A + y_{1ext}V_A$ (Equation 4.12):

$$V_{nEQ}^2 = \left(\frac{P_A^2}{V_A^2} + \frac{V_A^2}{V_{nL}^2}|y_{1ext}|^2 + 2\text{Re}[I_AV_A^*y_{1ext}^*]\right)|X_1|^2 + \left(\frac{V_A^2}{V_{nL}^2} + v_{nL}^2\right)|X_2|^2 + 2\text{Re}\left[I_AV_A^* + \frac{V_A^2}{V_{nL}^2}y_{1ext}\right](X_1X_2^*)$$

Sub-in equivalent noise source expressions (Equations 4.4, 4.5 and 4.6):

$$V_{nEQ}^2 = \frac{i_{nb}^2}{|y_{21}|^2} |X_1|^2 + \frac{v_{nL}^2}{|y_{21}|^2} |X_2|^2 + \frac{i_{nc}^2}{|y_{21}|^2} \left\{ |X_1|^2 \left[ |y_{11}|^2 + |y_{1ext}|^2 + 2\text{Re}(y_{11}y_{1ext}^*) \right] \right\} + 2\text{Re}\left[ (I_AV_A^* + \frac{V_A^2}{V_{nL}^2}y_{1ext}) (X_1X_2^*) \right] - 2\text{Re}\left( \frac{i_{nb}^*i_{nc}}{y_{21}^*} \right)(X_1X_2^*)$$

$$\text{(4.15)}$$

4.2.4 Output Phase Noise $S_{\Delta out}$

The input phase noise ($S_{\Delta in}$) is defined as:

$$S_{\Delta in} \triangleq 2 \left( \frac{\text{NoisePower}}{\text{OscillationPower}} \right) = 2 \frac{V_{nEQ}^2}{|V_{osc}|^2} \quad (4.16)$$

where the factor 2 is to account for both sidebands. Based on Leeson’s feedback model, the output phase noise ($S_{\Delta out}$) is given by Equation 4.17 [4,6].

$$S_{\Delta out}(\omega_m) = S_{\Delta in} \left( 1 + \frac{\omega^2}{4Q^2\omega_m^2} \right) \quad (4.17)$$
For a small frequency offset \( \omega_m \) from carrier, the phase noise is approximately:

\[
S_{\Delta_{out}} \approx S_{\Delta m} \left( \frac{\omega^2}{4\omega^2_m Q^2} \right) = \frac{V^2_{nEQ} \omega^2}{2 \left| V_{osc} \right|^2 \omega^2_m Q^2}
\]

Sub-in \( \frac{V^2_{nEQ}}{\omega^2_m Q^2} \) (Equation 4.15 into 4.18):

\[
S_{\Delta_{out}} = \frac{\omega^2}{2 \left| V_{osc} \right|^2 \omega^2_m Q^2} \left\{ \frac{i^2_{nb}}{i^2_L} \left| X_1 \right|^2 + \frac{i^2_n}{\left| y_{21} \right|^2} \left| X_2 \right|^2 \right. \\
+ \left. \left| y_{11} \right|^2 + \left| y_{1ext} \right|^2 + 2 \text{Re} \left( y_{11} y^*_{1ext} \right) \right\} \left\{ \left| y_{11} \right|^2 \left( y^*_{1ext} + y_{1ext} \right) X_1 X_2^* \right. \\
- \left. 2 \text{Re} \left( \frac{\left( y_{11} y^*_{1ext} \right)}{\left| y_{21} \right|^2} \left[ \left| y_{11} \right|^2 \left( y^*_{1ext} + y_{1ext} \right) X_1 X_2^* \right] \right) \right\}
\]

Equation 4.19 is the final solution for the output phase noise in the admittance formalism. Since the goal was to derive phase noise as a function of design parameters, let us recast \( S_{\Delta_{out}} \) as a function of: \( C_{1ext}, L_B, C_2, J_c, A_e, \omega \). By setting \( C_n=0 \) for simplicity, the y-parameters reduce to:

\[
y_{11} = sC_{be}, \quad y^*_{11} = s (C_{1ext} + C_{be}) = sC_1, \\
y_{12} = y^*_{12} = 0, \\
y_{21} = g_m, \quad y^*_{21} = 0, \\
y_{22} = y^*_{22} = sC_2, \\
\text{det} \left[ y^n \right] = y_{11} y^*_{22} - y_{12} y^*_{21} = s^2 C_1 C_2 \\
y_L = (R + sL)^{-1}, \quad y_{1ext} = sC_{1ext}
\]
Also, \( \omega \) and Q-factor can be expressed as:

\[
\omega^2 = \frac{C_1 + C_2}{L_B C_1 C_2} \quad Q = \frac{\omega L_B}{R}
\]

Substituting these parameters into Equation 4.19:

\[
S_{\Delta_{\text{out}}} = \frac{1}{2 \omega_m^2 |V_{\text{osc}}|^2 C_1^2 \left( \frac{C_1}{C_2} + 1 \right)^2} \left\{ \frac{\overline{v_{nL}}^2 \omega^2 C_1^2 + \overline{i_{nb}^2} (1 + \omega^2 R^2 C_1^2) + \frac{\overline{v_{nc}^2}}{g_m} \left[ \omega^4 R^4 C_1^4 \right]}{-2q^2 R C_1 \left( \omega RC_1 \text{Im} \left\langle i_{nb} i_{nc}^* \right\rangle + \text{Re} \left\langle i_{nb} i_{nc}^* \right\rangle \right) + q V_T^2 \left( C_j A_e + C_{1\text{ext}} \right) \left[ 1 + \omega^2 R^2 \left( C_j A_e + C_{1\text{ext}} \right)^2 \right] - 2q V_T \omega^2 R \times \left[ \omega R \left( C_j A_e + C_{1\text{ext}} \right) \sin (\omega \tau) + \cos (\omega \tau) - 1 \right] \right\}
\]

Finally, substituting expressions for transconductance, junction capacitance, shot noise, shot noise cross correlation and thermal noise sources results in the final phase noise formula (Expression 4.20).

\[
\overline{i_{nb}^2} = \frac{2q J_e A_e}{\beta} \quad \overline{i_{nc}^2} = 2q J_e A_e \quad \left\langle i_{nb} i_{nc}^* \right\rangle = 2q J_e A_e \left( e^{j\omega \tau} - 1 \right) \quad \overline{v_{nL}^2} = 4k T R \\
C_1 = C_{be} + C_{1\text{ext}} = C_j A_e + C_{1\text{ext}} \quad g_m = \frac{I_C}{V_T} = \frac{J_e A_e}{V_T}
\]

\[
S_{\Delta_{\text{out}}} = \frac{1}{\omega_m^2 |V_{\text{osc}}|^2 \left( \frac{C_j A_e + C_{1\text{ext}}}{C_2} + 1 \right)^2} \left( 2k T \omega^2 R + \frac{q J_e A_e}{\beta (C_j A_e + C_{1\text{ext}})^2} \left[ 1 + \omega^2 R^2 (C_j A_e + C_{1\text{ext}})^2 \right] + \frac{q^2 V_T^2 \omega^4 R^4 (C_j A_e + C_{1\text{ext}})^2}{J_e A_e} - 2q V_T \omega^2 R \times \left[ \omega R (C_j A_e + C_{1\text{ext}}) \sin (\omega \tau) + \cos (\omega \tau) - 1 \right] \right)
\]

(4.20)
Similar to Expression 4.2, this expression also indicates that phase noise diminishes with a large $C_1:C_2$ capacitance ratio.

### 4.2.5 Effect of Shot Noise Correlation on Phase Noise

Expression 4.20 reveals the importance of including shot noise correlation to have an accurate phase noise model at high frequencies. The correlation term,

$$
-\frac{2qV_T\omega^2 R}{\omega_m^2 |V_{osc}|^2 \left( \frac{C_j A_e + C_{1ext}}{C_2} + 1 \right)^2} \left[ \omega R (C_j A_e + C_{1ext}) \sin (\omega \tau) + \cos (\omega \tau) - 1 \right]
$$

acts to correct the phase noise by a magnitude that increases by a power of three with respect to the frequency of oscillation. This correlation of $i_{nb}^2$ and $i_{ne}^2$ is neglected in present bipolar models, and would explain the pessimistic results of Spectre phase noise simulations when compared to experimental results.

### 4.2.6 Optimal Current Density Bias

The optimal current density bias for lowest phase noise is simply found by evaluating:

$$
\frac{\partial S_{\Delta out}}{\partial J_c} = \frac{1}{\omega_m^2 |V_{osc}|^2 \left( \frac{C_j}{C_2} + 1 \right)^2} \left( \frac{qA_e}{\beta C_1^2} \left( 1 + \omega^2 R^2 C_1^2 \right) - \frac{qV_T^2 \omega^4 R^2 C_1^2}{J_c^2 A_e} \right) = 0
$$

$$
\frac{qA_e}{\beta C_1^2} \left( 1 + \omega^2 R^2 C_1^2 \right) = \frac{qV_T^2 \omega^4 R^2 C_1^2}{J_c^2 A_e}
$$

$$
J_c^2 = \frac{\beta \omega^4 V_T^2 R^2 C_1^4}{A_e^2 \left( 1 + \omega^2 R^2 C_1^2 \right)}
$$

$$
J_c = \frac{\beta^{0.5} \omega^2 V_T R C_1^2}{A_e \sqrt{1 + \omega^2 R^2 C_1^2}}
$$

Equation 4.21 is the solution for the optimal $J_c$ bias.
4.2.7 Tank Voltage Swing $V_{osc}$

The analysis begins by examining the large signal equivalent circuit in Figure 4.8. For large sinusoidal input voltages, the large signal transconductance ($G_m$) can be approximated by $\frac{2I_{DC}}{V_{osc}} \sin \omega t$ [5]. This approximation is based on the assumption that the current through the collector behaves as narrow pulses over time where each current pulse coincides with the maximum of the sinusoidal input voltage (Figure 4.9). Since the current waveform must have an average value equal to the bias current ($I_{DC}$),

$$\bar{i}_C = \frac{1}{T} \int_0^T i_D(t)dt = I_{DC}$$

From Fourier Series, $i_C$ has a fundamental amplitude given by,

$$|i_C| = \frac{2}{T} \int_0^T i_D(t) \cos \omega t dt$$

Recalling that $i_C$ consists of periodic narrow pulses coinciding with the maximum input, the cosine may be approximated by unity over the short pulse width. Thus,

$$|i_C| \approx \frac{2}{T} \int_0^T i_D(t) dt = 2I_{DC}$$

This large signal approximation increases in accuracy for larger signal swings [5].

![Figure 4.8: Large signal equivalent circuit of Colpitts oscillator.](image)
In the common-collector Colpitts topology, the tank voltage swing is located at the base node. To find the base voltage, Thevenin and Norton equivalent simplifications are applied to the current source \(2I_{DC}\), as illustrated in Figure 4.10. The first Thevenin/Norton transformation is to combine \(C_2\) in series with \(C_1\) into an equivalent capacitance \(C_{EQ}\). The second transformation places \(C_{EQ}\) into the equivalent RLC circuit of a Colpitts oscillator. At the LC-resonant frequency, the tank swing is simply the current multiplied by the equivalent parallel resistance of the resonant-tank \(R_p\).

For large values of inductor Q-factor, \(R_p\) can be approximated as:

\[
R_p \approx Q^2 R = \left(\frac{C_1 + C_2}{C_1 C_2 R}\right) L_B
\]

where \(R\) is the series resistance of the tank inductor \(L_B\). The tank swing becomes:

\[
V_{osc} = \frac{2I_{DC} L_B}{C_2 R}
\]  

(4.22)
Figure 4.10: A five step illustration of Thevenin and Norton transformation to find tank swing.
4.3 Phase Noise Analysis Using Simulations

Spectre simulations were performed on both single-ended and differential Colpitts oscillators to verify the following optimization techniques:

1. The existence of an optimal $J_c$ bias for lowest phase noise.
2. A smaller tank inductance ($L_B$) leads to lower phase noise.
3. The utilization of inductive emitter degeneration ($L_E$) improves linearity and phase noise.

Simulation schematics are shown in Figures 4.11 and 4.12. The load at the collector of the cascode transistor is a RLC resonant tank designed such that the voltage gain from the tank to output is between 0.75 and 1. To simplify matters, the cascode transistors are sized to be identical to the bottom negative resistance transistors, and the tank inductor ($L_B$) includes a series resistor ($R$) to model a finite $Q$-factor.

Simulations rely on Jazz Semiconductor’s SBC18HX 0.2-µm emitter width nominal npn models, and are run at 27°C. The simulated oscillators are targeted at 40 GHz to validate the design optimizations well into mm-wave frequencies.
Figure 4.11: Simulation circuit for single-ended Colpitts oscillator.

Figure 4.12: Simulation circuit for differential Colpitts oscillator.
4.3.1 Optimal $J_c$ Bias

By keeping the following design parameters constant, the effect of $J_c$ on phase noise can be isolated:

- $f_{osc} = 40$ GHz
- $V_{osc} = 2.5 \ V_{p-p}$
- $L_B = \text{fixed at } 200 \ \text{pH}, 100 \ \text{pH} \ or \ 50 \ \text{pH}$
- Q-factor of $L_B = 10$
- $L_E = 0 \ \text{pH}$
- Emitter Area ($A_e$) = constant in each tank inductance case

The variable parameters are:

- Current density $J_c$
- Capacitance Ratio, $C_1:C_2$ (adjusted for optimal phase noise)

The capacitance ratio must be adjusted for each $J_c$ value in order to hold the tank swing and oscillation frequency constant. Figure 4.13 shows phase noise versus $J_c$ for three different single-ended oscillator designs ($L_B = 200 \ \text{pH}, 100 \ \text{pH}, \ and \ 50 \ \text{pH}$). Also included is the $NF_{min}$ of the cascode at 40-GHz (dashed-line) which is plotted as a dashed-line. Each data point represents a 40-GHz single-ended Colpitts oscillator that has been optimized for phase noise given a certain $J_c$ and $L_B$. This plot supports the existence of an optimal $J_c$ bias, which is identical in all three $L_B$ cases. This optimum falls inline with the optimal $NF_{min}$ bias of the cascode, as indicated by the arrow. The optimal $NF_{min}$ bias point can be interpreted as a balance between the thermal noise of the base and emitter resistors that dominates at low $J_c$, and the shot-noise that dominates at high $J_c$. The conclusion from this experiment is to bias transistors at optimal $NF_{min}$ of cascode for lowest phase noise.
4.3.2 Optimal $L_B$ and $A_e$

To isolate the effect of $A_e$ and $L_B$, the following parameters are kept constant:

- $f_{osc} = 40$ GHz
- $V_{osc} = 2.5$ $V_{p-p}$
- Q-factor of $L_B = 10$
- $L_E = 0$ pH, $L_{EE} = 440$ pH (ideal inductor)
- $J_c = \text{optimal } NF_{\text{min}} \text{ bias of cascode}$
- $C_{\text{tail}} = 500$ fF

The variable parameters are:

- $L_B$
• $A_e$

• Capacitance ratio $C_1:C_2$ (adjusted for optimal phase noise)

The results are plotted in Figure 4.14, where each data point represents a 40-GHz oscillator completely optimized for best phase noise given a certain $L_B$ and $A_e$. It verifies that the lowest phase noise design is achieved when $L_B$ is minimized and bias current is maximized. This holds true in both single-ended and differential topologies. The amount of phase noise improvement is approximately 2-3 dB when $L_B$ and $A_e$ are scaled by a factor of two. In conclusion, this experiment shows that the best phase noise results are accomplished using the smallest reproducible tank inductor.

Figure 4.14: Phase noise versus $A_e$ over 3 different cases of $L_B$ for both single-ended and differential oscillators.
4.3.3 Optimal $L_E$

To isolate the effect of $L_E$, the following parameters are kept constant:

- $f_{osc} = 40$ GHz
- $V_{osc} = 2.5 \, V_{p-p}$
- $L_B$ = fixed at 200 pH, 100 pH or 50 pH
- Q-factor of $L_B$ = 10
- $L_{EE} = 440$ pH (ideal inductor)
- $J_c$ = optimal $NF_{\min}$ bias of cascode
- Q-factor of $L_E$ = infinite (ideal inductor)
- $A_e$ = constant in each tank inductance case
- $C_{tail} = 500$ fF

The variable parameters are:

- $L_E$
- Capacitance ratio $C_1:C_2$ (adjusted for optimal phase noise)

Figure 4.15 plots the phase noise of the differential oscillator versus $L_E$. Improvement in phase noise is approximately 5-6 dB per 100 pH of $L_E$. The size of $L_E$ is bounded by Conditions 4.23 and 4.24, which are derived in Appendix A.

$$\omega_{osc} > \frac{1}{\sqrt{L_{EE}C_2}}$$  \hspace{1cm} (4.23)

$$\omega_{osc} < \frac{1}{\sqrt{C_2 \left( \frac{L_EL_{EE}}{L_E+L_{EE}} \right)}}$$  \hspace{1cm} (4.24)
4.4 Varactor Design

The two most important goals to consider when designing the varactor are, 1) high Q-factor and 2) large tunable capacitance range. At microwave frequencies, it is typically the integrated inductor that limits the tank Q-factor, but this assumption no longer holds true at mm-wave frequencies where the inductor Q-factor surpasses that of the varactor [20]. The second criterion results in a widely tunable frequency which improves manufacturability.

Increasing the Q-factor of an AMOS varactor involves reducing the ohmic losses in the gate and channel. The gate resistance decreases with smaller gate finger widths,
$W_f$, and greater number of parallel fingers, $N_f$:

$$R_G = \frac{R_{Gsq} W_f}{3 N_f l_g} + \frac{R_{con}}{N_{con} N_f}$$  \hspace{1cm} (4.25)

$R_{Gsq}$ is the sheet resistance of the polysilicon gate, $R_{con}$ is the resistance per contact and $N_{con}$ is the number of contacts. The channel resistance decreases with shorter gate finger lengths $l_g$. Although smaller varactors will undoubtedly have smaller capacitances leading to higher Q-factors, there is a lower boundary on the size. This limitation is associated with the overlap capacitance between the gate and the source/drain regions resulting in reduced effective variable capacitance. Thus, the best design procedure is to first use minimum gate finger widths and lengths, then scale the number of fingers to attain the target capacitance and tuning range. Figure 4.16 illustrates the parasitics under consideration.

![Cross section of accumulation-mode nMOS varactor illustrating device parasitics.](image)

Figure 4.16: Cross section of accumulation-mode nMOS varactor illustrating device parasitics.
4.5 Systematic Design Methodology

This methodology applies to both fundamental and push-push VCOs.

Step 1. Set the tank voltage swing \( V_{osc} \) to the maximum allowable value for safe transistor operation. \( V_{osc} \) is SET. Doing so simultaneously minimizes phase noise and maximizes output power.

Step 2. Bias transistors at the minimum noise figure current density of the cascode amplifier. \( J_c \) is SET.

Step 3. Select the smallest reproducible tank inductance \( L_B \), and design it to have the highest possible Q-factor at \( f_{osc} \). \( L_B \) is SET. Doing so also sets the equivalent capacitance \( C_{eq} \) for a constant \( f_{osc} \).

\[
C_{eq} \approx \frac{1}{(2\pi f_{osc})^2 L_B}
\]

Step 4. Design varactor for high Q-factor and adequate tuning range. Then set \( C_2 \) as the middle of the tunable capacitance range, taking care that \( C_2 \) must be greater than \( C_{eq} \). \( C_2 \) is SET. Based on equation 4.22, \( A_e \) is SET.

\[
A_e = \frac{R_s C_2 V_{osc}}{2 J_c L_B}
\]

Based on \( C_{eq} \), the external capacitor \( C_{1ext} \) is SET.

\[
C_1 = C_j A_e + C_{1ext} = \frac{C_{eq} C_2}{C_2 - C_{eq}}
\]

\[
C_{1ext} = \frac{C_{eq} C_2}{C_2 - C_{eq}} - C_j A_e
\]

Step 5. Add emitter degeneration inductor \( L_E \).
Chapter 5

Experimental Results

5.1 Process Technology

All circuits were fabricated in Jazz Semiconductor’s commercially available SBC18 BiCMOS process. The base width of the featured SiGe HBTs was 0.2 $\mu$m with a measured $f_T$ and $f_{MAX}$ near 155 GHz for this particular batch of wafers (Figure 5.1). The npn HBTs have a collector-emitter breakdown voltage ($BV_{CEO}$) of approximately 1.8 V, and a minimum noise figure near 3.5 dB at 35 GHz and 5.5 dB at 60 GHz (Figure 5.2). This process offered 6 metal layers with the topmost two metals being suitable for RF applications [26].
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Figure 5.1: Measured and Simulated $f_T$ and $f_{MAX}$ of a 2 x 0.2 µm x 3 µm SiGe HBT.

Figure 5.2: Measured and Simulated $NF_{min}$ at 35 GHz and 60 GHz of a 2 x 0.2 µm x 3 µm SiGe HBT.
5.2 Die Photographs

Photos of the test circuits are shown in Figures 5.3 to 5.5. The extensive use of multi-turn spiral inductors allowed for very compact dimensions. The area consumption, including all pads, of the 35-GHz, 60-GHz, 70-GHz, and 120-GHz VCO test structures is 525 x 475 $\mu m^2$, 485 x 475 $\mu m^2$, 420 x 450 $\mu m^2$, and 450 x 375 $\mu m^2$, respectively.

Figure 5.3: Photograph of all 13 fabricated VCOs.
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Figure 5.4: Close up photograph of 60-GHz VCO operating on the fundamental.

Figure 5.5: Close up photograph of 120-GHz VCO operating on the second harmonic.
5.3 Varactor and Inductor Test Structures

Accumulation-mode n-MOS test structures with different gate finger widths and lengths were fabricated and measured to examine the varactor Q-V and C-V characteristics. The measurement results plotted in Figure 5.6 illustrate that the highest Q-factor varactor is attained when the minimum gate finger length and width are used. Figure 5.7 shows that the best-case Q-factor varactor is still capable of achieving a capacitance ratio of approximately 2.2 when gate lengths and widths are minimized. The varactor Q-factor is comparable to that of the on-wafer measured Q-factor of the multi-turn 80-pH inductor (Figure 5.8) employed in the 35-GHz fundamental-mode VCOs and the 70-GHz push-push VCO.

Figure 5.6: Measured worst-case bias varactor Q-factor at 40 GHz versus gate finger width and length.
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Figure 5.7: Q-V and C-V characteristics of optimized varactor. Gate length = 0.18 \( \mu m \), gate width = 1.0 \( \mu m \), gate finger count = 10.

Figure 5.8: Effective Inductance and Q-factor characteristics of 80-pH multi-turn spiral inductor.
5.4 VCO Measurement Setup

Each VCO was tested for output power, tuning range, and phase noise. The fundamental mode VCOs were measured using an Agilent E4448A power spectrum analyzer (PSA), an Agilent 11970V or 11970W waveguide harmonic mixer, 65-GHz DC blocking capacitors, a 50-ohm broadband termination load, and a HP 4352B VCO/PLL signal analyzer that was used as a low-noise DC power supply (Figure 5.9). A low-noise supply is crucial for reliable and repeatable phase noise measurements since any noise appearing on the varactor tuning node will be up converted around the carrier, thereby significantly increasing the observed phase noise. The measurement setup for a push-push VCO was similar to that of the fundamental mode with the exception that the output is biased through a 65-GHz bias-T (Figure 5.10).

![Diagram of measurement setup for 60-GHz VCO operating on the fundamental.](image)

During the time of testing, the available Anritsu network analyzer had a frequency range of 0 to 65 GHz. Thus, the losses in the cables, transitions, bias-Ts,
and DC blocking capacitors were only de-embedded up to 65-GHz and assumed constant for frequencies beyond. Therefore, the power measurements for the 70-GHz and 120-GHz VCOs are pessimistic since the setup components would realistically have greater losses at higher frequencies. Additionally, the external mixer conversion losses provided by Agilent were only effective up to 110 GHz, further adding to the inaccuracy of the 120-GHz VCO results.

5.5 VCO Measurements

This section presents measured phase noise, output power, and frequency tuning ranges of each of the 13 VCOs:

- eight 35-GHz VCOs operating on the fundamental
- two 60-GHz VCOs operating on the fundamental
• one 70-GHz VCO operating on the second harmonic
• two 120-GHz VCOs operating on the second harmonic

The objective was to evaluate the following five effects on phase noise, tuning range, and output power:

a) bias current
b) tank inductor
c) inductive emitter degeneration
d) scaling up the frequency of oscillation
e) operation on the 2nd harmonic

5.5.1 35 GHz fundamental mode VCOs

There are eight variations of the differential Colpitts topology to investigate the following:

(i) Phase-noise degradation due to lower varactor Q-factor when compared to a high Q-factor MIM fixed capacitor.

(ii) The scaling of $L_B$ and bias current on phase noise.

(iii) The effect of $L_E$ on phase noise.

Tables 5.1 and 5.2 lists the design variation and measured results of each VCO. The only difference between the four fixed frequency oscillators and the four VCO counterparts is the replacement of the MIM capacitor with an accumulation-mode n-MOS varactor.

The measured output power is the single-ended output power across 50-ohms. An example of the tuning characteristics and output power of one of the 35-GHz VCO
Table 5.1: List of fabricated 35-GHz fixed frequency oscillators with measured results.

<table>
<thead>
<tr>
<th>Osc. Design</th>
<th>$L_B$ (pH)</th>
<th>$L_E$ (pH)</th>
<th>$f_{osc}$ (GHz)</th>
<th>$V_{DD}$ (V)</th>
<th>$P_{DC}$ (mW)</th>
<th>$P_{OUT}$ (dBm)</th>
<th>$L{1 \text{ MHz}}$ (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>120</td>
<td>34.2</td>
<td>4.3</td>
<td>210</td>
<td>+2</td>
<td>-112.7</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>40</td>
<td>33.8</td>
<td>4.0</td>
<td>160</td>
<td>0</td>
<td>-110.5</td>
</tr>
<tr>
<td>3</td>
<td>200</td>
<td>120</td>
<td>34.3</td>
<td>4.0</td>
<td>121</td>
<td>-2</td>
<td>-109.0</td>
</tr>
<tr>
<td>4</td>
<td>200</td>
<td>40</td>
<td>33.9</td>
<td>4.3</td>
<td>142</td>
<td>-2</td>
<td>-108.4</td>
</tr>
</tbody>
</table>

Table 5.2: List of fabricated 35-GHz VCOs with measured results.

<table>
<thead>
<tr>
<th>VCO Design</th>
<th>$L_B$ (pH)</th>
<th>$L_E$ (pH)</th>
<th>Tuning Range</th>
<th>$V_{DD}$ (V)</th>
<th>$P_{DC}$ (mW)</th>
<th>$P_{OUT}$ (dBm)</th>
<th>$L{1 \text{ MHz}}$ (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>100</td>
<td>120</td>
<td>19.2 %</td>
<td>4.5</td>
<td>189</td>
<td>+1</td>
<td>-110.3</td>
</tr>
<tr>
<td>6</td>
<td>100</td>
<td>40</td>
<td>18.1 %</td>
<td>4.0</td>
<td>140</td>
<td>0</td>
<td>-109.3</td>
</tr>
<tr>
<td>7</td>
<td>200</td>
<td>120</td>
<td>15.1 %</td>
<td>4.1</td>
<td>127</td>
<td>-2</td>
<td>-107.9</td>
</tr>
<tr>
<td>8</td>
<td>200</td>
<td>40</td>
<td>16.9 %</td>
<td>4.0</td>
<td>120</td>
<td>-3</td>
<td>-105.0</td>
</tr>
</tbody>
</table>

$(L_B=100 \text{ pH}, \ L_E=120 \text{ pH})$ is shown in Figure 5.11. Averaged spectral plots of the lowest phase noise oscillator and VCO are shown in Figure 5.12.
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Figure 5.11: Measured frequency tuning range and output power characteristics of 35-GHz VCO.

Figure 5.12: Averaged spectral plots of a) oscillator design #1: $L_B=100\, \text{pH}, L_E=120\, \text{pH}$, b) VCO design #5: $L_B=100\, \text{pH}, L_E=120\, \text{pH}$. 
5.5.2 60 GHz fundamental mode VCOs

Two 60-GHz VCOs, one with a varactor and the other with a MIM capacitor were implemented to analyze the effects of scaling the differential Colpitts topology from 35 GHz to 60 GHz. The VCO design parameters and measured results are listed in Table 5.3. The phase noise at 1-MHz offset varies between -95 dBc/Hz and -103 dBc/Hz while the output power remains relatively constant between -1 and +1 dBm over the entire tuning range (Figure 5.14). The phase noise is observed to be highest when the gain of the VCO (\(\frac{df_{osc}}{\Delta V_{tune}}\)) is greatest, and lowest near the tuning limits where the gain is at a minimum. This behavior is associated with the noise on the tuning voltage, which contributes substantial phase noise when the gain of the VCO is high. At the tuning limits, the noise on the tuning voltage is less influential, and the VCO phase noise drops below -100 dBc/Hz reaching a minimum of -103.1 dBc/Hz, a value comparable to the fixed frequency phase noise of -104 dBc/Hz. Therefore, under these conditions the varactor only reduces the phase noise by approximately 1dB.

<table>
<thead>
<tr>
<th>(C_2)</th>
<th>(L_B) (pH)</th>
<th>(L_E) (pH)</th>
<th>(V_{DD}) (V)</th>
<th>(P_{DC}) (mW)</th>
<th>(P_{OUT}) (dBm)</th>
<th>Tuning Range or (f_{osc})</th>
<th>(L{1 \text{ MHz}}) (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIM Cap.</td>
<td>50</td>
<td>70</td>
<td>4.0</td>
<td>245</td>
<td>+1</td>
<td>59.4 GHz</td>
<td>-104.0</td>
</tr>
<tr>
<td>Varactor</td>
<td>50</td>
<td>70</td>
<td>4.0</td>
<td>245</td>
<td>+1</td>
<td>13 %</td>
<td>-103.1</td>
</tr>
</tbody>
</table>

Table 5.3: List of fabricated 60-GHz VCOs with measured results.

Measurements taken over a range of temperatures provide further information about the effective tuning range of the VCO. After temperature variations, the effective tuning range is only 8.2%, which is insufficient for a 60 GHz radio (Figure 5.15). In addition to this 8.2% tuning range, another 10% is needed to safely cover process variations. Therefore, a practical robust VCO design requires at least a 20-25% tuning range.
5.5.3 Phase Noise: Simulation versus Experimental

This section presents a comparison between all fundamental mode oscillator measurements and simulations to better illustrate the impact of base inductance, bias current, inductive emitter degeneration, and oscillation frequency on phase noise. Each data point in Figure 5.16 represents a 35-GHz or 60-GHz oscillator that has been completely optimized for a specific base inductance according to the presented systematic design methodology.

The measured data of 35-GHz oscillators is in good agreement with simulations as both validate the use of the smallest $L_B$ in conjunction with large bias currents to achieve the lowest phase noise. Both measured and simulated phase noise data show a phase noise improvement of approximately 2 to 3 dB each time $L_B$ and the bias current is scaled by a factor of two.

For each base inductance, oscillators with and without inductive emitter degeneration are simulated and measured. In both cases, the addition of $L_E$ improved phase noise by 3 to 4 dB according to measurements, and by 0.5 to 1 dB according to
simulations. Also included is the 60-GHz oscillator data, in which a two-fold increase in oscillation frequency increases the phase noise by approximately 12 dB (according to simulations). 6 dB increase is associated with the increase in frequency, and the other 6 dB is due to a higher transistor noise figure and a lower tank Q-factor.

5.5.4 Push-Push VCOs

Figure 5.17 reproduces the measured tuning range of the 70-GHz and 120-GHz push-push VCOs of 15 GHz (21%) and 10 GHz (8.5%), respectively. The 70-GHz VCO output power reaches -14 dBm with a phase noise of -94 dBc/Hz (Figure 5.18). The 120-GHz VCO spectrum shows an output power of -29.6 dBm, but recall that these values are pessimistic because losses are only de-embedded up to 65 GHz. The 70-GHz and 120-GHz VCOs operate from 4 V power supplies and consumes 128 mW and 200 mW of power, respectively. Phase noise was not measured on 120-GHz VCO because it was very poor (> -70 dBc/Hz @ 1MHz offset).
Figure 5.15: Effective tuning range of 60-GHz VCO after temperature variation.

Figure 5.16: Simulation and measurement results exploring lowest phase noise oscillator design space.
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Figure 5.17: Tuning ranges of 70-GHz and 120-GHz push-push VCOs.

Figure 5.18: a) 70-GHz VCO averaged spectral plot, b) 120-GHz VCO spectral plot.
5.6 Summary and Comparison

Table 5.6 summarizes and compares the work in this thesis to previously reported mm-wave fully integrated VCOs fabricated in a silicon-based process. Some references may have a superscript symbol $^2$ to indicate that it is a 2$^{nd}$ harmonic VCO. The figure of merit (FOM) is defined by Equation 5.1, which does not account for tuning range.

$$FOM = L \{f_{offset}\} - 20 \log \left(\frac{f_{osc}}{f_{offset}}\right) + 10 \log \left(\frac{P_{DC}}{P_{OUT}}\right)$$  \hspace{1cm} (5.1)

<table>
<thead>
<tr>
<th>Reference VCO</th>
<th>$f_{osc}$ (GHz)</th>
<th>$L(f_{offset})$ (dBc/Hz)</th>
<th>$V_{DD}$ (V)</th>
<th>Tuning Range</th>
<th>$P_{DC}$ (mW)</th>
<th>$P_{OUT}$ (dBm)</th>
<th>FOM</th>
<th>Technology $(f_T/f_{MAX})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[20] Colpitts</td>
<td>26</td>
<td>-87 @100 kHz</td>
<td>5.0</td>
<td>15%</td>
<td>75</td>
<td>1.0</td>
<td>-177.5</td>
<td>40/50 GHz (BJT)</td>
</tr>
<tr>
<td>[27] Colpitts</td>
<td>36</td>
<td>-105 @2 MHz</td>
<td>4.0</td>
<td>7%</td>
<td>84.0</td>
<td>-11.0</td>
<td>-160.0</td>
<td>70/100 GHz (HBT)</td>
</tr>
<tr>
<td>[13] X-coupled</td>
<td>40</td>
<td>-97 @1 MHz</td>
<td>1.5</td>
<td>15%</td>
<td>17.5</td>
<td>-5.0</td>
<td>-171.7</td>
<td>0.13 µm SOI CMOS</td>
</tr>
<tr>
<td>[18] Colpitts</td>
<td>43</td>
<td>-110 @1 MHz</td>
<td>-6.3</td>
<td>20%</td>
<td>280</td>
<td>6.5</td>
<td>-184.7</td>
<td>75 GHz (HBT)</td>
</tr>
<tr>
<td>[28] X-coupled</td>
<td>44</td>
<td>-90 @1 MHz</td>
<td>1.0</td>
<td>4%</td>
<td>14.0</td>
<td>-16.5</td>
<td>-154.7</td>
<td>0.13 µm CMOS</td>
</tr>
<tr>
<td>[29] X-coupled</td>
<td>44</td>
<td>-102 @1 MHz</td>
<td>1.5</td>
<td>10%</td>
<td>7.5</td>
<td>-6.0</td>
<td>-179.9</td>
<td>0.12 µm SOI CMOS</td>
</tr>
<tr>
<td>[30] X-coupled</td>
<td>50</td>
<td>-100 @1 MHz</td>
<td>1.3</td>
<td>2%</td>
<td>13.0</td>
<td>-9.5</td>
<td>-173.3</td>
<td>0.25 µm CMOS</td>
</tr>
<tr>
<td>[31] X-coupled</td>
<td>51</td>
<td>-85 @1 MHz</td>
<td>1.0</td>
<td>1%</td>
<td>1.0</td>
<td>-27.0</td>
<td>-152.2</td>
<td>0.12 µm CMOS</td>
</tr>
<tr>
<td>[14] X-coupled</td>
<td>60</td>
<td>-92 @1 MHz</td>
<td>1.5</td>
<td>14%</td>
<td>21.0</td>
<td>-3.8</td>
<td>-170.5</td>
<td>0.09 µm SOI CMOS</td>
</tr>
<tr>
<td>[19] Colpitts</td>
<td>77</td>
<td>-95 @1 MHz</td>
<td>-5.5</td>
<td>6%</td>
<td>930</td>
<td>14.3</td>
<td>-177.3</td>
<td>150/180 GHz (HBT)</td>
</tr>
<tr>
<td>[23]$^2$X-coupled</td>
<td>63</td>
<td>-85 @1 MHz</td>
<td>1.8</td>
<td>4%</td>
<td>119</td>
<td>-4.0</td>
<td>-156.2</td>
<td>0.25 µm CMOS</td>
</tr>
<tr>
<td>[10]$^2$ Colpitts</td>
<td>114</td>
<td>-108 @10 MHz</td>
<td>1.2</td>
<td>1%</td>
<td>8.4</td>
<td>-22.5</td>
<td>-157.0</td>
<td>0.13 µm CMOS</td>
</tr>
<tr>
<td>[11]$^2$ Colpitts</td>
<td>150</td>
<td>-85 @1 MHz</td>
<td>-6.5</td>
<td>25%</td>
<td>170</td>
<td>-5.0</td>
<td>-161.2</td>
<td>220 GHz (HBT)</td>
</tr>
</tbody>
</table>

This Work:

| 35-GHz Osc. | -112.7 @1 MHz | 4.3 | N/A | 193 | 4.0 | -184.5 | 155 GHz (HBT) |
| 35-GHz VCO  | -110.3 @1 MHz | 4.5 | 19% | 188 | 4.0 | -181.4 | 155 GHz (HBT) |
| 60-GHz Osc. | -104 @1 MHz  | 4.0 | N/A | 188 | 4.0 | -179.5 | 155 GHz (HBT) |
| 60-GHz VCO  | -103 @1 MHz  | 4.0 | 13% | 240 | 4.0 | -176.8 | 155 GHz (HBT) |
| 70-GHz VCO* | -94 @1 MHz   | 4.0 | 21% | 128 | >-14 | <-156.8 | 155 GHz (HBT) |
| 120-GHz VCO* | N/A           | 4.0 | 7%  | 200 | >-30 | N/A     | 155 GHz (HBT) |

Table 5.4: Comparison of Silicon-based monolithic mm-wave VCOs and oscillators.
Chapter 6

Conclusion

6.1 Summary

This thesis presented an algorithmic design methodology for lowest phase noise and wide tuning VCOs based on a comprehensive study of mm-wave SiGe HBT VCOs that included analytical phase noise derivations validated over 13 fabricated test circuits.

The study began by comparing the merits of the most popular VCO topologies. The fastest and most robust topology was decidedly the differential Colpitts described in Chapters 2 & 3. Based on a bipolar implementation, an expression for phase noise was analytically derived to include noise correlation. It was shown that phase noise improves when noise correlation is taken into account, especially at higher frequencies. This led to the VCO design methodology in Chapter 4, which was verified by way of Cadence Spectre simulations.

The investigation of mm-wave SiGe HBT VCO design demonstrated that phase noise improvement can only be achieved at the expense of increased bias current and reduced tank inductance. In regards to circuit techniques, inductive degeneration was experimentally found to improve phase noise by 3-4 dB with negligible impact on the tuning range and output power. Measured and simulated phase noise were in good
agreement, but simulations were slightly pessimistic because noise correlation is not captured in present bipolar models.

The feasibility of AMOS varactors and multi-turn spiral inductors has been successfully demonstrated in a novel push-push 120 GHz VCO, with a maximum frequency of 122 GHz. In the 35-GHz and 60-GHz VCOs, the AMOS varactors degraded the phase noise by 1 to 3.5 dB when compared to high Q-factor MIM capacitors. This validates the effectiveness of AMOS varactors in attaining wide tuning ranges with low phase noise.

At the expense of reduced output power, the 70-GHz push-push design exhibited a 50% larger tuning range than that of the fundamental 60-GHz VCO.

6.2 Future Work

Initially, this study intended to compare the differential Colpitts topology against the cross-coupled, but due to tight foundry deadlines, there was insufficient time to implement cross-coupled test circuits. An investigation of the cross-coupled topology would complement this work nicely, together providing a full understanding of integrated mm-wave VCOs.

The accuracy of the analytical phase noise expressions in this thesis can be improved by substituting the more complete bipolar model shown in Figure 3.1, which captures the base and emitter resistances. Doing so would allow a circuit designer to reasonably predict the best phase noise possible from any given process.

To the best of the author’s knowledge, there is no analytical phase noise expression for a harmonic VCO. Even the Cadence Spectre simulator lacks the functionality to properly simulate the phase noise at the output node of a 2nd harmonic VCO. If push-push VCOs are to make the transition from the research lab into commercial products, a rigorous analysis of the phase noise in harmonic VCOs is necessary.
References


REFERENCES


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Appendix A

Limitations on $L_E$ and $L_{EE}$

The following is a detailed derivation of the constraints on $L_E$ and $L_{EE}$, which were briefly demonstrated by H. Li and H.-M. Rein [18].

Given that the impedance $Z_{EMIT}$ must be capacitive in order to have negative resistance (Figure A.1), the derivation of $Z_{EMIT}$ is as follows:

![Figure A.1: Equivalent half circuit of a differential Colpitts oscillator.](image-url)
\[ Z_{\text{EMIT}} = sL_E + \left( \frac{1}{sL_{EE}} + sC_2 \right)^{-1} \]

\[ = sL_E + \frac{sL_{EE}}{1 + s^2L_{EE}C_2} \]

\[ = \frac{s(L_E + L_{EE}) + s^3L_EL_{EE}C_2}{1 + s^2L_{EE}C_2} \]

\[ = \frac{j\omega(L_E + L_{EE}) - j\omega_{osc}^3L_EL_{EE}C_2}{1 - \omega_{osc}^2L_{EE}C_2} \]

Let \( Z_{\text{EMIT}} = \frac{-j}{\omega_{osc}C_{eff}} \), where \( C_{eff} \) is the effective capacitance looking down into \( L_E \).

\[ \frac{-j}{\omega_{osc}C_{eff}} = \frac{-j}{\omega_{osc}} \left[ \frac{\omega_{osc}^2(L_E + L_{EE}) - \omega_{osc}^4L_EL_{EE}C_2}{\omega_{osc}^2L_{EE}C_2 - 1} \right] \]

\[ C_{eff} = \frac{\omega_{osc}^2L_{EE}C_2 - 1}{\omega_{osc}^2(L_E + L_{EE}) - \omega_{osc}^4L_EL_{EE}C_2} \] (A.1)

The effective capacitance must be positive in order for the transistor to provide negative resistance. This condition is true when the numerator and denominator are both positive.

Case 1: Numerator of equation A.1 > 0

\[ \omega_{osc}^2L_{EE}C_2 - 1 > 0 \]

\[ \omega_{osc}^2 > \frac{1}{L_{EE}C_2} \]

\[ \omega_{osc} > \frac{1}{\sqrt{L_{EE}C_2}} \] (A.2)

Condition A.2 implies that the \( L_{EE} \) and \( C_2 \) network must resonate at a frequency less than the resonant tank of the oscillator. That is, \( f_{\text{L}_{EE}||C_2} < f_{\text{osc,Colpitts}} \), where

\[ f_{\text{osc,Colpitts}} = \frac{\sqrt{C_1 + C_{eff}}}{2\pi \sqrt{L_B C_1 C_{eff}}} \]. This places a lower limit on the size of \( L_{EE} \).
APPENDIX A. LIMITATIONS ON $L_E$ AND $L_{EE}$

Case 2: denominator of equation A.1 > 0

\[
\omega_{osc}^2 (L_E + L_{EE}) - \omega_{osc}^4 L_EL_{EE}C_2 > 0
\]

\[
(L_E + L_{EE}) - \omega_{osc}^2 L_EL_{EE}C_2 > 0
\]

\[
\omega_{osc}^2 < \frac{L_E + L_{EE}}{L_EL_{EE}C_2}
\]

\[
\omega_{osc}^2 < \left[ C_2 \left( \frac{L_EL_{EE}}{L_E + L_{EE}} \right) \right]^{-1} = [C_2 (L_E || L_{EE})]^{-1}
\]

\[
\omega_{osc} < \frac{1}{\sqrt{C_2 \left( \frac{L_EL_{EE}}{L_E + L_{EE}} \right)}}
\]

(A.3)

Condition A.3 implies that the parallel network of $(L_E || L_{EE} || C_2)$ must resonate at a frequency greater than the resonant tank of the oscillator. That is: $f_{L_E || L_{EE} || C_2} > f_{osc, colpitts}$. This effectively places a upper limit on the value of $L_E$. 