Monday	
8:30 – 9:30	**Keynote I: Norm Rubin, AMD - GPU Evolution: Will Graphics Morph Into Compute?**
9:30 – 10:00	**Break**
10:00 – 12:00	**Session 1: Compilation** *Outer-Loop Vectorization - Revisited for Short SIMD Architectures,* Dorit Nuzman and Ayal Zaks *Redundancy Elimination Revisited,* Keith Cooper, Jason Eckhardt and Ken Kennedy *Exploiting the Reuse Supplied by Loop-Dependent Stream References in Stream Processors,* Ying Zhang, Jingling Xue, Ian Rogers, Xuejun Yang, Gen Li and Guibin Wang *Feature Selection and Policy Optimization for 3D Instruction Placement using Reinforcement Learning,* Katherine Coons, Behnam Robatmili, Matthew Taylor, Doug Burger and Kathryn McKinley
12:00 – 1:30	**Lunch**
1:30 – 3:00	**Session 2: CMP Architecture Design** *Core Cannibalization Architecture: Improving Lifetime Chip Performance for Multicore Processors in the Presence of Hard Faults,* Bogdan Romanescu and Daniel Sorin *Pangaea: A Tightly-Coupled IA32 Heterogeneous Chip Multiprocessor, Henry Wong, Anne Bracy, Ethan Schuchman, Tor Aamodt, Jamison Collins, Perry Wang, Gautham Chinya, Ankur Khandelwal Groen, Hong Jiang, and Hong Wang* *Skewed Redundancy,* Gordon Bell and Mikko Lipasti
3:00 – 3:30	**Break**
3:30 – 5:00	**Track 1: Session 3: Analyzing Applications** *The PARSEC Benchmark Suite: Characterization and Architectural Implications,* Christian Bienia, Sanjeev Kumar, Jaswinder Pal Singh and Kai Li *Visualizing Potential Parallelism in Sequential Programs,* Graham Price, John Giacomoni and Manish Vachharajani *Characterizing and Modeling the Behavior of Context Switch Misses,* Fang Liu, Fei Guo and Yan Solihin
	Track 2: Session 4: I/O Optimizations *MCAMP: Communication Optimization on Massively Parallel Machines with Hierarchical Scratch-pad Memory,* Hiroshige Hayashizaki, Yutaka Sugawara, Mary Inaba and Kei Hiraki *Profiler and Compiler Assisted Adaptive I/O Prefetching for Shared Storage Caches,* Seung Woo Son, Sai Prashanth Muralidhara, Ozcan Ozturk, Mahmut Kandemir, Ibrahim Kolcu and Mustafa Karakoy *Optimizing One-Sided Communication of Multiple Disjoint Memory Regions,* Costin Iancu

Tuesday	
8:30 – 9:30	**Keynote 2: Saman Amarasinghe, MIT - (How) Can Programmers Conquer the Multicore Menace?**
9:30 – 10:00	**Break**
10- 11:30	**Session 5: Multicore Memory Hierarchy Design (Part 1)** *Distributed Cooperative Caching*, Enric Herrero Abellanas, José González González and Ramon Canal Corretger *Scalable and Reliable Communication for Hardware Transactional Memory*, Seth Pugsley, Manu Awasthi, Niti Madan, Naveen Muralimanohar and Rajeev Balasubramonian *Improving Support for Locality and Fine-Grain Sharing in Chip Multiprocessors*, Hemayet Hossain, Sandhya Dwarkadas and Michael Huang
11:30 – 1:00	**Lunch**
1:00 – 2:30	**Session 6: Reconfigurable Architecture Optimization** *Edge-centric Modulo Scheduling for Coarse-Grained Reconfigurable Architectures*, Hyunchul Park, Kevin Fan, Scott Mahlke, Taewook Oh, Heeseok Kim and Hong-seok Kim *Chip multi-processor global power management with multi-optimization power-saving strategies*, Ke Meng and Russ Joseph *Multitasking Workload Scheduling on Flexible-Core Chip Multiprocessors*, Divya P. Gulati, Changkyu Kim, Simha Sethumadhavan, Stephen W. Keckler and Doug Burger
2:30 – 3:00	**Break**
3:00 – 4:30	**Session 7: Multicore Memory Hierarchy Design (Part 2)** *Leveraging On-Chip Networks for Cache Migration in Chip Multiprocessors*, Noel Eisley, Li-Shiuan Peh and Li Shang *Adaptive Insertion Policies for Managing Shared Caches on CMPs*, Aamer Jaleel, William Hasenplaugh, Moinuddin Qureshi, Julien Sebot, Simon Steely and Joel Emer *Analysis and Approximation of Optimal Co-Scheduling on Chip Multiprocessors*, Yunlian Jiang, Xipeng Shen, Jie Chen and Rahul Tripathi
4:-30 – 5:00	**Break**
5:00 – 6:00	**Session 8: Multithreading Improvements** *An Adaptive Resource Partitioning Algorithm for SMT Processors*, Huaping Wang, Israel Koren and C .Mani Krishna *Meeting Points: Using Thread Criticality to Adapt Multicore Hardware to Parallel Regions*, Qiong Cai, Jose Gonzalez, Ryan Rakvic, Grigorios Magklis, Pedro Chaparro and Antonio Gonzalez

Wednesday	
8:30 – 10:00	**Session 9: Middleware and Runtime Systems** *Prediction Models for Multi-dimensional Power-Performance Optimization on Many Cores*, Matthew Curtis-Maury, Ankur Shah, Filip Blagojevic, Dimitrios S. Nikolopoulos, Bronis R. de Supinski and Martin Schulz *Mars: A MapReduce Framework on Graphics Processors*, Bingsheng He, Wenbin Fang, Qiong Luo, Naga Govindaraju and Tuyong Wang *Multi-mode Energy Management for Multi-tier Server Clusters*, Tibor Horvath and Kevin Skadron
10:30 – 10:30	**Break**
10:30 – 12:00	**Session 10: Programming the Memory Hierarchy** *A Tuning Framework for Software-Managed Memory Hierarchies*, Manman Ren, Ji Young Park, Mike Houston, Alex Aiken and William Dally *Hybrid Access-Specific Software Cache Techniques for the Cell BE Architecture*, Marc Gonzalez, Nikola Vujic, Alexandre E. Eichenberger, Tong Chen, Xavier Martorell, Eduard Ayguada, Zehra Sura, Tao Zhang, Kevin O'Brien, and Kathryn O'Brien *COMIC: A Coherent Shared Memory Interface for Cell BE*, Jaejin Lee, Sangmin Seo, Chihun Kim, Junghyun Kim, Posung Chun, Zehra Sura, Jungwon Kim and SangYong Han