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| Lab 1: Common-Source Amplifiers |

Student Name: Click or tap here to enter text.

Student Number: Click or tap here to enter text.

Preparation

Fill in the following table:

Table 1: Hand analysis table

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| VDD (V) | Type | Gain | Swing (VPP) | VOV (V) | ID (A) | gm (A/V) | Vo (V) | RD (Ω) | Av (V/V) |
| 5.0 | NMOS | - | Max | Click or tap here to enter text. | 1m | Click or tap here to enter text. | Click or tap here to enter text. | Click or tap here to enter text. | Click or tap here to enter text. |
| 5.0 | PMOS | - | Max | Click or tap here to enter text. | 0.5m | Click or tap here to enter text. | Click or tap here to enter text. | Click or tap here to enter text. | Click or tap here to enter text. |
| 1.2 | NMOS | Max | 0.2 | Click or tap here to enter text. | 0.5m | Click or tap here to enter text. | Click or tap here to enter text. | Click or tap here to enter text. | Click or tap here to enter text. |

Hand in only this first page within 30 minutes of the start of the lab period.

Q1: MOS Input/Output Characteristics

1. **Single transistor DC sweep simulations**

With LTSpice, use the models given on the lab webpage, and build a single transistor circuit with an ALD1101 NMOS transistor with an ideal voltage source VG driving the gate and an ideal voltage source VD driving the drain and the source is grounded (do not forget to bias the bulk with the correct voltage). Let both VG and VD voltage sources have a default DC voltage of 1V.

1. Show your schematic.



1. Plot the drain current vs. drain voltage when sweeping VD from 0 to 3V and leaving VG fixed at 1V.



1. Plot the drain current vs. gate voltage when sweeping VG from 0 to 3V and leaving VD fixed at 1V.



1. **Transistor simple square law model**

The transistor models used in simulation are far more complicated and accurate than the simple square law used for hand analysis. Therefore, there is always some deviation between hand analysis and simulation results. In this section you will repeat the transistor DC sweep simulation using a simple square-law model to have an insight to accuracy of transistor models. For a feasible comparison you must put two models (model from lab webpage and square-law model) in parallel and plot drain currents of transistors in the same window.

1. Show your schematic.



1. Run and plot a dc simulation. Select plot window and Use *“Plot Settings 🡪 Notes & Annotations"* to annotate traces in the plot window (Placing texts and arrows ...).



Q2: Common-source Amplifier

In LTSpice, simulate the first two common-source amplifiers (NMOS \& PMOS) designed in the preparation.

1. Show your schematic.



1. Take a screen capture of the DC operating point simulation for the amplifiers. As mentioned before, some deviation from the hand analysis should not be a surprise. **MAKE SURE TO RELABLE NETS** so that your results can be interpretable by a TA.



1. Perform a DC sweep to plot VO, ID, and dVO/dVi = AV versus Vi in the same plot window. Vi should be swept from 0V to VDD. **ALSO:** label and comment on the plots to clearly show the small-signal gain AV, Vi, and output swing for the ID specified in Table 1.



**Do the following steps only for NMOS amplifier.**

1. In experimental practice, the input-output transfer curve of a circuit can be extracted by imposing a low frequency triangular signal to the input and and measuring the input (Vi) and output (VO) simultaneously using 2 of the input channels of the oscilloscope. Then the XY plot mode of the oscilloscope is enabled to plot VO versus Vi. To mimic this condition, perform a transient simulation. Set the input voltage source to generate a triangular wave with 0V to VDD swing at 100Hz. Set the simulation time to cover two periods of the triangular wave.
2. Plot Vi and VO vs. time.



1. Extract the XY transfer curve. Change the x-axis variable to Vi by right-clicking on it and editing *"Quantity Plotted"*.



1. Compare results with previous step.

Click or tap here to enter text.

1. Perform a transient simulation to show VO versus time. Use a sinusoidal voltage source at 1kHz with 10mVPP amplitude as the input source. Make sure that the input and thus the output are biased at the voltages found in the previous steps. Verify the small-signal gain found in the previous steps.



1. Repeat transient simulations for 100mVPP and 200mVPP input amplitude. Comment on results.
2. 100mVPP



1. 200mVPP



1. Comment on results.

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1. Now try to bias your amplifier using bias circuits shown in Figure 2 and tune the potentiometer for the input bias voltage found in the previous steps (use a 10uF capacitor and for potentiometer model follow Lab 0). Show your schematic.



1. Use a sinusoidal voltage source at 1kHz with 10 mVPP amplitude as the input source to your biased amplifier.
2. Plot Vi and transistor's gate voltage in the same window.



1. Plot VO to validate amplifier's gain.



1. Define an initial condition to set the gate voltage, VG=4V. Perform a transient simulation for 200ms and plot the gate voltage, VG, and output voltage, VO, versus time.



What causes the change in the waveforms?

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Q3: Two-stage Amplifier

Figure 4 shows a two stage amplifier which is implemented by cascading an NMOS common-source amplifier and a PMOS common-source amplifier, where VDD=3.3V and Vi=1.155V.

1. Show your schematic.



1. Perform a DC operating point simulation for the amplifier given below. Note the bias currents $ID1 and ID2.



1. Perform a DC sweep simulation to plot dVO/dVi (=AV) versus Vi. Vi should be swept from 0V to VDD. Note the maximum gain possible and corresponding Vi value.



1. Change the Vi DC value to the value found in the previous step (which corresponds to the maximum gain).
2. Perform a transient simulation to show VO versus time. Use a sinusoidal voltage source at 1kHz with 200mVPP amplitude as the input source.



1. Note the small-signal gain. Why it is not the same as the maximum gain?

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1. How much do you need to decrease the input sinusoidal voltage swing in order to obtain the maximum gain?

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1. This report is to be completed during the lab period by filling out this pre-made template and handed in within 30 minutes after the end of the session.