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| Lab 2: Current Mirrors |

Student Name: Click or tap here to enter text.

Student Number: Click or tap here to enter text.

Preparation

1. **Current mirrors**

Consider ID1=1mA and VDD=5V and using the device parameters shown in Table 1 (ignore the transistor's output impedance):

1. Calculate RB and VB for current mirrors in Figure 1. Show your hand calculations.



Final answer: Click or tap here to enter text.

1. For the cascoded current mirror in Figure 1(b), calculate VB2 wisely to maximize the output swing while keeping the transistors in saturation. Show your hand calculations.



Final answer: Click or tap here to enter text.

Hand in only the first two pages within 30 minutes of the start of the lab period.

Q1: Current Mirror

Do the following for both of the current mirrors in Figure 1. Use ID1=1mA and VDD=5V. For the cascoded current mirror, set VB2 wisely to maximize the output swing while keeping the transistors in saturation.

1. Use potentiometer model provided in Lab 0 in the current mirror circuit, set the total resistance to 5kΩ and define the ratio as a parameter *"val"*.
2. Show your schematic.



1. Perform a dc simulation with parametric sweep of *"val"* to bias ID1=1mA.



1. Compare achieved results for RB and VB with the preparation section.

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1. Run a DC sweep to plot ID2 versus VO. You need to connect a DC voltage source to the output of the current mirror to provide VO and sweep it.



1. Plot rout=1/(dIDS/dVO ). To do so, right-click on the plot window of previous step, select *"Add Traces"* (or *"Ctrl+A"*) and use following expression: "1/D(I(Mx))" where "x" is the output transistor number. Label and comment on the plot as necessary to clearly show the output impedance and swing of the current mirror.



1. Compare the output impedance of current mirrors.

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Q2: Chain of Current Mirror

Figure 3 shows three NMOS and PMOS current mirrors connected together. Each current mirror copies the reference current I1 to its output with a certain scale. Connect all NMOS substrates to GND.

1. Without simulation, try to determine the value of the current I2. Show hand calculations



1. Show your schematic.



1. Perform a DC sweep simulation to plot I2 versus V1. V1 should be swept from 0V to VDD=3.3V. Check if the value of the current is the same as the value you thought of in step 1.



1. Can you remove transistors M6, M7, and M8 and replace them with one transistor which gives the same current response? (hint: you can play with the W/L ratio of the transistor)
2. Explain what you would do and why this works?

Click or tap here to enter text.

1. Show a DC operating point highlighting the new current.



Q3: Common-source amplifier with an active load

Do the following for the common-source amplifier with an active load shown in Figure 2. Use ID1=1mA and VDD=5V.

1. Adjust the potentiometer (RB) for ID1=1mA. (Same procedure as step 1 in Lab - Part 1). Show your schematic.



1. Run a DC sweep to plot VO and AV=dVO/dVi versus Vi. On your graph, show the input bias point for maximum signal swing.



1. Bias the input with a potentiometer and capacitor same as Lab 1. Show your schematic.



1. Run a transient analysis for 10ms with a 10mVPP 1kHz sinusoidal input biased at the voltage found in the previous step. Plot VO and verify the small-signal gain found in the previous step.



1. Change the amplitude of the input to determine the output swing of the amplifier.



Output swing: Click or tap here to enter text.

1. This report is to be completed during the lab period by filling out this pre-made template and handed in within 30 minutes after the end of the session.