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| Lab 3: Push-Pull Power Amplifier |

Student Name: Click or tap here to enter text.

Student Number: Click or tap here to enter text.

Preparation

1. For the power amplifier of Figure 1, determine the value of CS for the cutoff frequency of 50Hz or less (f3dB=1/(2πRLCS)). For simplicity, assume the power stage is a dependent voltage source with zero output impedance. Show your hand calculation.



Final answer: Click or tap here to enter text.

1. For the power amplifier of Figure 2(b), consider |VTP|=3.5V and |VTN|=4V. Then determine the value of R1 to R4 for biasing the gate voltage of transistors at the points shown in the figure. In your calculations:
2. Neglect the current through $5k~\Omega$ resistor.
3. Assume R2=R3.
4. Set the current through resistors to 12.5uA.



Final answer: Click or tap here to enter text.

Hand in only the first two pages within 30 minutes of the start of the lab period.

Q1: Class-AB Power Amplifier Implementation

1. Simulate the class-B push-pull power amplifier in Figure 1(a) with a 1kHz 12VPP sinusoid input biased at 6V.
2. Show your schematic.



1. Plot Vi, Vx, Vo, ID1 and ID2. Use the value calculated in the preparation for CS. Simulate the circuit long enough (about 50~ms) to let $C\_s$ settle, and zoom in to the portion close to the end of the simulation to show a few cycles of the sinusoid.



1. Measure average current sourced by VDD, hence average consumed power.

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1. Determine the value of VOS and R1 in Figure 1(c) required to cancel the dead zone using the plot in the previous step.
2. Plot showing no dead zone.



1. Final values: Click or tap here to enter text.
2. Simulate the class-AB push-pull amplifier in Figure 1(c) using the value of R1 found in the previous step. Adjust the input signal source such that the output node, VX is biased at 6V with a 2VPP swing.
3. Show your schematic.



1. Plot Vi, VX, VO, ID1 and ID2. Simulate the circuit long enough (about 50ms) to let CS settle and zoom in to the portion close to the end of the simulation to show a few cycles of the sinusoid. Make sure that the power transistors are biased just in class-AB region, so the power consumption is kept minimum while the dead zone is cancelled. This step requires fine tuning of R1 as well as the input signal source.



1. Determine the voltage gain of the power amplifier. This can be done simply by comparing the input to output sinusoid amplitude.

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1. Measure average current sourced by VDD, hence average consumed power.

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1. Increase the value R1 by 20 percent. Run a transient simulation.
2. Plot VO, ID1 and ID2.



1. Measure the average consumed power.

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1. How is the power-amplifier performance affected? why?

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Q2: Class-A and Class-B Power Amplifier

1. Implement Class-A and Class-B PA as shown in Figure 2 using the values calculated in the preparation for undetermined components. Connect RL=8Ω and Vin (Zero DC and f=1kHz) by a CS=10uF to output and input of PAs respectively. Show your schematic.



1. Perform DC analysis and find the transistor currents for each PA structure. Explain any large differences between simulation and analysis.

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1. Set the input voltage to 20mVPP and perform transient analysis.
2. Plot the output.



1. Plot FFT for output signals in each case.



1. Measure the average consumed power for each PA.

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1. Determine the voltage gain of the power amplifier.

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1. Repeat step 4 for 1VPP input voltage.

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1. For 1VPP input voltage:
2. Plot ID1 and ID2 of Class-A PA in Figure 2(a).



1. Compare the result with those of class-B push-pull PA in Figure 1(a).

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1. This report is to be completed during the lab period by filling out this pre-made template and handed in within 30 minutes after the end of the session.