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| Lab 4: Frequency Response and Operational Amplifier |

Student Name: Click or tap here to enter text.

Student Number: Click or tap here to enter text.

Preparation

1. **Frequency response**

For the single-stage amplifier shown in Figure 1, write down analytic equations for all low/high frequency poles and zeros. In your calculations ignore the ro of transistor. Show hand calculations.



1. **Operational amplifier**
2. Find the numerical values for Ad, Ac, CMRR, and f3dB for IB=1mA and CL=1nF. Show hand calculations.



Final answer: Click or tap here to enter text.

1. Find the input common-mode voltage that maximizes the output swing. Show hand calculations.



Final answer: Click or tap here to enter text.

1. Write down the equation relating vO to vs based on differential gain (Ad) and common-mode gain (Ac). Then determine the condition in which the configuration of Figure 3 can be used to obtain Ad from an AC simulation. Show hand calculations.



Final answer: Click or tap here to enter text.

1. **Operational amplifier**

For the circuit in Figure 4, the output voltage is the superposition of two input signals, VCM and Vin. Input VCM is a dc voltage source and goes through a non-inverting gain Anon\_inv while input Vin is an ac voltage source and goes through an inverting gain Ainv.

1. Write down the analytic equation for Anon\_inv (in this case the coupling capacitor would be open since the input (VCM is a dc voltage). Show hand calculations.

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1. Write down the analytic equation for Ainv (in this case coupling capacitor would be shorted and VCM is set equal to zero). Show hand calculations.



1. Considering VCM=2V, determine the value of R1 and R2 to have Vo-DC=3V and an ac gain of 2. Show hand calculations.



Final answer: Click or tap here to enter text.

Hand in only the first seven pages within 30 minutes of the start of the lab period.

Q1: Frequency Response Simulation

1. Implement the the single-stage amplifier of Figure 1 in LTSpice. Use VDD=5V and VBias=2V. Show your schematic.



1. Run a DC simulation and determine gm of the transistor (to see transistor operating point use *"View 🡪 SPICE Error Log"*).

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1. Using the DC simulation result and equations extracted in part 1 of the preparation, obtain numerical values for poles and zeros location. Show hand calculations



Final answer: Click or tap here to enter text.

1. Run an AC simulation.
2. Plot frequency response over 1Hz to 10MHz.



1. Compare the result with the values from previous section.

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Q2: Operational Amplifier Simulation

1. Implement the opamp circuit shown in Figure 2 in LTSpice. Adjust the bias current (IB) to 1 mA. Show your schematic.



1. Write down the bias resistor value.

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1. Run a DC simulation to show the output swing with a differential input with the common-mode voltage found in lab preparation. You can use configuration in Figure 5(a) and sweep VDC around common-mode voltage. Label and comment on the plots to clearly show the results.



1. Using the configuration in Figure 5(b) run AC simulations to show Ad, Ac and CMRR at low frequencies. Label and comment on the plots to clearly show the results.



1. Insert a 1-nF load capacitor at the opamp output and find the f3dB.

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1. Run a transient analysis (Vin-CM=1.85V, amplitude: 1mV, frequency: 1kHz).
2. Plot Vx and Vo.



1. Explain what you observe.

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1. Change width of M4 from 1.379mm to 2.01mm.
2. Plot Vo and Vx again.



1. Justify the new waveforms.

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1. Run DC simulations and adjust one of the opamp inputs such that Vo-DC=Vx-DC. Now, the opamp is at equilibrium (you need to use separate dc voltage source for different inputs). The opamp differential input at the equilibrium is the offset voltage of the opamp. Find this offset.

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1. Repeat the transient simulation.
2. Plot Vx and Vo.



1. Compare the results with that of item 7 and 8 (before and after compensating for the offset)

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Q3: Opamp Application

1. Incorporate the opamp circuit shown in Figure 2 into the configuration of Figure 4. Use your designed value in preparation for R1 and R2 (use transistor with ideal width). Show your schematic.



1. Run a transient simulation for a 1kHz, 1VPP sinusoidal input signal. Plot Vin and Vout.



1. Justify your design considering signal gain and output dc level.

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This report is to be completed during the lab period by filling out this pre-made template and handed in within 30 minutes after the end of the session.

Q4: Bonus

1. Connect Vo and Vx of opamp circuit together in a way shown in the Figure 6. How does Ad and Ac of this circuit compare to the original values you found in item 5 of section 2.

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1. Run a transient simulation on this circuit and explain the output.



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