A Survey of Behavioral Modeling of Ferroelectric Capacitors

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Abstract: Six different behavioral models for ferroelectric capacitors are surveyed with an emphasis on their usefulness in the transient circuit simulation of integrated nonvolatile memories. These models can be broadly classified into two categories, namely, those that rely on the hysteresis loop and those that rely on the switching current of a ferroelectric capacitor. The former often involves a continuous cycling of a ferroelectric capacitor with a sinusoidal waveform. The latter employs a pulse measurement technique to capture the switching current of the capacitor. The pulse waveform applied to the ferroelectric capacitor in the latter approach resembles the actual waveform encountered in a typical ferroelectric memory access. This resemblance makes switching-current based models more suitable for use in high-speed-memory circuit simulations.

I. Introduction

There have been many attempts at modeling ferroelectric capacitors [1-5, 7] since they were introduced as storage elements in integrated nonvolatile memory applications. Although significant progress has been made in modeling, it seems that ferroelectric processing techniques and the exploitation of this material in nonvolatile memories have proceeded even faster. Therefore, the need for a transient model (as well as a more accurate steady-state model) is much more acute today than what it was, for example, five years ago.

Two potential areas of research to improve this situation lie in the investigation of physically based models and behavioral models. Physically based models normally provide better intuition into the material behavior. However, historically they have developed only gradually—sometimes many years after the material has been used in practical applications. On the other hand, behavioral modeling does not require a detailed knowledge of ferroelectric theory; it only requires a careful observation of the ferroelectric capacitor behavior from the circuit point of view.

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In this paper, we examine a variety of behavioral models for ferroelectric capacitors. We begin with the Dual Capacitor Model which approximates the nonlinear hysteresis loop with two linear capacitors. This simple model is capable of simulating the steady-state behavior of the ferroelectric capacitor. Another model that is similar in essence to the Dual Capacitor Model, but does not suffer from the linear approximation, is called the Mathematical Model [3]. In fact, this model introduces a different kind of approximation by using a closed form mathematical formula for the hysteresis loop. Nevertheless, the Mathematical Model accommodates several critical parameters of the hysteresis loop. We discuss this model further in Section 3.

The Distributed Switching Threshold Model [5] is a circuit model representing the ferroelectric capacitor. The circuit consists of a parallel combination of five different elements, corresponding to the five components of FE capacitor charge. The details of this model are presented in Section 4.

The duality between ferroelectricity and ferromagnetism brings a question to mind: Is it possible to take the solution of a similar problem in the ferromagnetic domain and apply it to its ferroelectric counterpart? This question is answered in the affirmative in Section 5, where we discuss the Ferromagnetic-Based Model [7].

All of the above models have a common basis; they all try to describe a model for the hysteresis loop characteristic of ferroelectric materials. For this reason, they are appropriate for steady-state analysis of ferroelectric capacitors. An alternative would be a model that is based on the transient current of the capacitor. Such a model would be more appropriate for transient circuit analysis. To date, there are very few models of this type in the literature. We discuss and critique two recent models [1][2] in Sections 6 and 7.

II. Dual Capacitor Model

The Dual Capacitor Model is based on the hysteresis loop characteristic of the ferroelectric capacitor. As illustrated in Fig. 1, this model approximates the two branches of the hysteresis loop by two straight lines. Each line represents a capacitor with a capacitance equal to the slope of the line. Hence, C_1 represents the lower slope line (Switch S_1 open) and C_1+C_2 represents the higher slope one (Switch S_1 closed). Assuming a symmetrical hysteresis loop, the same capacitors are used to model the left hand side of the hysteresis loop. Therefore, as an alternating voltage across the ferroelectric capacitor goes through one full cycle, Switch S_1 must be closed twice—corresponding to the right and left hand sides of the hysteresis loop.

To approximate the hysteresis loop illustrated in Fig. 1, two specific points are chosen, namely: the intercepts of the hysteresis loop and the Q axis (Q_r), and the farthest point in the hysteresis loop from the origin (Q_{max}). This choice ensures the final charge on the capacitor as calculated by the model to be equal to the one derived from the hysteresis loop. Depending on the simulation requirements, other curve fitting methods can be employed. In particular, the mean-square-error criteria is a better alternative in evaluating the slopes of the lines and, thereby, the capacitance values of the two capacitors if a simulation in a smaller range of applied voltage is required.

Since the hysteresis loop is often a combined characteristic of the ferroelectric capacitor and the voltage waveform across it, the Dual Capacitor Model is also waveform dependent, as it is based on the hysteresis loop characteristic. The two capacitances C_1 and C_2 will take different values if the voltage waveform changes from sinusoidal to, for example, triangular. Even if the voltage waveform across the capacitor is preserved except for its amplitude, the model parameters have to be changed to fit the slope of the new hysteresis loop.

To explain another implication of the waveform dependency of the hysteresis loop, consider a circuit consisting of an FE capacitor and a number of linear elements. Since the voltage waveform across the ferroelectric capacitor is not known in advance, the model parameters C_1 and C_2 cannot be determined, and hence, must be approximated. This implies another source of inaccuracy in circuit simulation using this type of modeling.

In summary, the Dual Capacitor Model parameters are waveform dependent and hard to specify, especially in more complicated circuits. However, it is simple in structure. In the next section, we discuss the Mathematical Model that sacrifices simplicity for accuracy.

III. Mathematical Model

As we mentioned in the last section, one of the major drawbacks of the Dual Capacitor Model is the waveform dependency of its parameters. This is partially caused by using a single hysteresis loop as the defining characteristic of the ferroelectric capacitor. Miller et. al. [3][4] have eliminated this drawback by incorporating a series of hysteresis loops into a mathematical model. The Saturated Polarization Loop, defined as the switching component of the largest hysteresis loop of the FE capacitor, forms the basis of the model. Recall that the switching polarization saturates when all the domains become aligned with the electric field. The variation of the other components (i.e. the electronic and non-switching ionic polarizations) are considered to be linear with the electric field.

Based on the saturability of the switching polarization and the symmetry of the hysteresis loop, the Mathematical Model approximates the Saturated Polarization Loop with two hyperbolic functions:

$$P_{sat}^{+}(E) = P_s \tanh\left[\frac{E - Ec}{2\delta}\right] \tag{1}$$

and,

$$P^{-}_{sat}(E) = -P^{+}_{sat}(-E) \qquad (2)$$

where $P_{sat}^{+}(E)$ and $P_{sat}^{-}(E)$ represent the polarization corresponding to the positive and negative going branches of the hysteresis loop, respectively. P_s and E_c are the saturation polarization and the coercive field extracted from the actual hysteresis loop. With the fixed P_s and E_c , δ is uniquely specified by P_r , the remanent polarization, through the following equation:

$$\delta = E_c\left[ln\left(\frac{1 + P_r/P_s}{1 - P_r/P_s}\right)\right]^{-1} \qquad (3)$$

A sketch of the graphs of Equations 1 and 2 are shown in Fig. 2. The symmetry with respect to the origin in this figure is guaranteed by Equation 2. Note particularly that the three parameters P_s , P_r , and E_c in this figure is the only information borrowed from the actual saturated hysteresis loop.

Minor (non-saturated) hysteresis loops are derived by assuming the following relationship between the derivatives of the unsaturated ($P_d(E)$) and the saturated polarization:

$$\frac{\partial P_d}{\partial E} = \Gamma\frac{\partial P_{sat}}{\partial E} \qquad (4)$$

where Γ is a positive function less than or equal to 1 [3]. This equation implies that the rate of change of the switching polarization is no greater than that of the saturated polarization.

The Mathematical Model provides a good approach for steady-state analysis of ferroelectric capacitor behavior. However, it is not suitable for transient analysis, as it does not include any parameter concerning the transient behavior of the FE capacitor. In fact, the minimum rise time used in [3] to verify the functionality of the model is more than 10 micro-seconds — at least two orders of magnitude larger than a typical access time of a Ferroelectric Random-Access Memory (FRAM).

IV. Distributed Threshold Switching Model

The electric field at which a dipole switches from one stable state to another is called the switching field. In single domain ferroelectrics, this field is equal to the coercive field (E_c) of the hysteresis loop characteristic of the material. In multi-domains, due to the non-unique direction of the unit cells, each dipole switches at a different value of the applied voltage. The relative number of dipoles that switch at a given voltage interval forms a distribution over the applied voltage range. This distribution can be considered Gaussian (normal) when dealing with a large number of dipoles (Law of Large Numbers). The same distribution can be justified for the incremental polarization per unit applied voltage, assuming each dipole contributes the same amount of polarization to the total polarization. Fig. 3 illustrates two such distributions that form the basis of the Distributed Threshold Switching Model (DTSM) [5].

The parameters V_c and σ in Fig. 3 represent the mean value and the standard deviation of the normal dipole distribution in the material. These values, as well as the area underneath each curve, are derived from the hysteresis loop characteristic of the material. In fact, these curves represent the saturated hysteresis loop slope as a function of applied voltage. Therefore, the mean value and the area under each curve correspond to the coercive voltage and $2P_s$ of the saturated hysteresis loop (refer to Fig. 2). The standard deviation (σ) of the distribution is representative of the squareness of the hysteresis loop.

As shown in Fig. 4, the Distributed Threshold Switching Model consists of five parallel circuit elements: one linear resistor, one linear capacitor, and three nonlinear capacitors. The linear resistor, R1, models the leakage through the dielectric as well as the thermal dissipation of polarization cycling. Capacitors C_0 to C_3 simulate various sources of polarization. C_0 simulates the linear part of electronic and nonswitching ionic polarizations. Capacitors C_1 and C_3 simulate the nonlinear nonswitching and switching polarizations, respectively. The combined characteristics of these two capacitors have a similar distribution to the one in Fig. 3. The dP/dV characteristic of C_1 is specified by a single zero-mean Gaussian function. Therefore, the charge on this capacitor simultaneously returns to zero (nonremanent) with the applied voltage. Capacitor C_3 , on the other hand, is specified by two Gaussian functions centered on $-V_c$ and $+V_c$. As the voltage across the FE capacitor increases, more dipoles switch to the opposite state and thereby increase the number of dipoles that can be switched back by a negative voltage. Capacitor C_3 keeps track of the available polarization that can be switched to one side by an applied voltage pattern. Finally, the Nonlinear Nonremanent Capacitor, C_2 , crudely models the effect of polarization relaxation, which is defined as a reduction of the remanent polarization in a microsecond time regime if the capacitor is left unaccessed following a sequence of continuous cycling [6].

In spite of their different representations, the DTSM and the Mathematical Model are in essence very similar. Both the hyperbolic tangent function, in the Mathematical Model, and the normal distribution function, in the DTSM, are used to incorporate the same characteristics: the total polarization of P_{sat}, the coercive voltage of V_c, and the standard deviation of the hysteresis loop slope of σ (or δ). In fact, both functions are uniquely specified by these three parameters. Fig. 5 compares the polarization derivative as calculated by each model. Note that both curves have an identical area, corresponding to the same P_{sat}. Also, they are centered on the same voltage, corresponding to the same V_c.

Among the FE capacitor models we have discussed so far, the Dual Capacitor Model can be easily implemented as a macromodel, using the existing features of a circuit simulator such as HSPICE. The two others, however, require source level computer programming in order to be integrated as new models in the simulator. In the next three sections, we discuss three models that can be specified explicitly as HSPICE macromodels.

V. Ferromagnetic Based Model

Ferroelectric (FE) and Ferromagnetic (FM) materials are duals in the sense that both exhibit similar hysteresis loop characteristics. The B-H curve of an FM core resembles the P-E curve of an FE capacitor. Also, the flux-voltage relationship of an FM core ($v = \frac{d\phi}{dt}$) is identical to the polarization-current relationship of an FE capacitor ($i = \frac{dQ}{dt}$). When a time-varying current source is applied to the winding around an FM core, it generates a magnetic flux in the core (according to the FM hysteresis loop) that passes through the winding and generates a voltage across it. Similarly, when a time-varying voltage source is applied to an FE capacitor, it generates a polarization charge (according to the FE hysteresis loop) on the capacitor and causes a current to flow through the capacitor. The FM Based Model [7] converts the voltage across the FE capacitor to a proportional current source, applies it to the FM core to generate a voltage based on the FM hysteresis loop, then converts this voltage back as a proportional current that flows through the capacitor. The final current waveform is guaranteed to resemble the actual current by a linear mapping of the FM and FE hysteresis loops.

An implementation of the model in HSPICE is shown in Fig. 6. A voltage controlled current source ($K_1 V_c$) converts the voltage across the capacitor, V_c, to a proportional current driving the primary winding of the HSPICE Magnetic Core Model [8]. The output voltage of this model, V_{out}, is then converted back as the ferroelectric capacitor current via the voltage controlled current source in the input circuit. The capacitor C_{lin} is added at the input to allow fine adjustment of the slope of the hysteresis curve in saturation. K_1 and K_2 are proportionality constants that can be used to scale the input and output variables when calibrating the model.

An investigation of the HSPICE Magnetic Core Model indicates that four critical points are chosen to quantify the B vs. H hysteresis loop. These points can be translated into the saturation polarization (and its corresponding electric field), the remanent polarization, the coercive field, and a knee point on an FE hysteresis loop. The FM Based Model is more accurate compared to the Dual Capacitor Model in which only two points are used to approximate the hysteresis loop. Also, this model is easier to implement as an HSPICE macromodel, since it does not require any switch to change the capacitance from one linear part of the hysteresis loop to another.

Although the FM Based Model uses the HSPICE Magnetic Core Model, it is not restricted to this model. In fact, by using a more accurate magnetic model, the corresponding FE model will acquire more accuracy. The model validity, however, is restricted to the frequency range for which: 1) a comprehensive ferromagnetic model exists and 2) the linear duality between the ferromagnetic and ferroelectric materials is preserved.

The similarity between the hysteresis loop characteristic of ferromagnetic and ferroelectric materials provides sufficient basis for the steady-state analysis of ferroelectric capacitors. For the transient analysis, however, there is no apparent duality that supports the Ferromagnetic Based Model.

VI. Current-Based Switching Model

Unlike the previous models discussed in this chapter, the Current Based Switching Model is intended for both transient and steady-state analyses [1]. This model is, in essence, a linear capacitor in parallel with a current source as illustrated in Fig. 7. Capacitor C_L is determined by the small-signal permittivity of the FE capacitor. Current source $i_s(t)$, which represents the switching current of the capacitor, is obtained from the pulse measurements. It is also assumed that the area under the switching current curve is equal to the remanent polarization of the hysteresis loop. Therefore, this model is suitable for both transient current and hysteresis loop simulations.

In order to implement this idea into a SPICE macromodel, the switching current is approximated by the following formula:

$$i_s(t) = I_0(e^{-t/\tau_n} - e^{-t/\tau_g}) \tag{5}$$

where I_0, τ_n, and τ_g are determined by curve fitting and the area constraint mentioned above. A SPICE macromodel, Fig. 8, is formed by using Equation 5 and the Thevenin equivalent of the circuit of Fig. 7. The two RC circuits on the right side of the figure generate appropriate exponential voltages across their capacitors. The difference between the two exponential voltages is fed back to the input circuit as the Thevenin equivalent of the switching current.

When the polarity of the applied voltage pulse is the same as the polarity of the initial charge on C_n and C_g , V_{cn} and V_{cg} do not change and, hence, V_p remains constant. In this case, the ferroelectric capacitor model is simply a capacitor in series with a DC voltage source. On the other hand, when the polarity of the applied voltage pulse is the opposite of the previous case, two exponential voltages will develop across the capacitors. The difference between these two voltages generates the approximated switching current (Equation 5) through V_p.

As we mentioned earlier, the model assumes that the area under the switching current waveform is equal to the remanent polarization. However, our measurement results [2] suggest this area to be 70% (or less) of the remanent polarization (a similar observation has been pointed out by Bernacki et al. [9]). This drawback can be resolved by removing the area constraint from the approximated switching current and using curve fitting techniques to determine all three parameters in Equation 5.

This model is only valid for one amplitude of the applied voltage, as the switching current is a function of the pulse amplitude. The three parameters (I_0 , τ_n , and τ_g), therefore, must be derived separately for each individual pulse amplitude. This complicates the model usage in a circuit with unknown pulse amplitude across the FE capacitor.

Another drawback of the model is the dependency of its parameters, especially τ_n and τ_g, on the RC time constant of the measurement setup. The switching of the FE capacitor is believed to happen much faster than 5RC, which is the time required for the applied voltage to fully develop across the capacitor [10]. Therefore, the model parameters, once determined, cannot be used in circuits with different time constants. These issues are addressed in the next section by discussing the Zero Switching-Time Transient Model [2].

VII. Zero Switching-Time Transient (ZSTT) Model

As its name suggests, the ZSTT model assumes the switching time of a ferroelectric capacitor to be zero. This assumption will introduce little inaccuracy if the RC time constant of the circuit under study is much larger than the switching time of the FE capacitor. It is shown [2] that for a typical memory circuit including FE capacitors such an assumption is quite valid.

Zero switching-time implies that a charge increment on the FE capacitor will take place instantaneously[1]. Therefore, a charge increment is only a function of the applied voltage and the initial state of the capacitor, not a function of time. In other words:

$$\Delta Q = \Delta Q(V, Q_{init}) \tag{6}$$

where V and Q_{init} represent the applied voltage and the initial polarization charge on the capacitor. Since there are only two initial states that are important to a memory cell (i.e. digital 0 and 1), the above equation can be broken into two parts, each corresponding to one initial state. In other words:

$$\Delta Q = \begin{cases} \Delta Q_0(V) & \text{for digital 0 state} \\ & \text{or} \\ \Delta Q_1(V) & \text{for digital 1 state} \end{cases} \tag{7}$$

Equation 7 is further represented as a state diagram in Fig. 9. A positive voltage pulse, for example, brings the capacitor to a digital 0 state if it is initially in a digital 1 state. This state transition corresponds to a charge increment of ΔQ_1 followed by a charge decrement of ΔQ_0 —both of them functions of the pulse amplitude. The pulse-measurement approach discussed in [2] approximates $\Delta Q_0(V)$ and $\Delta Q_1(V)$ with two piecewise-linear functions of voltage. Each piecewise-linear function is implemented as a piecewise-linear capacitor that exists in most circuit simulators.

1. Although an instantaneous charge increment implies an infinite current, this never occurs in a practical circuit. This is because the current is always limited by an external resistance such as the ON resistance of the access transistor.

A. *Model Implementation*

A circuit representation of the ZSTT Model is shown in Fig. 10. $C_0(V_0)$ and $C_1(V_1)$ represent the two nonlinear capacitors corresponding to the two binary states of the FE capacitor discussed earlier. If the binary state of the FE capacitor is 0, switches S_{01} and S_{12} are closed while switches S_{11} and S_{02} are open. In this case, the equivalent capacitance looking into the input terminals is $C_0(V_0)$. Meanwhile, a voltage controlled voltage source, which is equal to V_i , is connected to $C_1(V_1)$ to initialize this capacitor for the opposite binary state. For binary state 1, the states of the switches are the reverse: switches S_{11} and S_{02} are closed while switches S_{01} and S_{12} are open. Therefore, the capacitance looking into the input terminals is $C_1(V_1)$, and the controlled source is connected to $C_0(V_0)$ for the similar reason mentioned above.

If the initial binary state of an FE capacitor is known, its subsequent binary states can be determined by the applied pulse pattern. A binary state 0 remains unchanged in response to a positive pulse as well as the leading edge (falling edge) of a negative pulse. It only changes on the trailing edge (rising edge) of the negative pulse. A binary state 1 remains unchanged in response to a negative pulse as well as the rising edge of a positive pulse. It only changes on the falling edge of the positive pulse.

The ZSTT Model can be easily implemented as an HSPICE macro-model if the two nonlinear capacitors in Fig. 10 are replaced by their piecewise linear approximations. The switches can be replaced by voltage-controlled resistors (VCRs) that exhibit high and low resistances for the open and closed states of the switches, respectively. The logic circuit shown in Fig. 11 provides appropriate control signals for the switches. The flip-flop toggles with the falling edge of T, where:

$$T = \overline{QPD + \overline{Q}NU} \tag{8}$$

The toggle flip-flop and the logic gates are all implemented in HSPICE.

One example of an input voltage pattern and its corresponding control signals for the switches are illustrated in Fig. 12. The initial binary state of the capacitor, in this example, is considered to be 0. Therefore, S_{01} and S_{12} are initially closed ($CS_{01} = CS_{12}$ = High), and the equivalent capacitance looking into the input terminals is $C_0(V_0)$. On the rising edge of the first negative pulse, switches S_{11} and S_{02} are closed ($CS_{11} = CS_{02}$ = logic 1) and switches S_{01} and S_{12} are opened ($CS_{01} = CS_{12}$ = logic 0). In this case, the capacitance looking into the input terminals is $C_1(V_1)$. This situation will be reversed again on the falling edge of the first positive pulse.

VIII. Conclusion

Among the six different models surveyed in this paper, the Current-Based Switching Model and the Zero Switching-Time Transient model employ transient current information. The rest rely on the hysteresis loop characteristic of the material, which is waveform dependent and inaccurate for transient analysis.

The Current-Based Switching Model parameters are affected by the RC time constant of the measurement setup. They must also be optimized for every pulse amplitude. Both of these drawbacks are addressed by the Zero Switching-Time Transient Model.

Further improvement in the ZSTT model (Fig. 10) can be achieved by adding two resistors, $R_0(V)$ and $R_1(V)$, in parallel with $C_0(V)$ and $C_1(V)$, respectively, to model the effect of polarization relaxation. This requires an accurate measurement of the decay rate of the volatile-remanent polarization as a function of the input-pulse voltage amplitude.

Table 1 summarizes the relative strengths and weaknesses of the models surveyed in this paper.

IX. Acknowledgment

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X. References

[1] D. E. Dunn, A Ferroelectric Capacitor Macromodel and Parameterization Algorithm for Spice Simulation, IEEE Trans. on UFFC, Vol. 41, No. 3, pp. 360-369, May 1994.

[2] A. Sheikholeslami and P. Glenn Gulak, “Transient Modeling of Ferroelectric Capacitors for Nonvolatile Memories”, IEEE Trans. on UFFC, Vol. 43, No. 3, pp. 450-456, May 1996

[3] S. L. Miller, J.R. Schwank, R. D. Nasby, M. S. Rodgers, “Modeling Ferroelectric Capacitor Switching with Asymmetric Nonperiodic Input Signals and Arbitrary Initial Conditions”, *J. Appl. Phys.,* No. 70 (5), 1 Sep. 1991.

[4] S. L. Miller, R.D. Nasby, J. R. Schwank, M. S. Rodgers, et al., “Device Modeling of Ferroelectric Capacitors”, *J. Appl. Phys.,* No. 68 (12), 15 Dec. 1990.

[5] Radiant Technologies, Inc., “RT66A Model 2.1 User’s Manual”, pp. 22-29, 1990.

[6] R. Moazzami, et al., “Impact of Polarization Relaxation on Ferroelectric Memory Performance,” *Symp. on VLSI Technology, Dig. of Tech. Papers*, Oiso, Japan, pp. 61-62, May 1991.

[7] S. W. Wood, “Ferroelectric Memory Design”, M.A.Sc. Thesis, Univ. of Toronto, 1992.

[8] Meta-Software, Inc., “HSPICE User’s Manual”, Vol. 2, Page 11-18, 1996.

[9] S. Bernacki, L. Jack, Y. Kisler, S. Collins, et al., “Standardized Ferroelectric Capacitor Test Methodology for Nonvolatile Semiconductor Memory Applications”, *Integrated Ferroelectrics”,* Vol. 3, pp. 97-112, 1993.

[10] P. K. Larsen, G. L. M. Kampschoer, M. J. E. Ulenaers, G. A. C. M. Spierings, and R. Cuppens, “Nanosecond Switching of Thin Ferroelectric Films”, *Appl. Phys. Lett.*, Vol. 59, No. 5, pp. 611-613, 29 July 1991.

FIGURES

Captions

Figure 1: Dual Capacitor Model: The hysteresis loop is approximated by two straight lines, and hence, two linear capacitors. S1 is closed for the higher slope line.

Figure 2: The hysteresis loop forms the basis of the Mathematical Model. Two hyperbolic tangent functions approximate the Saturated Polarization Loop.

Figure 3: The distribution of polarization is considered Gaussian in the DTSM. The dashed and the solid curves correspond to decreasing and increasing applied voltages, respectively.

Figure 4: Distributed Threshold Switching Model.

Figure 5: The polarization derivative with respect to the applied voltage as calculated by the Mathematical Model (solid curve) and the DTSM (dashed curve).

Figure 6: Ferromagnetic Based Model. The voltage across the ferroelectric capacitor is fed into its ferromagnetic counterpart by a voltage controlled current source (K_1V_c). The output voltage of the ferromagnetic core is transformed back into a proportional current by another voltage controlled current source (K_2V_{out}).

Figure 7: (**a**) A linear capacitor in parallel with a current source forms the basis of the Current Based Switching Model. (**b**) The current source waveform is the switching current of the FE capacitor.

Figure 8: Current-Based Switching Model. (**a**) The voltage controlled voltage source, V_p, takes the difference between the two exponential voltages across C_n and C_g and generates the appropriate switching current in the input circuit. (**b**) The polarity of V_n and V_g changes with the input voltage. (**c**) The voltage controlled resistors, R_n and R_g , determine the time constants of the exponential voltages across C_n and C_g. V_{cg} and V_{cn} remain unchanged when the input voltage is less than the coercive voltage which is 1 Volt in this case.

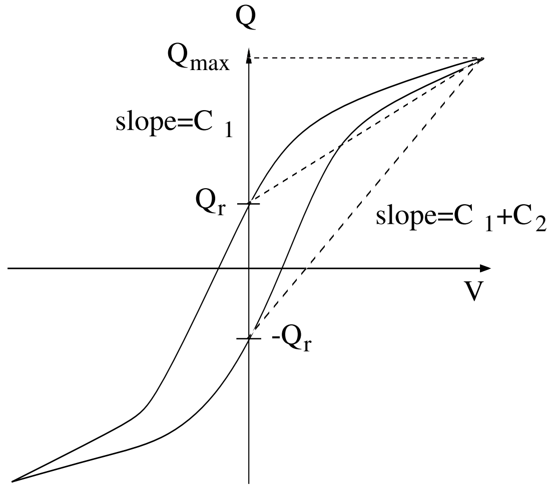
Figure 9: (**a**) Hysteresis Loop employed as a polarization state diagram, (**b**) State Transition Diagram for a two-state capacitor model

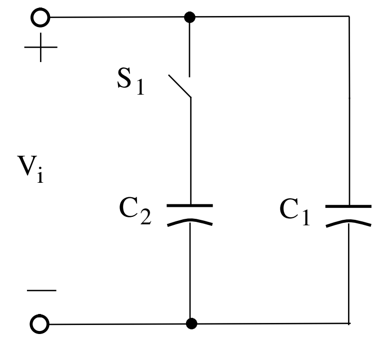
Figure 10: An implementation of the ZSTT Model.

Figure 11: (a) A logic circuit providing the control signals for the switches in the ZSTT model, (b) the corresponding state-transition diagram.

Figure 12: A sample voltage pattern across the FE capacitor and its corresponding control signals for switches in the ZSTT Model.

Table 1: The relative strengths and weaknesses of the FE capacitor models.





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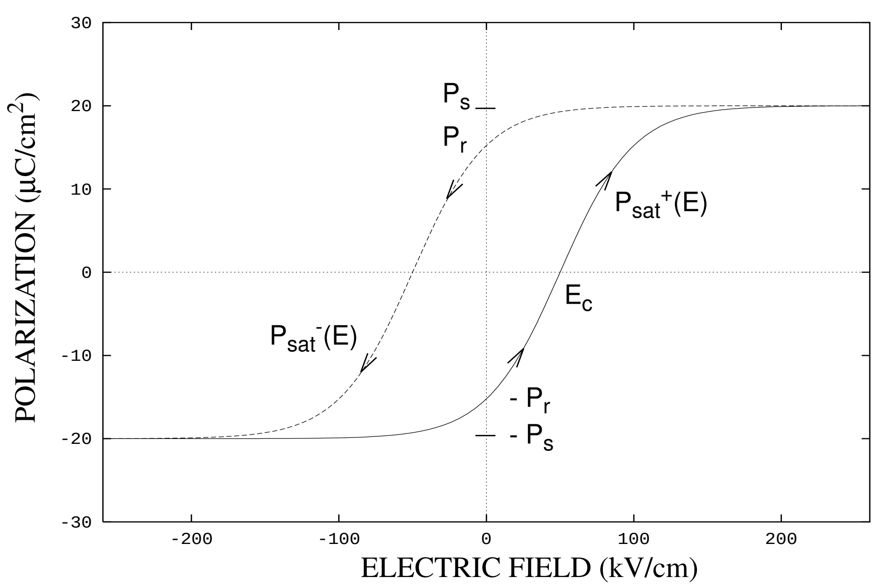


Figure 2: The hysteresis loop forms the basis of the Mathematical Model. Two hyperbolic tangent functions approximate the Saturated Polarization Loop.

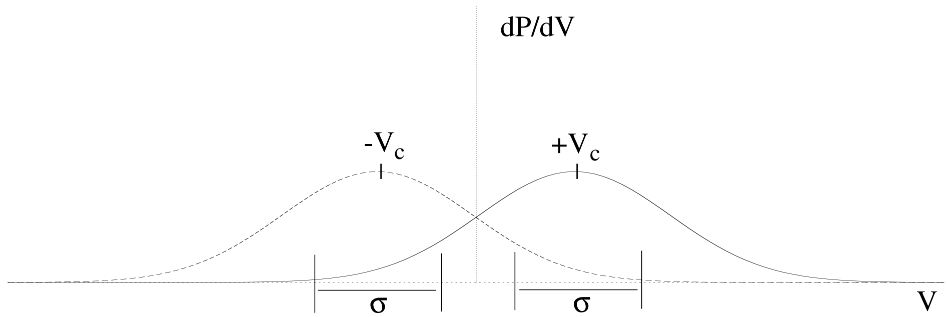


Figure 3: The polarization derivative with respect to the applied voltage in the DTSM. The dashed and the solid curves correspond to decreasing and increasing applied voltages, respectively.

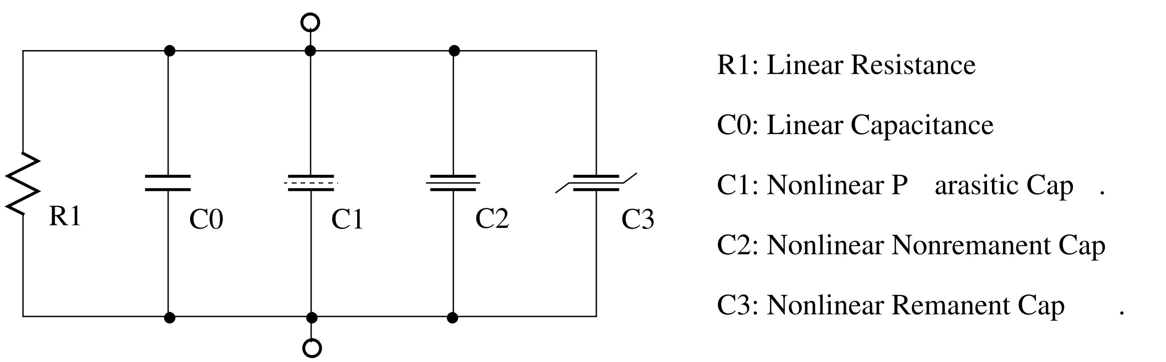


Figure 4: Distributed Threshold Switching Model

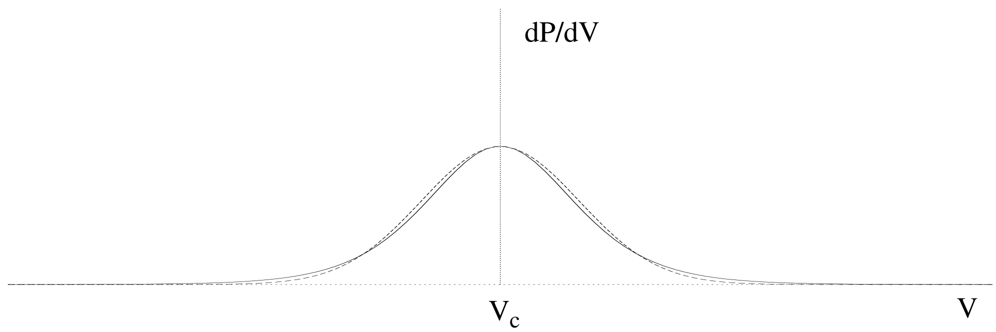


Figure 5: The polarization derivative with respect to the applied voltage as calculated by the Mathematical Model (solid curve) and the DTSM (dashed curve).

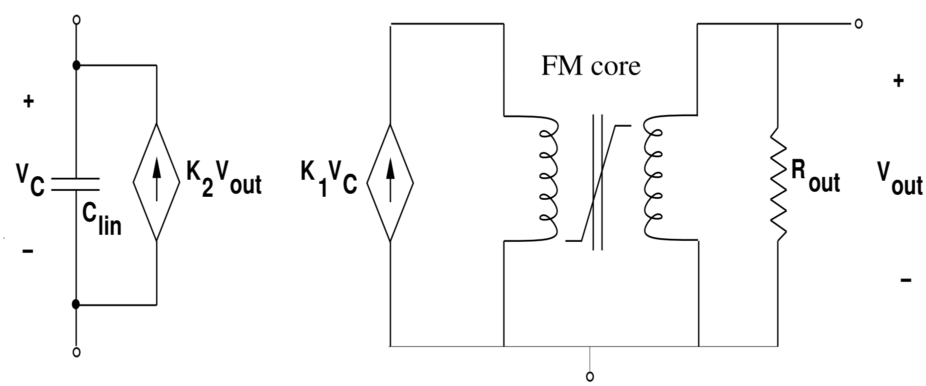
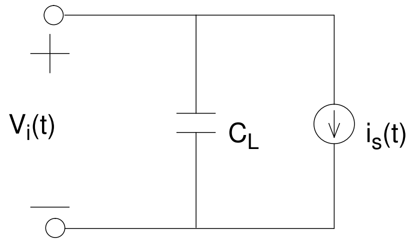
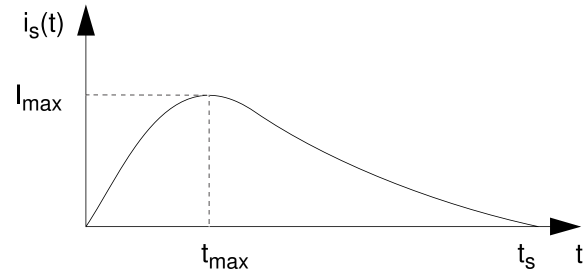


Figure 6: Ferromagnetic (FM) Based Model: The voltage across the ferroelectric capacitor is fed into its ferromagnetic counterpart by a voltage controlled current source (K_1V_c). The output voltage of the ferromagnetic core is transformed back into a proportional current by another voltage controlled current source (K_2V_{out}).

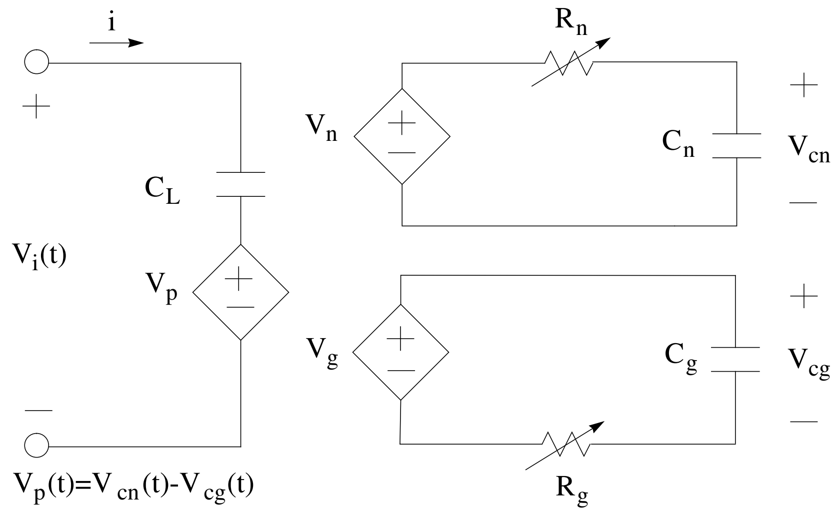


(**a**)

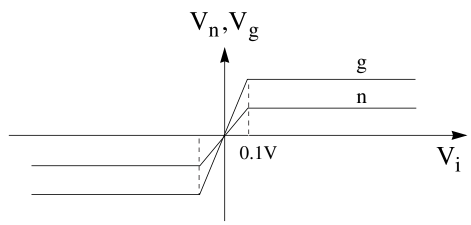


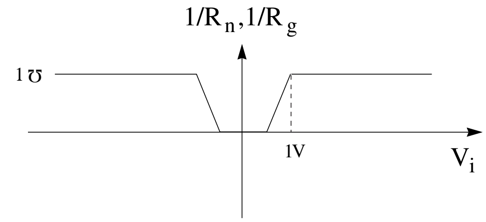
(**b**)

Figure 7: (**a**) A linear capacitor in parallel with a current source forms the basis of the Current Based Switching Model. (**b**) The current source waveform is the switching current of the FE capacitor.



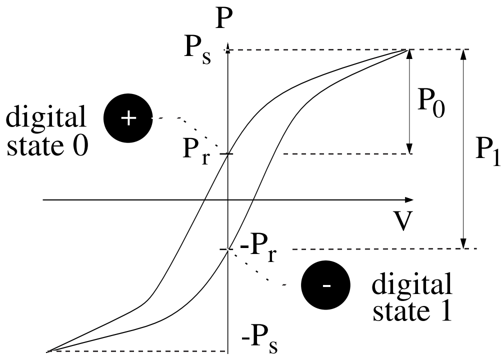
(**a**)



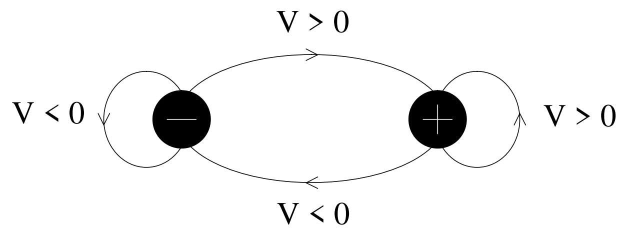


(**b**) (**c**)

Figure 8: Current-Based Switching Model: (**a**) The voltage controlled voltage source, V_p, takes the difference between the two exponential voltages across C_n and C_g and generates the appropriate switching current in the input circuit. (**b**) The polarity of V_n and V_g changes with the input voltage. (**c**) The voltage controlled resistors, R_n and R_g , determine the time constants of the exponential voltages across C_n and C_g. V_{cg} and V_{cn} remain unchanged when the input voltage is less than the coercive voltage which is 1 Volt in this case.



(**a**)



(**b**)

Figure 9: (**a**) Hysteresis Loop employed as a polarization state diagram, (**b**) State Transition Diagram for a two-state capacitor model

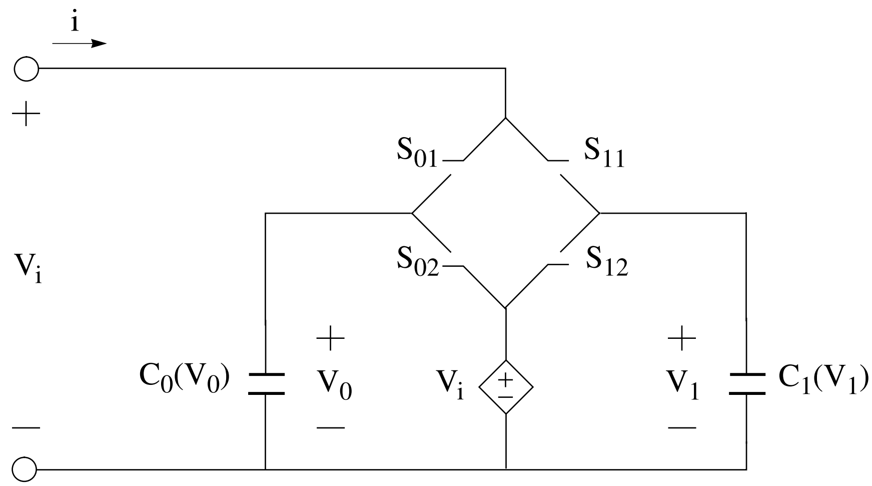


Figure 10: An implementation of the ZSTT Model.

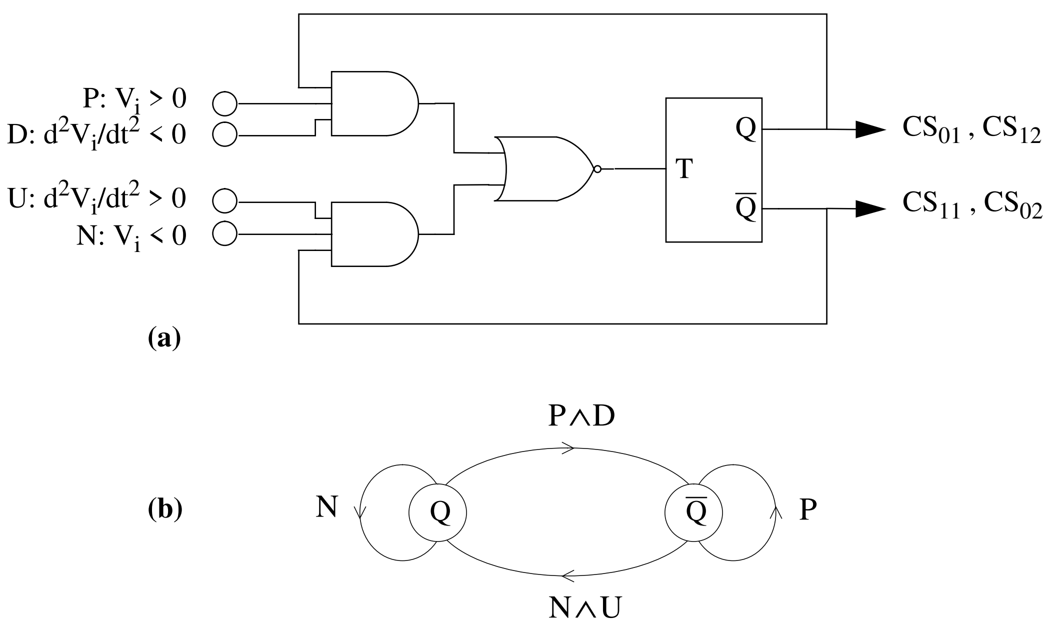


Figure 11: (a) A logic circuit providing the control signals for the switches in the ZSTT model, (b) the corresponding state-transition diagram.

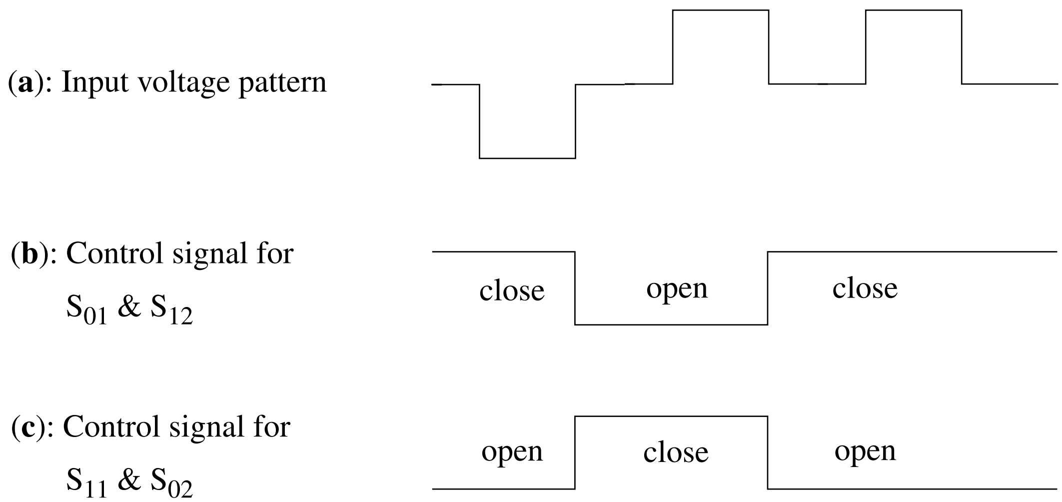


Figure 12: A sample voltage pattern across the FE capacitor and its corresponding control signals for switches in the ZSTT Model.

Model	Steady State	Transient	Strengths	Weaknesses†	Reference
Dual Capacitor Model	Yes	No	Simple, Macromodel‡	Approximate	—
Mathematical Model	Yes	No	Accurate	Complex	[3]
DTSM	Yes	No	Accurate	Complex	[5]
Ferromagnetic Based Model	Yes	No	Simple, Macromodel	Approximate	[7]
Current-Based Switching Model	Yes	Yes	Macromodel	Approximate, RC Dependent	[1]
ZSTT Model	Yes	Yes	Accurate, Macromodel	—	[2]

Table 1: The relative strengths and weaknesses of the FE capacitor models

† Time-dependent switching is not considered in any of the above models. Polarization relaxation is only approximately modeled by DTSM.

‡ The term *macromodel* indicates that the model can be implemented in a standard circuit simulator.