

A Digital Offset-Compensation Scheme for an LA and CDR in 65-nm CMOS

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Abstract

A digital offset-compensation scheme for a limiting amplifier (LA) and CDR is presented. The proposed scheme detects the LA offset by sampling the CDR recovered clock with the LA output. The scheme eliminates offset-induced data jitter and compensates offset even for levels that saturate the LA output and cause the CDR not to lock. The compensation circuitry consumes 7.2 mW and occupies $160 \times 110 \mu\text{m}^2$, a third the area of the LA.

Introduction

Optical communication receivers employ a limiting amplifier (LA) whose input signal swing can be on the order of tens of mV, a value comparable to the LA offset. If uncompensated, the offset degrades receiver performance and in the extreme may saturate the LA output, leading to receiver failure.

The conventional offset-compensation scheme [1] senses the offset in the voltage domain, requiring a capacitor on the order of μF to achieve a low-frequency cutoff of tens of kHz, as specified by SONET standards. The scheme proposed in [2], which also senses the offset in the voltage domain, occupies an area 10 times that of the LA itself and, further, loads each LA stage, constraining the LA bandwidth.

In this paper we propose a digital offset-compensation scheme that detects the effects of LA offset in the duty-cycle distortion (DCD) present in the LA output and compensates for it digitally in the time domain. This eliminates large circuit components. To illustrate this concept, a receiver targeting 10-Gb/s operation was fabricated in 65-nm CMOS.

Proposed Compensation Technique

Fig. 1 illustrates the proposed offset-detection technique. A phase-tracking CDR aligns its recovered clock, CK_{OUT} , to the input signal, LA_{OUT} , such that its falling edge aligns at the LA_{OUT} transition (more accurately, a sampler's $t_{CK-to-Sample}$ delay earlier) and its rising edge aligns at the midpoint of LA_{OUT} unit intervals (UIs).

An LA with an uncompensated offset produces output with unequal UI widths, or DCD. For positive offset, the 1 UI is wider than the 0 UI and sampling CK_{OUT} on the rising transition of LA_{OUT} yields high samples, while sampling CK_{OUT} on the LA_{OUT} falling transition yields low samples; conversely, samples of the opposite polarity are produced for negative offset. This technique is different than [4] in which the data is sampled by the clock. Integrating and filtering the difference between these samples produces a correction signal that can be fed back to the LA. The averages of the samples equalize when the UI widths are balanced, at which point the offset—and the DCD introduced by the offset—is canceled.

If there is no DCD present in the LA's input signal, this scheme completely cancels the LA offset. If the input signal does possess DCD, the scheme adjusts the offset of the LA such that the aggregate DCD at its output is canceled. Canceling DCD eliminates the dead zone that it induces in the phase detector's transfer characteristic, improving CDR jitter tracking and receiver jitter tolerance.

CK_{OUT} is sampled on both edges of LA_{OUT} to reduce the effect of the samplers' $t_{CK-to-Sample}$ (< 2 ps in simulation) and thus reduce the residual offset.

Receiver Architecture

The receiver (Fig. 2) consists of an LA, CDR and offset-detection and offset-correction blocks. The LA consists of four 3rd-order interleaving active feedback stages [3]. The full-rate CDR employs the quadricorrelator to enable frequency acquisition without a reference clock. A 1:16 DEMUX converts the CML recovered data to CMOS levels.

The rising-edge and falling-edge offset samples are subtracted, integrated, converted to a bias voltage, V_{CTRL} , by the 7-bit DAC and finally fed back to the LA input stage to cancel its offset. The bandwidth of the compensation loop is set three orders of magnitude lower than that of the CDR. This guarantees that the compensation loop does not interfere with the CDR's frequency or phase acquisition process, as confirmed by simulations.

Circuit Implementation

The rising- and falling-edge offset samples are DEMUXed and fed to the compensation logic (Fig. 3). There they are each summed by an analog adder and compared to determine the set that contains more high samples. The comparator outputs each enable a 16-bit counter, which, upon overflow, cause the 7-bit up/dn counter to increment or decrement. The up/down counter's output is converted to a bias voltage, V_{CTRL} and $\overline{V_{CTRL}}$, by the DAC and fed back to the LA input stage (Fig. 4). This signal serves as bias voltages that correct the LA offset via a small secondary input pair. An additional pair of tail devices allows an offset to be applied from off-chip by V_{OS-EXT} . The simulated 3- σ offset of 25 mV requires that the DAC possess a 290-mV swing, or 2.3-mV LSB.

If the LA offset is larger than the input, its output will saturate at logic low or high, producing no transitions on which to sample the clock. This is accounted for by detecting the occurrence of consecutive identical digits (CIDs) above the 72 required by the SONET CID immunity requirement [5]. Sixteen-input NOR and AND gates detect if all 16 bits of each DEMUXed frame are low or high. The output of each gate enables a 3-bit counter that causes the up/dn counter to respectively decrement or increment upon overflow. The 3-bit counters are reset if data of the opposite polarity is detected, leaving the up/dn counter undisturbed for less than 128 CIDs.

Experimental Results

The receiver is fabricated in 65-nm CMOS and was measured by direct probing. The VCO tuning range is centered at 7.9 GHz, 21 percent below the target for 10-Gb/s operation. The receiver core consumes 314 mW from 1.2 V, 7.2 mW of which is consumed by the compensation logic and DEMUX. The output buffers operate from 1.3 V and consume 115 mW.

Measured with a Centellax BERT, the receiver achieves $\text{BER} < 10^{-12}$ for $28\text{-mV}_{pp} 2^{31}-1$ PRBS input at 7.5 Gb/s. Fig. 5 illustrates the improvement in the recovered data due to

reduction of offset-induced jitter for 28-mV_{pp} input. Data jitter is reduced from 36.8 to 23.1 ps_{pp} and from 39.0 to 23.0 ps_{pp} when 3-mV and 12-mV offsets are applied to the LA.

Fig. 6 plots the receiver's jitter tolerance for BER < 10⁻¹⁰ with 2³¹-1 input. Measurement equipment allowed jitter to be applied only up to 10 MHz. As shown in Fig. 6(a), the tolerance is degraded by a 6-mV offset when compensation is disabled but is restored to the level of the offset-free case when compensation is enabled.

Fig. 6(b) plots the jitter tolerance measured with 14-mV_{pp} input and 0-, 7- and 14-mV offsets. With compensation disabled, the CDR fails to lock for the latter two cases. With it enabled, the CDR locks and the tolerance is equal to that of the offset-free case, demonstrating the compensation of offset larger than the input. Fig. 7 shows a die micrograph and performance summary. The compensation logic occupies 160×110 μm² and the full receiver 1.27×1.10 mm².

References

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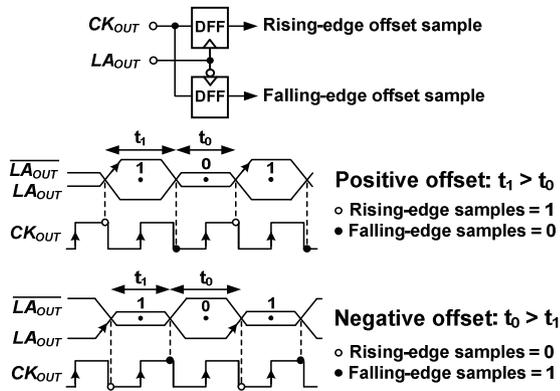


Fig. 1. Offset-detection concept.

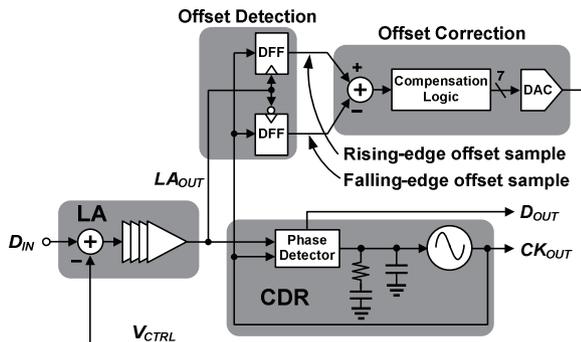


Fig. 2. Receiver architecture.

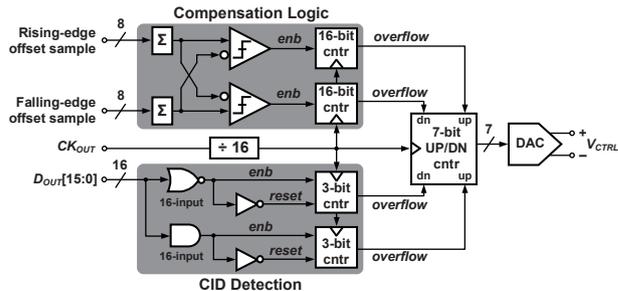


Fig. 3. Offset-compensation circuitry.

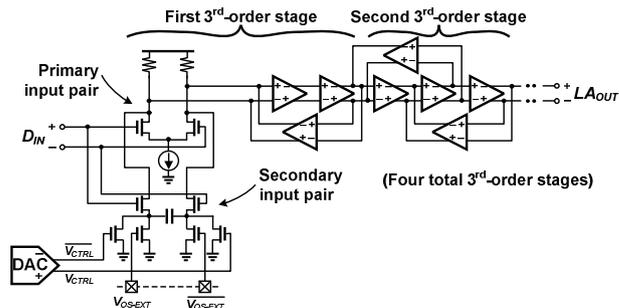


Fig. 4. Limiting amplifier schematic.

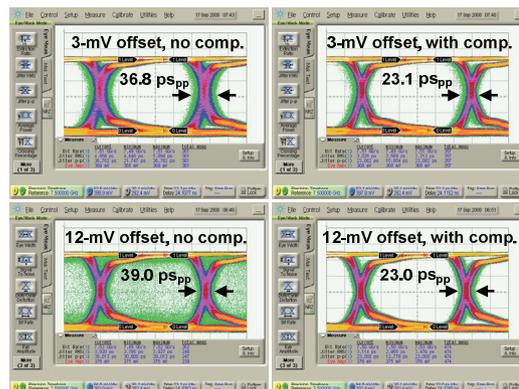


Fig. 5. Reduction of offset-induced jitter in recovered data.

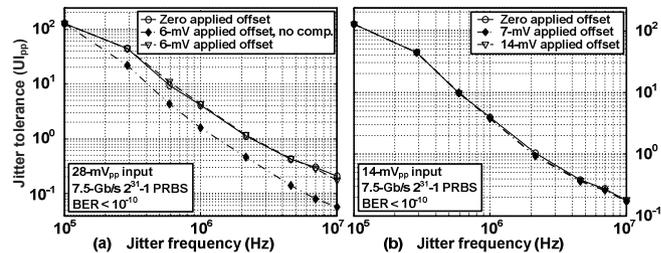


Fig. 6. Measured jitter tolerance.

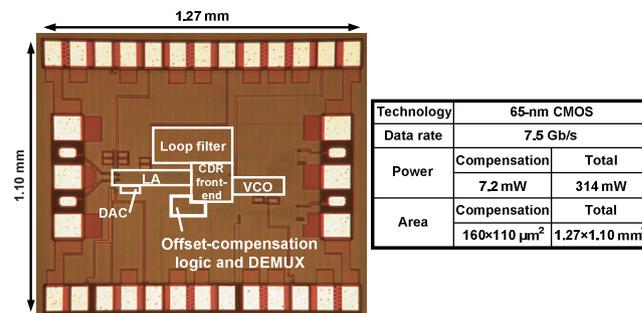


Fig. 7. Die micrograph and performance summary.