Natalie Enright Jerger

Contact Information

The Edward S. Rogers Department of Electrical and Computer Engineering
10 King's College Rd
University of Toronto
Toronto, ON M5S 3G4 Canada

Voice: (416) 978-5056
Fax: (416) 971-2326
E-mail: enright@ece.utoronto.ca
Webpage: www.eecg.toronto.edu/~enright

Education

University of Wisconsin, Madison, Wisconsin USA

Ph.D., Electrical Engineering, December 2008

Dissertation: "Chip Multiprocessor Coherence and Interconnect System Design"
Advisors: Mikko H. Lipasti and Li-Shiuan Peh

M.S., Electrical and Computer Engineering, May 2004

Purdue University, West Lafayette, Indiana USA

B.S., Computer Engineering, May 2002

Appointment

University of Toronto, Electrical and Computer Engineering, Toronto, Ontario, Canada

Professor — **July 2017 - Present**

Associate Professor — **July 2014 - July 2017**

Assistant Professor — **January 2009 - July 2014**

Research Interests

Computer architecture, many-core architectures, approximate computing, on-chip networks, cache coherence protocols, interconnection networks, emerging applications for many-core architectures.

Industrial Experience

Advanced Micro Devices, Bellevue, WA — Visiting Scholar, July 2015-December 2016

IBM, Rochester, MN — Intern, June 2006 - Oct 2006

Intel, Santa Clara, CA — Intern, Microarchitecture Research Lab, May 2004 - December 2004

Hewlett Packard, Vancouver, WA — Intern, May 2001 - August 2001

Hewlett Packard, Vancouver, WA — Intern, May 2000 - August 2000

Honors and Awards

IEEE Fellow, 2021

Computing Research Association Distinguished Service Award, 2020
As part of the team that founded the Committee to Aid Reporting on Discrimination and Harassment Policy Violations (CARES)

McLean Senior Fellow, 2019

Canada Research Chair in Computer Architecture, 2019

ACM Distinguished Scientist, 2018

Gordon R. Slemon Teaching of Design Award, 2017

IEEE MICRO Top Picks Honorable Mention for "The Anytime Automaton", 2017

Percy Edward Hart Professor in Electrical and Computer Engineering, 2016-2019

125 People of Impact from University of Wisconsin, Department of Electrical and Computer Engineering, 2016

IEEE MICRO Top Picks from Computer Architecture for "Enabling Interposer-based Disintegration of Multi-core Processors", 2016

Borg Early Career Award, 2015

Sloan Research Fellow, 2015-2017

IEEE MICRO Top Picks Honorable Mention for "NoC Architectures for Silicon Interposer System", 2015

Ontario Professional Engineers Young Engineer Medal, 2014

Ministry of Research and Innovation Early Researcher Award, 2012

IBM Ph.D. Fellowship, 2007, 2008

Peter R. Schneider Distinguished Graduate Fellowship, University of Wisconsin-Madison, 2002

University of Wisconsin Teaching Academy Future Faculty Partner, 2004-2008

Publications Peer-Reviewed Conferences

[C1] **Hossein Farrokhbakht, Henry Kao, Kamran Hasan**, Paul Gratz, Tushar Krishna, Joshua San Miguel, Natalie Enright Jerger "Pitstop: Enabling a Virtual Network Free Network-on-Chip", *In Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2021.

[C2] **Mario Badr**, Carlo Delconte, Isak Edo, Radhika Jagtap, Matteo Andreozzi, Natalie Enright Jerger, "Mocktails: Capturing the Memory Behaviour of Propietary Mobile Architectures," *In Proceedings of the ACM/IEEE International Symposium on Computer Architecture (ISCA)*, June 2020.

[C3] Jieming Yin, Subhash Sethumurugan, Yasuko Eckert, Alan Smith, Chintan Patel, Eric Morton, Mark Oskin, Natalie Enright Jerger, Gabriel H. Loh, "Experiences with ML-Driven Design: A NoC Case Study." *In Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2020.

[C4] **Mayank Parasar, Hossein Farrokhbakht**, Natalie Enright Jerger, Paul Gratz, Tushar Krishna, Joshua San Miguel, "DRAIN: Deadlock Removal for Arbitrary Irregular Networks." *In Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2020.[1]

[C5] **Mayank Parasar**, Natalie Enright Jerger, Paul Gratz, Joshua San Miguel and Tushar Krishna, "SWAP: Synchronized Weaving of Adjacent Packets for Network Deadlock Prevention." *In Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO)*, October 2019.

[C6] **Hossein Farrokhbakht**, Henry Kao and Natalie Enright Jerger, "UBERNoC: Unified Buffer Power-Efficient Router for Network-on-Chip." *In Proceedings of the ACM/IEEE International Symposium on Networks on Chip (NOCS)*, October 2019.

[C7] **Hossein Farrokhbakht**, Hadi Mardani Kamali and Natalie Enright Jerger, "Muffin: Minimally-Buffered Zero-Delay Power-Gating Technique in On-Chip Routers." *In Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, July 2019.

[C8] **Karthik Ganesan, Joshua San Miguel** and Natalie Enright Jerger. "The What's Next Intermittent Computing Architecture." *In Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, 2019 (acceptance rate: 21%).

[C9] Joshua San Miguel, **Karthik Ganesan, Mario Badr, Chunqiu Xia, Rose Li, Hsuan Hsiao**, and Natalie Enright Jerger, "An Analytical Model for Early Design Space Exploration

[1] Student authors identified in bold.

of Intermittent Processor Architectures." *In Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO)*, October 2018 (acceptance rate: 21%).

[C10] **Hossein Farrokhbakht**, Hadi Mardani Kamali, Natalie Enright Jerger, and Shaahin Hessabi, "SPONGE: A Scalable Pivot-based On/Off Gating Engine for Reducing Static Power in NoC Routers." *In Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, July 2018.

[C11] Jieming Yin, Zhifeng Lin, Onur Kayiran, Matthew Poremba, Muhammad Shoaib Bin Altaf, Natalie Enright Jerger and Gabriel H. Loh. "Modular Routing Design for Chiplet-based Systems." *In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA)*, June 2018 (acceptance rate: 17%.).

[C12] **Joshua San Miguel, Jorge Albericio**, Natalie Enright Jerger and Aamer Jaleel. "The Bunker Cache for Spatio-Value Approximation." *In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October 2016 (acceptance rate: 22%).

[C13] **Patrick Judd, Jorge Albericio, Tayler Hetherington**, Tor Aamodt, Natalie Enright Jerger and Andreas Moshovos. "Proteus: Exploiting Numerical Precision Variability in Deep Neural Networks." *In Proceedings of the ACM International Conference on Supercomputing (ICS)*, 2016.

[C14] **Jorge Albericio, Patrick Judd, Tayler Hetherington**, Tor Aamodt, Natalie Enright Jerger and Andreas Moshovos. "Cnvlutin: Zero-Neuron-Free Deep Convolutional Neural Network Computing." *In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA)*, June 2016, pp. 1-13 (acceptance rate: 19%).

[C15] **Joshua San Miguel** and Natalie Enright Jerger. "The Anytime Automaton." *In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA)*, June 2016, pp. 545-557 (acceptance rate: 19%).

[C16] **Zimo Li, Joshua San Miguel** and Natalie Enright Jerger. "The Runahead Network-on-Chip." *In Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2016, pp. 333-344 (acceptance rate: 22%).

[C17] Jieming Yin, Onur Kayiran, Matthew Poremba, Natalie Enright Jerger and Gabriel H. Loh. "Efficient Synthetic Traffic Models for Large, Complex SoCs." *In Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2016, pp. 297-308 (acceptance rate: 22%).

[C18] **Ajaykumar Kannan**, Natalie Enright Jerger and Gabriel H. Loh. "Enabling Interposer-based Disintegration of Multi-core Processors" *In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2015, pp. 546-558 (acceptance rate: 21%).

[C19] **Joshua San Miguel, Jorge Albericio**, Andreas Moshovos and Natalie Enright Jerger. "Doppelganger: A Cache for Approximate Computing" *In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2015, pp. 50-61 (acceptance rate: 21%).

[C20] Gabriel H. Loh, Natalie Enright Jerger, **Ajaykumar Kannan** and Yasuko Eckert. "Interconnect-Memory Challenges for Multi-Chip, Silicon Interposer Systems" *In Proceedings of the ACM International Symposium on Memory Systems (MEMSYS)*, October 2015, pp. 3-10.

[C21] **Robert Hesse** and Natalie Enright Jerger. "Improving DVFS in NoCs with Coherence Prediction" *In Proceedings of the IEEE/ACM International Symposium on Networks on Chip (NOCS)*, September 2015.

[C22] **Joshua San Miguel** and Natalie Enright Jerger. "Data Criticality in Network-on-Chip Design" *In Proceedings of the IEEE/ACM International Symposium on Networks on Chip (NOCS)*, September 2015. (**Best paper nominee**).

[C23] **Jorge Albericio, Joshua San Miguel**, Natalie Enright Jerger and Andreas Moshovos. "Wormhole: Wisely predicting multidimensional branches." *In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2014, pp. 509-520 (acceptance rate: 19%).

[C24] Natalie Enright Jerger, **Ajaykumar Kannan, Zimo Li** and Gabriel H. Loh. "NoC Architectures for Silicon Interposer Systems." *In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2014, pp. 458-470 (acceptance rate: 19%).

[C25] **Joshua San Miguel, Mario Badr** and Natalie Enright Jerger. "Load Value Approximation" *In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2014 (acceptance rate: 19%), pp. 127-139.

[C26] **Haofan Yang, Jyoti Tripathi**, Natalie Enright Jerger and Dan Gibson. "Dodec: Random-Link, Low-Radix On-Chip Networks." *In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2014 (acceptance rate: 19%), pp 496-508.

[C27] **Andrew Bitar, Jeffrey Cassidy**, Natalie Enright Jerger and Vaughn Betz. "Efficient and Programmable Ethernet Switching with a NoC-Enhanced FPGA." *In Proceedings of the ACM/IEEE Symposium on Architectures for Networking and Communication Systems (ANCS)*, October 2014 (acceptance rate: 34%).

[C28] **Wenbo Dai** and Natalie Enright Jerger. "Sampling-based Approaches to Accelerating Network-on-Chip Simulation." *In Proceedings of the IEEE/ACM International Symposium on Networks on Chip (NOCS)*, September 2014 (acceptance rate: 26%).

[C29] **Parisa Khadem Hamedani**, Natalie Enright Jerger and Shaahin Hessabi. "QuT: A Low-Power All-Optical Architecture for a Next Generation of Network-on-Chip." *In Proceedings of the IEEE/ACM International Symposium on Networks on Chip (NOCS)*, 2014 (acceptance rate: 26%).

[C30] **Goran Narancic, Patrick Judd, Di Wu, Islam Atta, Michel El Nacouzi, Jason Zebchuk**, Natalie Enright Jerger, Serag Gadelrab, Kyros Kutulakos, Andreas Moshovos and Jorge Albericio. "Evaluating Memory System Behavior of Smartphone Workloads." *In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, 2014.

[C31] **Mario Badr** and Natalie Enright Jerger. "SynFull: Synthetic Traffic Models Capturing a Full Range of Cache Coherence Behaviour." *In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA)*, June 2014 (acceptance rate: 18%).

[C32] **Tahir Diop, Steven Gurfinkel**, Jason Anderson and Natalie Enright Jerger. "DistCL: A Framework for Distributed Execution of OpenCL Kernels." *In Proceedings of the IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS)*. August 2013 (acceptance rate: 27%).

[C33] **John Matienzo** and Natalie Enright Jerger. "Performance Analysis of Broadcasting Algorithms on the Intel Single Chip Cloud Computer." *In Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2013, pp. 163-172. (acceptance rate: 26%).

[C34] **Michel El Nacouzi, Islam Atta, Myrto Papadopoulou, Jason Zebchuk**, Natalie Enright Jerger and Andreas Moshovos. "A Dual-Grain Hit/Miss Detector for Large Stacked Die DRAM Caches." *In Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, March 2013, pp. 89-92. (acceptance rate: 36%).

[C35] **Robert Hesse, Jeff Nicholls** and Natalie Enright Jerger. "Fine-Grained Bandwidth Adaptivity in Networks-on-Chip Using Bidirectional Channels." *In Proceedings of the IEEE/ACM 6th International Network on Chip Symposium (NOCS)*, May 2012, pp. 132-141. (acceptance rate: 30%).

[C36] **Sheng Ma**, Natalie Enright Jerger and Zhiying Wang. "Whole Packet Forwarding: Efficient Design of Fully Adaptive Routing Algorithms for Networks-on-Chip." *In Proceedings of the 18th IEEE International Symposium on High Performance Computer Architecture (HPCA)*. Feb. 2012, pp. 467-479. (acceptance rate: 17%).

[C37] **Sheng Ma**, Natalie Enright Jerger and Zhiying Wang. "Supporting Efficient Collective Communication in NoCs." *In Proceedings of the 18th IEEE International Symposium on High Performance Computer Architecture (HPCA)*. Feb. 2012, pp. 165-177. (acceptance rate: 17%).

[C38] **Parisa Khadem Hamedani**, Shaahin Hessabi, Hamid Sarbazi-Azad and Natalie Enright Jerger. "Exploration of Temperature Constraints for Thermal Aware Mapping of 3D Networks on Chip." *In Proceedings of the 20th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP)*. Feb. 2012, 499-506. (acceptance rate: 34%).

[C39] **Sheng Ma**, Natalie Enright Jerger, and Zhiying Wang. "DBAR: An Efficient Routing Algorithm to Support Multiple Concurrent Applications in Networks-on-Chip." *In Proceedings of the 38th ACM/IEEE International Symposium on Computer Architecture (ISCA)*. June 2011, pp. 413-424. (acceptance rate: 19%).

[C40] **Danyao Wang**, Natalie Enright Jerger, and J. Gregory Steffan. "DART: A Programmable Architecture for NoC Simulation on FPGAs." *In Proceedings of the 5th IEEE/ACM International Network on Chip Symposium (NOCS)*. May 2011, pp 145-152. (acceptance rate: 25%).

[C41] Natalie Enright Jerger. "SigNet: Network-on-Chip Filtering for Coarse Vector Directories." *In Proceedings of the International Conference on Design Automation and Test in Europe (DATE)*. March 2010, pp. 1378-1383. (acceptance rate: 26%).

[C42] **Mitch Hayenga**, Natalie Enright Jerger and Mikko Lipasti. "SCARAB: A Single Cycle Adaptive Routing and Bufferless Network." *In Proceedings of the 42nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*. New York, New York. Dec. 2009, pp. 244-254. (acceptance rate: 25%).

[C43] Dennis Abts, Natalie Enright Jerger, John Kim, **Dan Gibson**, and Mikko Lipasti. "Achieving Predictable Performance through Better Memory Controller Placement in Many-Core CMPs." *In Proceedings of the 36th IEEE/ACM International Symposium on Computer Architecture (ISCA)*. June 2009, pp. 451-461. (acceptance rate: 20%).

[C44] Natalie Enright Jerger, Li-Shiuan Peh and Mikko H. Lipasti. "Virtual Tree Coherence: Leveraging Regions and In-Network Multicast Trees for Scalable Cache Coherence." *In Proceedings of the 41st IEEE/ACM International Symposium on Microarchitecture (MICRO)*. Nov. 2008, pp. 35-46. (acceptance rate: 19%).

[C45] Natalie Enright Jerger, Li-Shiuan Peh and Mikko H. Lipasti. "Virtual Circuit Tree Multicasting: A Case for On-Chip Hardware Multicast Support." *In Proceedings of the 35th IEEE/ACM International Symposium on Computer Architecture (ISCA)*. Beijing, China. June 2008, pp. 229-240. (acceptance rate: 14%).

[C46] Natalie Enright Jerger, Li-Shiuan Peh and Mikko H. Lipasti. "Circuit-Switched Coherence." *In Proceedings of the 2nd IEEE/ACM International Symposium on Networks on Chip(NOCS)*. April 2008, pp. 193-202. (acceptance rate: 32%).

[C47] Natalie Enright Jerger, Dana Vantrease and Mikko Lipasti. "An Evaluation of Server Consolidation Workloads for Multi-Core Designs." *In Proceedings of IEEE International Symposium on Workload Characterization (IISWC)*. Sept. 2007, pp. 47-56. (acceptance rate: 40%).

[C48] Natalie Enright Jerger, Eric Hill, and Mikko Lipasti. "Friendly Fire: Understanding the Effects of Multiprocessor Prefetches." *In Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*. March 2006, pp. 177-188. (acceptance rate: 30%).

Publications Peer-Reviewed Journals

[J1] Phillip Stanley-Marbell, Armin Alaghi, Michael Carbin, Eva Darulova, Lara Dolecek, Andreas Gerstlauer, Ghayoor Gillani, Djordje Jevdjic, Thierry Moreau, Mattia Cacciotti, Alexandros Daglis, Natalie Enright Jerger, Babak Falsafi, Sasa Misailovic, Adrian Sampson, Damien Zufferey, "Exploiting Errors for Efficiency: A Survey from Circuits to Applications," *ACM Computing Surveys*, accepted February 2020.

[J2] **Xia Zhao**, Sheng Ma, Zhiying Wang, Natalie Enright Jerger and Lieven Eeckhout, "CD-Xbar: A Converge-Diverge Crossbar Network for High-Performance GPUs," *IEEE Transactions on Computers*, accepted March 2019.

[J3] **Mario Badr** and Natalie Enright Jerger, "A High-Level Model for Exploring Multi-Core Architectures," *Elsevier Journal on Parallel Computing*, 2018.

[J4] Andreas Moshovos, **Jorge Albericio, Patrick Judd, Alberto Delmas Lascorz, Sayeh Sharify, Zissis Poulos, Tayler Hetherington**, Tor Aamodt and Natalie Enright Jerger, "Exploiting Typical Values to Accelerate Deep Learning," *IEEE Computer*, vol. 51, no. 5, pp 18-30, May 2018.

[J5] Andreas Moshovos, **Jorge Albericio, Patrick Judd, Alberto Lascorz, Sayeh Sharify, Tayler Hetherington**, Tor Aamodt, Natalie Enright Jerger, "Value-Based Deep Learning Hardware Accelerators," *IEEE Micro*, 2018.

[J6] **Joshua San Miguel, Karthik Ganesan, Mario Badr**, and Natalie Enright Jerger, "The EH Model: Analytical Exploration of Energy-Harvesting Architectures," *IEEE Computer Architecture Letters*, 2017.

[J7] **Thierry Moreau, Joshua San Miguel, Mark Wyse, James Bornholt**, Luis Ceze, Natalie Enright Jerger and Adrian Sampson, "A Taxonomy of Approximate Computing Techniques," *IEEE Embedded Systems Letters*, 2017.

[J8] **Patrick Judd, Jorge Albericio, Tayler Hetherington,** Tor Aamodt, Natalie Enright Jerger, Raquel Urtasun and Andreas Moshovos. "Proteus: Exploiting Precision Variability in Deep Neural Networks." *Elsevier Journal on Parallel Computing*, 2017.

[J9] **Ajaykumar Kannan**, Natalie Enright Jerger and Gabriel H. Loh. "Exploiting Interposer Technologies to Disintegrate and Reintegrate Multi-core Processors." *IEEE Micro Top Picks from Computer Architecture*, May-June 2016.

[J10] **Sheng Ma**, Zhiying Wang, Zonglin Liu and Natalie Enright Jerger. "Leaving One Slot Empty: Flit Bubble Flow Control for Torus Cache-coherent Networks-on-Chip." *IEEE Transactions on Computers*, vol. 64, no. 3, pp. 763-777, March 2015.

[J11] **Sheng Ma**, Zhiying Wang, Natalie Enright Jerger, Li Shen and Nong Xiao. "Novel Flow Control for Fully Adaptive Routing in Cache-coherent NoCs." *IEEE Transactions on Parallel and Distributed Computing*, vol. 25, no. 9, pp. 2397-2407, September 2014.

[J12] **Parisa Khadem Hamedani**, Shaahin Hessabi, Hamid Sarbazi-Azad and Natalie Enright Jerger. Exploration of Temperature Constraints for Thermal Aware Mapping of 3D Networks on Chip. International Journal of Adaptive, Resilient and Autonomic Systems, Special issue on Networked Embedded Systems, vol, 4, no. 3, pp. 42-60, July-September 2013

[J13] **Sheng Ma**, Natalie Enright Jerger, Zhiying Wang, Mingche Lai, and Libo Huang. Holistic Routing Algorithm Design to Support Workload Consolidation in NoCs. *IEEE Transactions on Computers*, vol. 63, no. 3, pp. 529-542, March 2014.

[J14] **Danyao Wang, Charles Lo, Jasmina Vasiljevic**, Natalie Enright Jerger and J. Gregory Steffan. DART: A Programmable Architecture for NoC Simulation on FPGAs. IEEE Transactions on Computers, vol. 63, no. 3, pp. 664-678, March 2014.

[J15] **Matthew Misler** and Natalie Enright Jerger. Moths: Mobile Threads for On-Chip Networks. In ACM Transactions on Embedded Computing. (manuscript submitted: March 2011, revised: August 2011, accepted: December 2011, published: March 2013).

[J16] Radu Marculescu, Umit Ogras, Li-Shiuan Peh, Natalie Enright Jerger and Yatin Hoskote. Outstanding Research Problems in NoC Design: Circuit-, Microarchitecture- and System-Level Perspective. In IEEE Transactions on Computer-Aided Design, vol. 28, no. 1, pp. 3-21, 2009. (Most downloaded article in Transactions on Computer-Aided Design of 2009.)

[J17] Natalie Enright Jerger, Mikko Lipasti and Li-Shiuan Peh. Circuit-Switched Coherence. IEEE Computer Architecture Letters, vol. 6, no. 1, Mar. 2007.

[J18] Elizabeth M. O'Callaghan and Natalie Enright Jerger. Women and Girls in Science and Engineering: Understanding the Barriers to Recruitment, Retention and Persistence across the Educational Trajectory. Journal of Women and Minorities in Science and Engineering, vol. 12, no. 2-3, pp. 209–232, 2006.

Publications Book

[P1] Natalie Enright Jerger, Joshua San Miguel, "Approximate Cache Architectures", In *Approximate Circuits and Methodologies*, Springer, 2018, p. 18.

[P2] Natalie Enright Jerger, Tushar Krishna and Li-Shiuan Peh. "On-Chip Networks, 2nd Edition", Synthesis Lecture in Computer Architecture. (Editor: Margaret Martonosi). Morgan & Claypool Publishers. June 2017, 212 pages.

[P3] Natalie Enright Jerger and Li-Shiuan Peh. "On-Chip Networks", Synthesis Lecture in Computer Architecture. (Editor: Mark Hill). Morgan & Claypool Publishers. July 2009, 142 pages. (downloaded over 4700 times as of December 2016).

Publications Refereed Workshop & Posters

[P4] **Karthik Ganesan, Kamran Hasan** and Natalie Enright Jerger, "Approximate Computing for Privacy in IoT Devices," Workshop on Approximate Computing Across the Stack (in conjection with ASPLOS), 2020. (Cancelled due to COVID-19).

[P5] **Karthik Ganesan, Joshua San Miguel** and Natalie Enright Jerger, "The What's Next Computing Architecture," Workshop on Approximate Computing Across the Stack, 2018.

[P6] **Mario Badr** and Natalie Enright Jerger, "On the Evaluation of Computer Architectures," Proceedings of the Second Workshop on Pioneering Processor Paradigms, 2018.

[P7] **Mario Badr** and Natalie Enright Jerger, "Fast and Accurate Performance Analysis of Synchronization." Proceedings of the 9th International Workshop on Programming Models and Applications for Multicores and Manycores, 2018.

[P8] **Mark Sutherland** and Natalie Enright Jerger. "Near Data Processing at Runtime." *1st International Workshop on Architecture for Graph Processing*, 2017.

[P9] **Robert Hesse** and Natalie Enright Jerger. "Hierarchical Clustering for On-Chip Networks". *1st International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems*, 2016.

[P10] **Patrick Judd, Jorge Albericio, Tayler Hetherington**, Tor Aamodt, Natalie Enright Jerger and Andreas Moshovos. "Proteus: Exploiting Numerical Precision Variability in Deep Neural Networks." *2nd Workshop on Approximate Computing*, 2016.

[P11] **Mark Sutherland, Joshua San Miguel**, Natalie Enright Jerger. "Texture Cache Approximation on GPUs." *Workshop on Approximate Computing Across the Stack*, 2015.

[P12] **Ajaykumar Kannan, Mario Badr, Parisa Khadem Hamedani**, Natalie Enright Jerger. "Offloading to the GPU: An Objective Approach." *In the 3rd Annual Workshop on Parallelism in Mobile Platforms*, 2015.

[P13] **Mark Sutherland, Ajaykumar Kannan**, Natalie Enright Jerger. "Not quite my tempo: Matching Prefetches to Memory Access Time." *In Workshop for 2nd Data Prefetching Competition*, 2015.

[**P14**] **Jorge Albericio, Joshua San Miguel**, Natalie Enright Jerger and Andreas Moshovos. "Wormhole Branch Prediction Using Multi-dimensional Histories." *In the 4th Championship Branch Prediction Workshop*, 2014.

[**P15**] **Joshua San Miguel** and Natalie Enright Jerger. "Load Value Approximation: Approaching the Ideal Memory Access Latency" *Workshop on Approximate Computing Across the System Stack (WACAS)*, 2014.

[**P16**] **Tahir Diop**, Natalie Enright Jerger and Jason Anderson. "Power Modeling for Heterogeneous Processors." *Workshop on General Purpose Processing using GPUs*, 2014.

[**P17**] **Wenbo Dai** and Natalie Enright Jerger. "Accelerating Network-on-Chip Simulation via Sampling". In *International Symposium on Performance Analysis of Systems and Software* (poster). March 2014.

[**P18**] **Sam Vafaee** and Natalie Enright Jerger. "C++ Front-End for Distributed Transactional Memory." In the Intel Symposium on Single-Chip Cloud Computing. March 2011

[**P19**] **Matthew Misler** and Natalie Enright Jerger. "Moths: Mobile Threads for On-Chip Network", Intl Conf. on Parallel Architectures and Compilation Techniques (poster). Sept 2010.

[**P20**] **Danyao Wang**, Natalie Enright Jerger, J. Gregory Steffan. "DART: Fast and Flexible NoC Simulation Using FPGAs," 5th Annual Workshop on Architectural Research Prototyping, June 2010.

Publications Non-Reviewed

[**P21**] Natalie Enright Jerger, "Chiplet-Based Systems", Computer Architecture Today (Editor: Rajeev Balasubramonian), November 9, 2020, `https://www.sigarch.org/chiplet-based-systems/`.

[**P22**] Natalie Enright Jerger, "Time to Eliminate In-Person PC Meetings?" Computer Architecture Today (Editor: Rajeev Balasubramonian), March 11, 2020, `https://www.sigarch.org/time-to-eliminate-in-person-pc-meetings/`.

[**P23**] Daniel J. Sorin and Natalie Enright Jerger, "Save IEEE Computer Architecture Letters." Computer Architecture Today (Editor: Alvin Lebeck), July 16, 2019, `https://www.sigarch.org/save-ieee-computer-architecture-letters/`.

[**P24**] Natalie Enright Jerger and Kelly Shaw, "Chilly Climate in Computer Architecture?," Computer Architecture Today (Editor: Alvin Lebeck), August 23, 2018, `https://www.sigarch.org/chilly-climate-in-computer-architecture/`.

[**P25**] Natalie Enright Jerger, David Kaeli, Christos Kozyrakis, Gabriel Loh, Thomas Wenisch, David Wood, "R2: The Future of ISCA, or not," Computer Architecture Today (Editor: Alvin Lebeck), May 31, 2018, `https://www.sigarch.org/r2-the-future-of-isca-or-not/`.

[**P26**] Natalie Enright Jerger, "Welcome to the Women in Computer Architecture (WICARCH) community," Computer Architecture Today (Editor: Alvin Lebeck), May 7, 2018, `https://www.sigarch.org/welcome-to-the-women-in-computer-architecture-wicarch-community/`.

[**P27**] Natalie Enright Jerger and Kim Hazelwood, "Gender Diversity in Computer Architecture," Computer Architecture Today (Editor: Alvin Lebeck), September 28, 2017, `https://www.sigarch.org/gender-diversity-in-computer-architecture/`.

[**P28**] **Patrick Judd, Jorge Albericio, Tayler Hetherington**, Tor Aamodt, Natalie Enright Jerger, Raquel Urtasun and Andreas Moshovos, "Reduced-Precision Strategies for Bounded Memory in Deep Neural Nets", Tech report, 2015.

[**P29**] Natalie Enright Jerger, "Explaining Parallel Architecture Design", Book Review: Parallel Computer Organization and Design, Computing in Science and Engineering, 2013.

[**P30**] Natalie Enright Jerger and Mikko Lipasti, "Systems for Very Large-Scale Computing," IEEE MICRO Special Issue (guest editors' introduction), Vol. 31, No. 3, pp. 4-7, 2011.

PUBLICATIONS
PATENT

[P31] Natalie D. Enright[2], Jamison Collins, Perry Wang, Hong Wang, Xinmin Tran, John Shen, Gad Sheaffer, Per Hammarlund. Mechanism to exploit synchronization overhead to improve multithread performance. Patent no: 7487502. Sept 2009. Assignee: Intel Corporation.

SOFTWARE ARTIFACTS RELEASED

DART: An FPGA Network-on-Chip Simulation Acceleration Engine
Released: May 2011
Downloads to date: 341.

DistCL: A Framework for Distributed Execution of OpenCL Kernels
Released: August 2013
Downloads to date: 84.

Power Modeling for Heterogeneous Processors Framework
Released: April 2014
Downloads to date: 26.

SynFull: Synthetic Traffic Models Capturing Cache Coherent Behaviour
Released: May 2014
Downloads to date: 146.

Mocktails: Capturing the Memory Behaviour of Propietary Mobile Architectures
Released: June 2020

INVITED TALKS

Architecting Chiplet-based Systems
Keynote, 13th International Workshop on Network-on-Chip Architectures, October 2020
CS Distinguished Lecture, Purdue University, October 2019
Carnegie Mellon University, August 2019
Keynote at International Conference on Parallel Architectures and Compilation Techniques (PACT), November 2018

Error-Efficient Architectures for Machine Learning
ECE Distinguished Lecture, Ohio State University, April 2019

Rapid Design Space Exploration of Interconnection Networks
Invited Talk at Workshop on Modeling and Simulation of Systems and Applications, August 2018

Architectural Techniques to Efficiently Handle Big Data Challenges
Princeton University, January 2018

Hardware Software Co-Design for Approximate Computing
Brown University, October 2017

Exploiting Approximate Value Locality
AMD Research, July 2015

Energy-Efficient Communication in Many-Core Architectures
AMD (Markham), August 2015
University of Rochester, October 2014

Accelerating Network-on-Chip Simulation with SynFull
PACT 2014 Tutorial: Advanced Design, Analysis and Verification of NoC Architectures

[2]Issued under maiden name

Designing High Performance, Energy-Efficient Networks-on-Chip
University of Wisconsin-Madison, November 2013
Google (Madison), November 2013

Optimizations for Cache-Coherent Networks-on-Chip
University of Washington, April 2013
AMD Research, April 2013
MIT, April 2013
Texas A&M University, March 2013
Cornell University, March 2013
University of Illinois, March 2013
University of Michigan, February 2013
Northwestern University, January 2013

Accelerating Many-Core Network-on-Chip Simulation
Intel Corporation, January 2014
Intel Corporation, January 2013

Reactive Coherence-based Traffic Models
Intel Corporation, January 2012

Towards Application-Aware Network-on-Chip Architectures
McMaster University, March 2012
Intel Corporation, November 2011
IBM T.J. Watson, June 2011
University of Waterloo, ECE Department, March 2011
Qualcomm, November 2010

On-Chip Network Research: Opportunities to Leverage Platform 2012
Research Workshop on STMicroelectronics Platform 2012 (organized by CMC Microsystems), November 2010

Outstanding Research Challenges in On-Chip Networks
Altera Corporation, Toronto ON, June 2009.

Virtual Tree Coherence: Leveraging Regions and In-Network Multicast Trees for Scalable Cache Coherence
International Symposium on Microarchitecture, November 2008.
12th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2008.
Gigascale Systems Research Center, Quarterly Concurrent Theme Meeting, June 2008.

Virtual Circuit Tree Multicasting: A Case for On-Chip Hardware Multicast Support
International Symposium on Computer Architecture, June 2008

Harnessing Computing Power through Communication
Computer Science and Engineering Colloquium, Washington University in St. Louis, April 2008
Computer Engineering Group, University of Toronto, March 2008

Virtual Proximity: Interconnect Support for Flexible Scheduling of Server Consolidation Workloads in CMPs
IBM Research Triangle Park, October 2007

11th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2007

An Evaluation of Server Consolidation Workloads for Multi-Core Designs
IEEE International Symposium on Workload Characterization, Boston MA, September 2007

Circuit-Switched Coherence
2nd Annual IEEE Network on Chip Symposium, April 2008
10th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2006
IBM Austin Research Lab, October 2006

Friendly Fire: Understanding the Effects of Multiprocessor Prefetches
IEEE Symposium on Performance Analysis of Systems and Software, March 2006
8th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2004

Press

"How Chip Makers Are Circumventing Moore's Law to Build Super-Fast CPUs of Tomorrow" `https://gizmodo.com/how-chip-makers-are-circumventing-moores-law-to-build-s-1831268322`

"Inside AMD's Quest to Build Chips That Can Beat Intel"
`https://gizmodo.com/inside-amds-quest-to-build-chips-that-can-beat-intel-1824064984`

Funding and Support

Ultra Low Power Secure Processors for Emerging Applications at the Edge 2020
Source of support: NSERC Discovery Grant (sole PI)
Total amount: $380,000
Annual amount: $76,000
Annual amount/PI: $76,000

Ultra Low Power Secure Processors for Emerging Applications at the Edge 2020
Source of support: NSERC Discovery Accelerator Supplement (sole PI)
Total amount: $120,000
Annual amount: $40,000
Annual amount/PI: $40,000

McLean Senior Fellow 2019
Source of support: University of Toronto (sole PI)
Total amount: $125,000
Annual amount: $125,000
Annual amount/PI: $125,000

Canada Research Chair in Computer Architecture 2019-2024
Source of support: Canada Research Chairs (sole PI)
Total amount: $500,000
Annual amount: $100,000
Annual amount/PI: $100,000

Design exploration of an ASIC for Blockchain Processing 2019
Source of support: NSERC Engage Grant (sole PI)
Total amount: $25,000
Annual amount: $25,000
Annual amount/PI: $25,000

NSERC COHESA: Computing Hardware for Emerging Intelligent Sensory Applications 2017-2022
Source of support: Natural Science and Engineering Research Council, Strategic Network Grant (co-PI, PI: Andreas Moshovos)
Total amount: $5,500,000

Annual amount: $1,100,000
Annual amount/PI: $55,000

Percy Edward Hart Chair 2016
Source of support: University of Toronto (sole PI)
Total amount: $225,000
Annual amount: $75,000
Annual amount/PI: $75,000

Sloan Research Fellowship 2015
Source of support: Alfred P. Sloan Foundation (sole PI)
Total amount: $50,000 (USD)
Annual amount: $25,000 (USD)
Annual amount/PI: $25,000 (USD)

Power and Performance Characterization of Embedded GPUs 2014
Source of support: NSERC Engage Grant (sole PI)
Total amount: $25,000
Annual amount: $25,000
Annual amount/PI: $25,000

Intelligently Orchestrating Communication in Many-Core Architectures 2014
Source of support: Natural Sciences and Engineering Research Council, Discovery (sole PI)
Total amount: $186,000
Annual amount: $31,000
Annual amount/PI: $31,000

Evaluation of Direct Interconnect Architectures for Datacenters 2013
Source of support: Natural Sciences and Engineering Research Council, Engage Grant (sole PI)
Total amount: $25,000
Annual amount: $25,000
Annual amount/PI: $25,000

Power-Efficient Heterogeneous Architectures 2012
Source of support: Ontario Centres of Excellence (OCE) and AMD (PI w/ J. Anderson)
Total amount: $25,000 (OCE) + $20,000 (AMD)
Annual amount: $45,000
Annual amount/PI: $22,500

High Performance Many-Core Architectures and Interconnection Networks 2012-2017
Source of support: Ministry of Research and Innovation, Early Researcher Award (sole PI)
Total amount: $140,000
Annual amount: $28,000
Annual amount/PI: $28,000

Data Supply Architectures for Smartphone and Tablet Devices 2011-2014
Source of support: Natural Sciences and Engineering Research Council, Collaborative Research and Development Grant (co-PI w/ A. Moshovos and T. Aamodt (UBC))
Total amount: $171,212
Annual amount: $57,070
Annual amount/PI: $19,023

Data Supply Architectures for Smartphone and Tablet Devices 2011-2014
Source of support: Qualcomm (co-PI w/ A. Moshovos and T. Aamodt (UBC))
Total amount: $150,000
Annual amount: $50,000
Annual amount/PI: $16,667

Developing, Analyzing and Accelerating Smartphone Workloads 2011-2014
Source of support: Natural Science and Engineering Research Council (co-PI w/ A. Moshovos and K. Kutulakos)

Total amount: $507,590
Annual amount: $169,196
Annual amount/PI: $56,399

On-Chip Networks to Enable Exascale Computing 2011-2012
Source of support: Connaught New Researcher Award (sole PI)
Total amount: $50,000
Annual amount: $25,000
Annual amount/PI: $25,000

Next Generation FPGA Platforms 2011-2013
Source of support: Fujitsu Labs (co-PI w/ A. Sheikholeslami and J. Anderson)
Total amount: $297,000
Annual amount: $148,500
Annual amount/PI: $49,500

Early-Stage Coherence Modeling for On-Chip Network Performance & Power Analysis 2011-2014
Source of support: Intel University Research Office (sole PI)
Total amount: $171,000 (USD)
Annual amount: $57,000 (USD)
Annual amount/PI: $57,000 (USD)

Applications Exploiting Heterogeneous Processor Architectures for Improved Throughput and Energy-Efficiency 2011
Source of support: Natural Sciences and Engineering Research Councile, Engage Grant (PI w/ J. Anderson)
Total amount: $24,940
Annual amount: $24,940
Annual amount/PI: $12,470

Multi-core applications, architectures and algorithms for complex systems 2011-2016
Source of support: Canadian Foundation for Innovations (co-PI w/ Z. Tate and J. Anderson)
Total amount: $291,789
Annual amount: $58,357
Annual amount/PI: $19,452

Multi-core applications, architectures and algorithms for complex systems 2011-2016
Source of support: Ministry of Research and Innovation, Ontario Research Fund (co-PI, w/ Z. Tate and J. Anderson)
Total amount: $291,785
Annual amount: $58,356
Annual amount/PI: $19,452

Heterogeneous Multi-Core Architectures 2010
Source of support: AMD (PI w/ J. Anderson)
Total amount: $20,000 + Donation of 2 ATI Graphics Cards
Annual amount: $20,000
Annual amount/PI: $10,000

Exploiting Efficient Communication in the SCC 2010
Source of support: Intel Corporation (PI w/ G. Steffan)
In-Kind Contribution: Access to the Intel Single-Chip Cloud Computer (consists of 48 IA-32 cores on a single die with 4 memory controllers and a 4×6 mesh on-chip network)

Hybrid NoC/Crossbar Designs for SoC Fabrics 2010
Source of support: Natural Sciences and Engineering Research Council, Engage Grant (sole PI)
Total amount: $23,580
Annual amount: $23,580
Annual amount/PI: $23,580

Integrated Photonics for Energy-Efficient Multi-Core Processors 2010-2013
Source of support: Natural Science and Engineering Research Council, Strategic Project Grant (co-PI w/ J. Poon, A. Moshovos, A. Leon-Garcia)
Total amount: $533,100
Annual amount: $177,700
Annual amount/PI: $44,425

Semantically Rich Networks for Many-Core Architectures 2009-2014
Source of support: Natural Sciences and Engineering Research Council, Discovery (sole PI)
Total amount: $135,000
Annual amount: $27,000
Annual amount/PI: $27,000

Communication-centric Many-Core Computing Architectures 2009
Source of support: Connaught Fund (sole PI)
Total amount: $10,000
Annual amount: $10,000
Annual amount/PI: $10,000

Start-Up Funds 2009
Source of support: University of Toronto (sole PI)
Total amount: $100,000

Teaching

Instructor ratings below refer to the "Overall Rating as an Instructor" question on the anonymous course evaluations filled out by students at the end of the semester.

ECE253 – Digital and Computer Systems 2019, 2020

- A second year EngSci course on digital logic, assembly language and computer organization.
- Fall 2019 enrollment: –; Instructor rating: –/5 (Dept. average: –/5).
- Fall 2019 enrollment: –; Instructor rating: –/5 (Dept. average: –/5).

ECE342 – Computer Hardware 2017-2019

- Course covers arithmetic circuits, digital system design, asynchronous logic, testing of logic circuits.
- Winter 2019 enrollment: 74; Instructor rating: 4.4/5 (Dept. average: 3.9/5).
- Winter 2018 enrollment: 87; Instructor rating: 3.7/5 (Dept. average: 3.6/5).
- Winter 2017 enrollment: 94; Instructor rating: 3.8/5 (Dept. average: 3.8/5).

ECE1755 – Parallel Computer Architecture and Programming 2017-2019

- Course covers topics in parallel architecture including cache coherence, memory consistency, interconnection networks, etc.
- Winter 2019 enrollment: 12; Instructor rating: 4.8/5 (Dept. average: 4.2/5).
- Winter 2018 enrollment: 22; Instructor rating: 3.8/5 (Dept. average: 4.1/5).
- Winter 2017 enrollment: 13; Instructor rating: 4.6/5 (Dept. average: 4.4/5).

ECE552 – Computer Architecture 2009-2014, 2018-2019

- Course covers traditional and advanced topics on computer architecture: pipelining, caches, dynamic scheduling, multiprocessors and multi-threading.
- Fall 2019 enrollment: –; Instructor rating: –/5 (Dept. average: –/5).
- Fall 2018 enrollment: 70; Instructor rating: 4.6/5 (Dept. average: 3.9/5).
- Fall 2014 enrollment: 90; Instructor rating: 4.5/5 (Dept. average: 3.9/5).
- Fall 2013 enrollment: 90; Instructor rating: 4.6/5 (Dept. average: 3.8/5).

– Fall 2012 enrollment: 85; Instructor rating: 6.33/7 (Dept. average: 5.72/7).
– Fall 2011 enrollment: 69; Instructor rating: 6.07/7 (Dept. average: 5.86/7).
– Fall 2010 (as ECE452/1718) enrollment: 82; Instructor rating: 5.62/7 (Dept. average: 5.79/7).
– Fall 2009 (as ECE452) enrollment: 34; Instructor rating: 4.61/7 (Dept. average: 5.74/7).

ECE352 – Computer Organization 2017

– Course covers arithmetic circuits, digital system design, assembly language programming, I/O interfaces, processor design, memory systems.
– Fall 2017 enrollment: 51; Instructor rating: 4.1/5 (Dept. average: 3.9/5).

ECE243 – Computer Organization 2011-2015

– A second year course on assembly language and computer organization.
– Winter 2015 enrollment: 117; Instructor rating: 4.1/5 (Dept. average: 3.8/5).
– Winter 2014 enrollment: 90; Instructor rating: 4.1/5 (Dept. average: 3.6/5).
– Winter 2013 enrollment: 114; Instructor rating: 6.00/7 (Dept. average: 5.61/7).
– Winter 2012 enrollment: 110; Instructor rating: 5.62/7 (Dept. average: 5.61/7).
– Winter 2011 enrollment: 91; Instructor rating: 5.44/7 (Dept. average: 5.71/7).

ECE1749 – Interconnection Networks for Parallel Computer Architectures 2010-2014

– Course covers fundamental concepts related to interconnection networks: topology, routing algorithms, flow control and router microarchitecture. The course also exposes students to cutting-edge research in this field.
– Fall 2014 enrollment: 8; Instructor rating: 4.1/5 (Dept. average: 4.2/5).
– Spring 2014 enrollment: 8; Instructor rating: 5.92/7 (Dept. average: 6.14/7).
– Fall 2012 enrollment: 24; Instructor rating: 5.92/7 (Dept. average: 6.14/7).
– Fall 2011 enrollment: 21; Instructor rating: 6.52/7 (Dept. average: 6.09/7).
– Winter 2011 enrollment: 10; Instructor rating: 6.60/7 (Dept. average: 6.23/7).
– Winter 2010 enrollment: 8; Instructor rating: 6.75/7 (Dept. average: 6.07/7).

Student Supervision

Graduated Ph.D. Students

Mario Badr 1/2014 – 10/2019
Thesis: New Tools for Evaluating Parallel and Heterogeneous Architectures
First Employment: Assistant Professor, Computer Science, University of Toronto

Wenbo Dai 9/2011 – 7/2017
Thesis: Network Improvement and Evaluation in Datacenters and Chip-Multiprocessors
First Employment: Intel

Robert Hesse 8/2009 – 12/2015
Thesis: Fine-Grained Adaptivity For Dynamic On-Chip Networks
First Employment: Intel

Parisa Khadem Hamedani 1/2012 – 4/2017
Thesis: Improving Communication in Chip Multiprocessors Using Emerging Technologies and Machine Learning
First Employment: Intel

Joshua San Miguel 5/2012 – 8/2017
Thesis: Reading Between the Bits: Uncovering New Insights in Data for Efficient Processor Design
First Employment: Assistant Professor, University of Wisconsin-Madison

Graduated M.A.Sc. Students

Mario Badr 5/2011 – 1/2014
Thesis: Synthetic Traffic Models That Capture Cache Coherent Behaviour
First Employment: PhD student, University of Toronto

Tahir Diop 9/2011 – 9/2013
Co-supervised ∼50% by Prof. J. Anderson
Thesis: Regression Modelling of Power Consumption for Heterogeneous Processors
First Employment: Software engineer, TXIO

Kai Feng 9/2010 – 9/2012
Thesis: Quality-of-Service for NoC-based Smartphone/Tablet Systems-on-Chip
First Employment: China Electronics Corporation

Karthik Ganesan 1/2016 – 1/2018
Thesis: Sporadic: An Anytime Architecture for Intermittent Computing
First Employment: PhD student, University of Toronto

Steven Gurfinkel 5/2011 – 4/2014
Co-supervised ∼50% by Prof. J. Anderson
Thesis: The Distribution of OpenCL Kernel Execution Across Multiple Devices
First Employment: Engineer, NVIDIA

Ajaykumar Kannan 9/2013 – 9/2015
Thesis: Enabling Interposer-Based Disintegration of Multi-Core Processors
First Employment: Engineer, Altera

Victor Kariofillis 9/2017 – 4/2020
Thesis: Precompression: A Prelude to Cache Compression
First Employment: PhD student, University of Toronto

Henry Kao 9/2017 – 1/2020
Thesis: Cache Coherence for Approximate Computing
First Employment: Engineer, Huawei

Zimo Li 9/2013 – 9/2016
Thesis: The Runahead Network on Chip
First Employment: Engineer, Amazon

Matthew Misler 1/2009 – 6/2010
Thesis: An Exploration of On-Chip Network Based Thread Migration
First Employment: IT Analyst, TD Bank Financial Group

Mark Sutherland 9/2014 – 8/2016
Thesis: Co-Locating Code and Data for Energy-Efficient CPUs
First Employment: PhD Student, EPFL

Danyao Wang 1/2009 – 9/2010
Co-supervised ∼50% by Prof. J. G. Steffan
Thesis: DART: An FPGA-based Accelerator Platform for Network-on-Chip Simulation
First Employment: Software Engineer, Google

Haofan Yang 9/2011 – 9/2013
Thesis: Dodec: A Random-Link Approach for Low-Radix On-Chip Networks
First Employment: Engineer, NVIDIA

Post-Doctoral Researchers

Jorge Albericio Latorre 7/2013 – 8/2016
Co-supervised ∼50% by Prof. A. Moshovos
Topic: Hardware Acceleration for Machine Learning
First Employment: NVIDIA

Current Ph.D. Students

Shehab Elsayed 9/2012 – Present
Topic: Quality of Service for Smartphone Networks-on-Chip

Hossein Farrokbakht 9/2018 – Present
Topic: Efficient Deadlock Avoidance in NoCs

Karthik Ganesan 1/2018 – Present
Topic: Energy Harvesting IoT Architectures

Victor Kariofillis 1/2020 – Present
Topic: TBD

Jiechen Zhao 9/2020 – Present
Topic: TBD

Current M.A.Sc. Students

Kamran Hasan 7/2018 – Present
Topic: Security for Machine Learning Accelerators

Rose Li 9/2017 – Present
Topic: Evaluation of Intermittent Computing Architectures

Evey Liu 1/2019 – Present
Topic: Architectures for Distributed Machine Learning

Iris Uwizeyimana 9/2020 – Present
Topic: TBD

Farhad Yusufali 9/2019 – Present
Topic: Approximate Computing

Visiting International Ph.D. Students

Thierry Moreau 9/2015 – 7/2016
Current Position: PhD Student, University of Washington

Sheng Ma 9/2010 – 9/2012
Current Position: Assistant Professor
National University of Defense Technology, China

M.Eng. Students Supervised

Pulkit Agarwal 9/2018 – 5/2019
Topic: Approximate Computing Techniques for Video Encoding
Current Position: Qualcomm

Remi Dufour 1/2013 – 9/2013
Topic: Multi-core Prefetching Algorithms
Current Position: Apple

Xiaoyin Liu 1/2012 – 6/2012
Topic: Simulation Visualization for Networks-on-Chip

John Matienzo 1/2012 – 10/2012
Topic: Optimized Broadcast Algorithms for the Intel SCC

Current Position: Apple

Undergraduate Research Students

Sophie Mao (NSERC Undergraduate Summer Research Award)	5/2019 – 8/2019
Charley Xu (NSERC Undergraduate Summer Research Award)	5/2019 – 8/2019
Steven Xia	5/2018 – 8/2018
Ziang (Bill) Xing (University of Toronto Excellence Award)	5/2013 – 8/2013
Victor Zhang (NSERC Undergraduate Summer Research Award)	5/2012 – 8/2012
Md Hasan Imam	5/2012 – 8/2012
Daniel Lee	5/2011 – 8/2011
Yifei Liu (ECE Entrance Research Award)	5/2011 – 8/2011
Jeff Nicholls (NSERC Undergraduate Summer Research Award)	5/2011 – 8/2011
Current Position: M.A.Sc. student, University of Toronto	
Jyoti Tripathi	5/2011 – 8/2011
Camille Wingson	5/2011 – 8/2011
Tian Fang Yu	5/2011 – 8/2011
Victor Feng (NSERC Undergraduate Summer Research Award)	5/2010 – 8/2010
Ruolong Lian (NSERC Undergraduate Summer Research Award)	5/2010 – 8/2010
Current Position: M.A.Sc. student, University of Toronto	
Thierry Moreau (NSERC Undergraduate Summer Research Award)	5/2009 – 8/2009
Current Position: Ph.D. student, University of Washington	

Graduate Student PhD Defence Committees

Sayeh Sharify (Supervisor: Andreas Moshovos), 2020

Alex Rodionov (Supervisor: Jonathan Rose), 2019

Mostafa Mahmoud (Supervisor: Andreas Moshovos), 2019

Patrick Judd (Supervisor: Andreas Moshovos), 2018

Myrto Papadopoulou (Supervisor: Andreas Moshovos), 2017

Jasmina Vasiljevic (Supervisor: Paul Chow), 2017

Henry Wong (Supervisors: Vaughn Betz and Jonathan Rose), 2017

Mohammed Abdelfattah (Supervisor: Vaughn Betz), 2016

Islam Atta (Supervisor: Andreas Moshovos), 2015

Marcel Gort (Supervisor: Jason Anderson), 2014

Jason Zebchuk (Supervisor: Andreas Moshovos), 2013

Ioana Burcea (Supervisor: Andreas Moshovos), 2012

Utku Aydonat (Supervisor: Tarek Abdelrahman), 2011

Peter Yiannacouras (Supervisors: Jonathan Rose and Greg Steffan), 2009

Mentoring and Outreach

Panelist

"After Tenure", MIT EECS Rising Stars Workshop, October 2018.

"Work-Life Balance", hosted by the University of Toronto Prospective Professor in Training Program, March 2018.

"3^{rd} year review and tenure process", workshop organized by the Office of the Vice-Provost, University of Toronto, 2015.

"Career Workshop for Women and Minorities in Computer Architecture", held in conjunction with MICRO, 2014.

"Academia and Industry Crossroads" at the University of Toronto ECE Connections Symposium, 2014.

"Being an Engineering Professor" hosted by the University of Toronto Prospective Professor in Training Program, April 2013.

"What if... You Thrived on the Tenure Track?" at Grace Hopper Celebraton of Women in Computing, 2011.

"Campus visit, interview and more" at Positioning Yourself for a Career in Academia hosted by the Status of Women Office at the University of Toronto, April 2010.

Chair: Women in Computer Architecture Group (WICARCH), 2011-Present

International membership consisting of professors, industry researchers and students in the field of computer architecture.

Organize annual networking events at major computer architecture conferences (ISCA and MICRO).

Organize monthly webinar featuring prominent and emerging female researchers in computer architecture.

Run online mentoring and community-building platform.

`http://www.sigarch.org/wicarch`

ECE Representative: Girls Leadership in Engineering Experience (GLEE) Dinner for prospective undergraduate students, 2013, 2014, 2018, 2019.

Speaker: CRA-W Graduate Cohort, April 2013

Co-Organizer: CRA-W/CDC Computer Architecture Discipline Specific Mentoring Workshop, August 2012

Co-Organizers: Hillery Hunter (IBM), Russ Joseph, (Northwestern), Li-Shiuan Peh (MIT), Kelly Shaw (University of Richmond)

Received funding support from CRA-W/CDC and ACM SIGARCH, ACM SIGMICRO, AMD, IBM, Intel, Microsoft, Google, Oracle Labs, and VMware

High School Outreach

Speaker, Fall Campus Day, October 2014

Speaker, Fall Campus Day, October 2013

Lester B. Pearson Collegiate Institute: Presentation on ECE to Grade 10 Computer Science class, April 2012

Bishop Strachan School: Presentation on ECE to Grade 11 Physics class, March 2012.

Bishop Strachan School: Presentation on ECE to Grade 11 Physics class, January 2011.

CRA-W/CDC Distinguished Lecture Series Organizer for University of Toronto, 2010

Speakers: Margaret Martonosi (Princeton) and Jaime Moreno (IBM)

Professional Service

Co-Chair

ACM Council on Diversity and Inclusion, 2019-Present

Executive Committee

ACM Special Interest Group on Architecture (SIGARCH), Vice Chair, 2019-Present

ACM Special Interest Group on Architecture (SIGARCH), 2015-2019

IEEE Technical Committee on Computer Architecture (TCCA), 2015-2018

ACM Special Interest Group on Microarchitecture (SIGMICRO), Vice Chair, 2017-2020

Editor

Morgan Claypool Synthesis Lectures on Computer Architecture, 2019–Present

Program Chair

20th International Symposium on High Performance Computer Architecture (HPCA), 2014

Program Co-Chair
7th ACM/IEEE International Symposium on Networks-on-Chip, 2013

Steering Committee Member
International Symposium on Microarchitecture (MICRO), 2018–Present
International Symposium on High Performance Computer Architecture (HPCA), 2014–2018
International Symposium on Networks-on-Chip (NOCS), 2013–Present

Discovery Grant Evaluation Group Member: Electrical and Computer Engineering, 2016-2019
Natural Sciences and Engineering Research Council of Canada
Section Chair, 2018, 2019

Associate Editor in Chief
IEEE Computer Architecture Letters, 2019-Present

Associate Editor
ACM Transactions on Architecture and Code Optimization, 2013-2018
IEEE Computer Architecture Letters, 2014-2019
IEEE Transactions on Computers, 2015-Present

Guest Co-Editor
IEEE MICRO Special Issue on Approximate Computing, July/August 2018 (w/ Joshua San Miguel, University of Wisconsin-Madison)
IEEE MICRO Special Issue on Systems for Very Large Scale Computing, May/June 2011 (w/ Mikko Lipasti, University of Wisconsin-Madison)

Committee Member
IEEE Mildred Dresselhaus Medal Committee, 2020-Present
ACM SIGARCH/IEEE CS TCCA Outstanding Dissertation Award, 2019-Present (Chair, 2019)
IEEE Computer Society Awards Committee, 2017-2020
IEEE International Symposium on High Performance Computer Architecture Test of Time Award, 2018-Present (Chair, 2018)
IEEE Computer Society B. Ramakrishna Rau Award Committee, 2017-2018

Track Co-Chair
International Conference on Computer Design, Computer Systems and Applications Track, 2013
Canadian Conference on Electrical and Computer Engineering, Computer, Software and Applications Track, 2011

Student Travel Grants Co-Chair
International Symposium on Computer Architecture, 2017

Industrial Liaison
International Symposium on Computer Architecture, 2016

Finance Chair
International Symposium on Computer Architecture, 2015

Workshop/Tutorials Chair
International Conference on Parallel Architecture and Compilation Techniques, 2013

International Symposium on Performance Analysis of Systems and Software, 2013

Publicity Chair

International Symposium on Computer Architecture (ISCA), 2014

International Symposium on Code Generation and Optimization (CGO), 2010

Instructor, 8th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, 2012

4-day course: Networks-on-Chip: Communication challenges for many-core architectures

Workshop Co-Organizer

11th Workshop on Duplicating, Deconstructing and Debunking (held with ISCA-41)

10th Workshop on Duplicating, Deconstructing and Debunking (held with ISCA-39)

9th Workshop on Duplicating, Deconstructing and Debunking (held with ISCA-38)

8th Workshop on Duplicating, Deconstructing and Debunking (held with ISCA-36)

Session Chair

International Symposium on Computer Architecture (ISCA), June 2018

International Symposium on Computer Architecture (ISCA), June 2017

International Symposium on Computer Architecture (ISCA), June 2015

International Symposium on Microarchitecture (MICRO), December 2014

International Symposium on Networks on Chip (NOCS), September 2014

International Conference on Parallel Architectures and Compilation Techniques (PACT), August 2014

International Symposium on Computer Architecture (ISCA), June 2013

International Symposium on High Performance Computer Architecture (HPCA), February 2012

External Reviewer

NSERC Discovery Grants, Electrical and Computer Engineering Committee: 2011, 2012, 2013, 2015, 2021

Panelist

National Science Foundation (US), Computing and Communication Foundations (CCF) Grant Review Panel, 2012

National Science Foundation (US), Joint Computing and Communication Foundations (CCF)/ Computer and Network Systems (CNS) Grant Review Panel, 2011

Program Committee (Conferences)

Intl. Symposium on Computer Architecture (ISCA)	2013, 2015, 2017, 2018, 2020
Intl. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)	2017, 2018
Intl. Symposium on Microarchitecture (MICRO)	2011, 2016, 2017, 2019
Intl. Symposium on Workload Characterization (IISWC)	2016
IEEE Micro Top Picks	2013, 2015, 2019
Intl. Symposium on High Performance Computer Architecture (HPCA)	2012, 2013, 2015, 2016
Intl. Symposium on Networks-on-Chip (NOCS)	2014, 2015, 2016, 2017
Intl. Conference for High Performance Computing, Networking, Storage and Analysis (SC)	2014
Intl. Conference on Parallel Architectures and Compilation Techniques (PACT)	2010, 2014
Intl. Conference on Supercomputing (ICS)	2011, 2014
Intl. Conference on Parallel Processing (ICPP)	2010, 2013

Intl. Parallel and Distributed Processing Symposium (IPDPS) 2011, 2012, 2013
Intl. Conference on Computer Design (ICCD) 2009, 2010, 2011, 2012
Intl. Symposium on Performance Analysis of Software and Systems (ISPASS) 2011, 2012
Intl. Conference on Computer Aided Design (ICCAD) 2009, 2010
Intl. Conference on Design Automation and Test in Europe (DATE) 2010

Program Committee (Workshops)

General Purpose Processing Using GPUs (at ASPLOS) 2013
Interconnection Network Architectures: On-Chip, Multi-Chip (at HiPEAC) 2011, 2012, 2013
Communication Architecture for Scalable Systems (CASS) (at IPDPS) 2011, 2012, 2013
Network on Chip Architectures (at MICRO) 2009, 2010, 2011, 2012, 2013
Chip Multiprocessor Memory Systems and Interconnects (at ISCA, HPCA) 2009, 2010

External Review Committee

International Symposium on Computer Architecture (ISCA) 2019
International Conference o Parallel Architecture and Compilation Techniques (PACT) 2018
International Symposium on High Performance Computer Architecture (HPCA) 2017
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2010, 2013, 2015, 2016
Internationl Symposium on Microarchitecture (MICRO) 2014
Intl. Conf. on High-Performance and Embedded Architectures and Compilers (HiPEAC) 2012, 2013

Reviewer for Conference and Journals

Journals: IEEE Micro, ACM Transactions on Computers, IEEE Transactions on Computers, IEEE Transactions in VLSI, IEEE Computer Architecture Letters, ACM Transactions on Embedded Computing Systems, ACM Transactions on Architecture and Code Optimization, Journal of Parallel and Distributed Computing, IEEE Journal of Emerging and Selected Topics in Circuits and Systems, Transactions on Computer Aided Design, ACM Computing Surveys, ACM Transactions on Design Automation of Electronic Systems, IEEE Systems Journal, Canadian Journal of Electrical and Computer Engineering, Journal of Optical Communications and Networking, IEEE Transactions on Parallel and Distributed Computing

Cited as a 'Top Reviewer' in 2013 for IEEE Transactions on Computers

Conferences: International Symposium on Microarchitecture, International Symposium on Computer Architecture, International Conference on Architectural Support for Programming Languages and Operating Systems, International Conference on Parallel Architectures and Compilation Techniques, International Conference on Supercomputing, International Symposium on Parallel Algorithms and Architectures, International Conference on Parallel Processing, International Conference on Computer Design, International Conference on Computer Aided Design, International Symposium on High Performance Computer Architecture, International Symposium on Performance Analysis of Systems and Software, International Symposium on Circuits and Systems, Grace Hopper Celebration

Professional Memberships

IEEE, IEEE Computer Society, Technical Commitee on Computer Architecture (TCCA)
Fellow (2021)

ACM, SIGARCH, SIGMICRO
Distinguished Member (2018)

Licensed Professional Engineer (P.Eng.) in Ontario

University Service

Member
ECE Director of Faculty Recruiting 2019-2023

ECE Faculty Search Committee (Chair), 2019

Advisory Committee on the Appointment of ECE Chair, 2019

Advisory Committee for the Dean of the Faculty of Applied Science & Engineering, 2018-2019

ECE Advisory Committee (Computer Group Chair), 2018-Present

ECE Faculty Search Committee (Chair), 2018

ECE Promotion Through the Ranks (PTR) Committee, 2016-2019

ECE Department Space Committee, 2014-2015

Advisory Committee on the Appointment of ECE Chair, 2013

Community Affairs and Gender Issues Committee, Faculty of Applied Science and Engineering, 2010-2014

Vice-Chair

Community Affairs and Gender Issues Committee, Faculty of Applied Science and Engineering, 2010-2011, 2012-2013, 2013-2014 (acting chair)

Faculty Advisor

Mechatronics Design Association, 2014-2016