Natalie Enright Jerger

| CONTACT INFORMATION | The Edward S. Rogers Department of Electrical and Computer Engineering
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Webpage: www.eecg.toronto.edu/~enright |

EDUCATION

University of Wisconsin, Madison, Wisconsin USA

    Ph.D., Electrical Engineering, December 2008

        Dissertation: "Chip Multiprocessor Coherence and Interconnect System Design"
        Advisors: Mikko H. Lipasti and Li-Shiuan Peh

    M.S., Electrical and Computer Engineering, May 2004

Purdue University, West Lafayette, Indiana USA

    B.S., Computer Engineering, May 2002

APPOINTMENT

University of Toronto, Electrical and Computer Engineering, Toronto, Ontario, Canada
Assistant Professor   **January 2009 - present**

RESEARCH INTERESTS

Computer architecture, many-core architectures, on-chip networks, cache coherence protocols, interconnection networks, emerging applications for many-core architectures.

INDUSTRIAL EXPERIENCE

| IBM | Intern |
| Rochester, MN | June 2006 - Oct 2006 |

| Intel | Intern, Microarchitecture Research Lab |
| Santa Clara, CA | May 2004 - December 2004 |

| Hewlett Packard | Intern |
| Vancouver, WA | May 2001 - August 2001 |

| Hewlett Packard | Intern |
| Vancouver, WA | May 2000 - August 2000 |

HONORS AND AWARDS

Ministry of Research and Innovation Early Researcher Award, 2012

IBM Ph.D. Fellowship, 2008

IBM Ph.D. Fellowship, 2007

Peter R. Schneider Distinguished Graduate Fellowship, University of Wisconsin-Madison, 2002

University of Wisconsin Teaching Academy Future Faculty Partner, 2004-2008

PUBLICATIONS PEER-REVIEWED CONFERENCES

[C1] **Tahir Diop, Steven Gurfinkel**, Jason Anderson and Natalie Enright Jerger. "DistCL: A Framework for Distributed Execution of OpenCL Kernels." *In Proceedings of the International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS).* August 2013 (acceptance rate: 27%). Citations:1[1][2].

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[1]Student authors identified in bold.
[2]Citations from Google Scholar.

[C2] **John Matienzo** and Natalie Enright Jerger. "Performance Analysis of Broadcasting Algorithms on the Intel Single Chip Cloud Computer." *In Proceedings of the International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2013, pp. 163-172. (acceptance rate: 26%).

[C3] **Michel El Nacouzi, Islam Atta, Myrto Papadopoulou, Jason Zebchuk**, Natalie Enright Jerger and Andreas Moshovos. "A Dual-Grain Hit/Miss Detector for Large Stacked Die DRAM Caches." *In Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, March 2013, pp. 89-92. (acceptance rate: 36%). Citations: 1.

[C4] **Robert Hesse, Jeff Nicholls** and Natalie Enright Jerger. "Fine-Grained Bandwidth Adaptivity in Networks-on-Chip Using Bidirectional Channels." *In Proceedings of the 6th International Network on Chip Symposium (NOCS)*, May 2012, pp. 132-141. (acceptance rate: 30%). Citations: 3.

[C5] **Sheng Ma**, Natalie Enright Jerger and Zhiying Wang. "Whole Packet Forwarding: Efficient Design of Fully Adaptive Routing Algorithms for Networks-on-Chip." *In Proceedings of the 18th International Symposium on High Performance Computer Architecture (HPCA)*. Feb. 2012, pp. 467-479. (acceptance rate: 17%). Citations: 13.

[C6] **Sheng Ma**, Natalie Enright Jerger and Zhiying Wang. "Supporting Efficient Collective Communication in NoCs." *In Proceedings of the 18th International Symposium on High Performance Computer Architecture (HPCA)*. Feb. 2012, pp. 165-177. (acceptance rate: 17%). Citations: 7.

[C7] **Parisa Khadem Hamedani**, Shaahin Hessabi, Hamid Sarbazi-Azad and Natalie Enright Jerger. "Exploration of Temperature Constraints for Thermal Aware Mapping of 3D Networks on Chip." *In Proceedings of the 20th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP)*. Feb. 2012, 499-506. (acceptance rate: 34%). Citations 2.

[C8] **Sheng Ma**, Natalie Enright Jerger, and Zhiying Wang. "DBAR: An Efficient Routing Algorithm to Support Multiple Concurrent Applications in Networks-on-Chip." *In Proceedings of the 38th International Symposium on Computer Architecture (ISCA)*. June 2011, pp. 413-424. (acceptance rate: 19%). Citations: 43.

[C9] **Danyao Wang**, Natalie Enright Jerger, and J. Gregory Steffan. "DART: A Programmable Architecture for NoC Simulation on FPGAs." *In Proceedings of the 5th International Network on Chip Symposium (NOCS)*. May 2011, pp 145-152. (acceptance rate: 25%). Citations: 9.

[C10] Natalie Enright Jerger. "SigNet: Network-on-Chip Filtering for Coarse Vector Directories." *In Proceedings of the International Conference on Design Automation and Test in Europe (DATE)*. March 2010, pp. 1378-1383. (acceptance rate: 26%). Citations: 6.

[C11] **Mitch Hayenga**, Natalie Enright Jerger and Mikko Lipasti. "SCARAB: A Single Cycle Adaptive Routing and Bufferless Network." *In Proceedings of the 42nd International Symposium on Microarchitecture (MICRO)*. New York, New York. Dec. 2009, pp. 244-254. (acceptance rate: 25%). Citations: 71.

[C12] Dennis Abts, Natalie Enright Jerger, John Kim, Mikko Lipasti and **Dan Gibson**. "Achieving Predictable Performance through Better Memory Controller Placement in Many-Core CMPs." *In Proceedings of the 36th International Symposium on Computer Architecture (ISCA)*. June 2009, pp. 451-461. (acceptance rate: 20%). Citations: 64.

[C13] Natalie Enright Jerger, Li-Shiuan Peh and Mikko H. Lipasti. "Virtual Tree Coherence: Leveraging Regions and In-Network Multicast Trees for Scalable Cache Coherence." *In Proceedings of the 41st International Symposium on Microarchitecture (MICRO)*. Nov. 2008, pp. 35-46. (acceptance rate: 19%). Citations: 67.

[C14] Natalie Enright Jerger, Li-Shiuan Peh and Mikko H. Lipasti. "Virtual Circuit Tree Multicasting: A Case for On-Chip Hardware Multicast Support." *In Proceedings of the 35th International Symposium on Computer Architecture (ISCA)*. Beijing, China. June 2008, pp. 229-240. (acceptance rate: 14%). Citations: 134.

[C15] Natalie Enright Jerger, Li-Shiuan Peh and Mikko H. Lipasti. "Circuit-Switched Coherence." *In Proceedings of the 2nd Network on Chip Symposium (NOCS)*. April 2008, pp. 193-202. (acceptance rate: 32%). Citations: 70.

[C16] Natalie Enright Jerger, Dana Vantrease and Mikko Lipasti. "An Evaluation of Server Consolidation Workloads for Multi-Core Designs." *In Proceedings of IEEE International Symposium on Workload Characterization (IISWC)*. Sept. 2007, pp. 47-56. (acceptance rate: 40%). Citations: 46.

[C17] Natalie Enright Jerger, Eric Hill, and Mikko Lipasti. "Friendly Fire: Understanding the Effects of Multiprocessor Prefetches." *In Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*. March 2006, pp. 177-188. (acceptance rate: 30%). Citations: 10.

PUBLICATIONS
PEER-REVIEWED
JOURNALS

[J1] **Sheng Ma**, Zhiying Wang, Zonglin Liu and Natalie Enright Jerger. "Leaving One Slot Empty: Flit Bubble Flow Control for Torus Cache-coherent Networks-on-Chip." *IEEE Transactions on Computers*. (manuscript submitted: November 2012, revised: July 2013, accepted December 2013).

[J2] **Sheng Ma**, Zhiying Wang, Natalie Enright Jerger, Li Shen and Nong Xiao. "Novel Flow Control for Fully Adaptive Routing in Cache-coherent NoCs." *IEEE Transactions on Parallel and Distributed Computing*. (manuscript submitted: January 2013, revised: April 2013, accepted: June 2013).

[J3] **Parisa Khadem Hamedani**, Shaahin Hessabi, Hamid Sarbazi-Azad and Natalie Enright Jerger. Exploration of Temperature Constraints for Thermal Aware Mapping of 3D Networks on Chip. International Journal of Adaptive, Resilient and Automonic Systems, Special issue on Networked Embedded Systems. (manuscript submitted: April 2012, revised: July 2012, accepted: September 2012).

[J4] **Sheng Ma**, Natalie Enright Jerger, Zhiying Wang, Mingche Lai, and Libo Huang. Holistic Routing Algorithm Design to Support Workload Consolidation in NoCs. IEEE Transactions on Computers. (manuscript submitted: October 2011, revised: May 2012, accepted: August 2012).

[J5] **Danyao Wang, Charles Lo, Jasmina Vasiljevic**, Natalie Enright Jerger and J. Gregory Steffan. DART: A Programmable Architecture for NoC Simulation on FPGAs. IEEE Transactions on Computers. (manuscript submitted: October 2011, revised: April 2012, accepted: May 2012).

[J6] **Matthew Misler** and Natalie Enright Jerger. Moths: Mobile Threads for On-Chip Networks. In ACM Transactions on Embedded Computing. (manuscript submitted: March 2011, revised: August 2011, accepted: December 2011, published: March 2013).

[J7] Radu Marculescu, Umit Ogras, Li-Shiuan Peh, Natalie Enright Jerger and Yatin Hoskote. Outstanding Research Problems in NoC Design: Circuit-, Microarchitecture- and System-Level Perspective. In IEEE Transactions on Computer-Aided Design, vol. 28, no. 1, pp. 3-21, 2009. (Most downloaded article in Transactions on Computer-Aided Design of 2009.) Citations: 338.

[J8] Natalie Enright Jerger, Mikko Lipasti and Li-Shiuan Peh. Circuit-Switched Coherence. IEEE Computer Architecture Letters, vol. 6, no. 1, Mar. 2007. Citations: 5.

[J9] Elizabeth M. O'Callaghan and Natalie Enright Jerger. Women and Girls in Science and Engineering: Understanding the Barriers to Recruitment, Retention and Persistence across

the Educational Trajectory. Journal of Women and Minorities in Science and Engineering, vol. 12, no. 2-3, pp. 209–232, 2006. Citation: 5.

PUBLICATIONS
BOOK

[P1] Natalie Enright Jerger and Li-Shiuan Peh. "On-Chip Networks", Synthesis Lecture in Computer Architecture. (Editor: Mark Hill). Morgan & Claypool Publishers. July 2009, 142 pages. (downloaded over 2900 times as of September 2013). Citations: 56.

PUBLICATIONS
WORKSHOP &
POSTERS

[P2] **Wenbo Dai** and Natalie Enright Jerger. "Accelerating Network-on-Chip Simulation via Sampling". In *International Symposium on Performance Analysis of Systems and Software* (poster). March 2014.

[P3] **Sam Vafaee** and Natalie Enright-Jerger. "C++ Front-End for Distributed Transactional Memory." In the Intel Symposium on Single-Chip Cloud Computing. March 2011

[P4] **Matthew Misler** and Natalie Enright-Jerger. "Moths: Mobile Threads for On-Chip Network", Intl Conf. on Parallel Architectures and Compilation Techniques (poster). Sept 2010. Citations: 1

[P5] **Danyao Wang**, Natalie Enright Jerger, J. Gregory Steffan. "DART: Fast and Flexible NoC Simulation Using FPGAs," 5th Annual Workshop on Architectural Research Prototyping, June 2010. Citations: 6

PUBLICATIONS
NON-REVIEWED

[P6] Natalie Enright Jerger, "Explaining Parallel Architecture Design", Book Review: Parallel Computer Organization and Design, Computing in Science and Engineering, 2013 (to appear).

[P7] Natalie Enright Jerger and Mikko Lipasti, "Systems for Very Large-Scale Computing," IEEE MICRO Special Issue (guest editors' introduction), Vol. 31, No. 3, pp. 4-7, 2011.

PUBLICATIONS
PATENT

[P8] Natalie D. Enright[3], Jamison Collins, Perry Wang, Hong Wang, Xinmin Tran, John Shen, Gad Sheaffer, Per Hammarlund. Mechanism to exploit synchronization overhead to improve multithread performance. Patent no: 7487502. Sept 2009. Assignee: Intel Corporation. Citations 3.

PUBLICATIONS
SUMMARY &
IMPACT

Career Totals

Total Publications: 34	
Refereed conference papers (published)	17
Refereed journal papers (published)	9
Other publications (non-refereed)[1]	8

[1] Non-refereed articles include posters, workshop papers, patents and invited articles

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[3]Issued under maiden name

Top Cited and Citations Summary								
Paper:	[J7]	[C14]	[C11]	[C15]	[C13]	[C12]	[P1]	[C16]
Count:	338	134	71	70	67	64	56	46
Total citations (all papers)								966
Average citations per paper								28.41
h-index								10
i10-index								11

SOFTWARE ARTIFACTS RELEASED

DART: An FPGA Network-on-Chip Simulation Acceleration Engine
Released: May 2011
Downloads to date: 143.

DistCL: A Framework for Distributed Execution of OpenCL Kernels
Released: August 2013
Downloads to date: 7.

INVITED TALKS

Designing High Performance, Energy-Efficient Networks-on-Chip
    University of Wisconsin-Madison, November 2013

    Google (Madison), November 2013

Optimizations for Cache-Coherent Networks-on-Chip
    University of Washington, April 2013

    AMD Research, April 2013

    MIT, April 2013

    Texas A&M University, March 2013

    Cornell University, March 2013

    University of Illinois, March 2013

    University of Michigan, February 2013

    Northwestern University, January 2013

Accelerating Many-Core Network-on-Chip Simulation
    Intel Corporation, January 2013

Reactive Coherence-based Traffic Models
    Intel Corporation, January 2012

Towards Application-Aware Network-on-Chip Architectures
    McMaster University, March 2012

    Intel Corporation, November 2011

    IBM T.J. Watson, June 2011

    University of Waterloo, ECE Department, March 2011

    Qualcomm, November 2010

On-Chip Network Research: Opportunities to Leverage Platform 2012
    Research Workshop on STMicroelectronics Platform 2012 (organized by CMC Microsystems), November 2010

Outstanding Research Challenges in On-Chip Networks

Altera Corporation, Toronto ON, June 2009.

Virtual Tree Coherence: Leveraging Regions and In-Network Multicast Trees for Scalable Cache Coherence
International Symposium on Microarchitecture, November 2008.

12th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2008.

Gigascale Systems Research Center, Quarterly Concurrent Theme Meeting, June 2008.

Virtual Circuit Tree Multicasting: A Case for On-Chip Hardware Multicast Support
International Symposium on Computer Architecture, June 2008

Harnessing Computing Power through Communication
Computer Science and Engineering Colloquium, Washington University in St. Louis, April 2008

Computer Engineering Group, University of Toronto, March 2008

Virtual Proximity: Interconnect Support for Flexible Scheduling of Server Consolidation Workloads in CMPs
IBM Research Triangle Park, October 2007

11th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2007

An Evaluation of Server Consolidation Workloads for Multi-Core Designs
IEEE International Symposium on Workload Characterization, Boston MA, September 2007

Circuit-Switched Coherence
2nd Annual IEEE Network on Chip Symposium, April 2008

10th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2006

IBM Austin Research Lab, October 2006

Friendly Fire: Understanding the Effects of Multiprocessor Prefetches
IEEE Symposium on Performance Analysis of Systems and Software, March 2006

8th Annual Wisconsin Architecture Industrial Affiliates Meeting, October 2004

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FUNDING AND
SUPPORT

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- **Evaluation of Direct Interconnect Architectures for Datacenters** 2013
  Source of support: Natural Sciences and Engineering Research Council, Engage Grant (sole PI)
  Total amount: $25,000
  Annual amount: $25,000
  Annual amount/PI: $25,000

- **Power-Efficient Heterogeneous Architectures** 2012
  Source of support: Ontario Centres of Excellence (OCE) and AMD (PI w/ J. Anderson)
  Total amount: $25,000 (OCE) + $20,000 (AMD)
  Annual amount: $45,000
  Annual amount/PI: $22,500

- **High Performance Many-Core Architectures and Interconnection Networks** 2012-2017
  Source of support: Ministry of Research and Innovation, Early Researcher Award (sole PI)
  Total amount: $140,000
  Annual amount: $28,000
  Annual amount/PI: $28,000

- **Data Supply Architectures for Smartphone and Tablet Devices** 2011-2014
  Source of support: Natural Sciences and Engineering Research Council, Collaborative Research and Development Grant (co-PI w/ A. Moshovos and T. Aamodt (UBC))
  Total amount: $171,212

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Annual amount: $57,070
Annual amount/PI: $19,023

- **Data Supply Architectures for Smartphone and Tablet Devices** 2011-2014
  Source of support: Qualcomm (co-PI w/ A. Moshovos and T. Aamodt (UBC))
  Total amount: $150,000
  Annual amount: $50,000
  Annual amount/PI: $16,667

- **Developing, Analyzing and Accelerating Smartphone Workloads** 2011-2014
  Source of support: Natural Science and Engineering Research Council (co-PI w/ A. Moshovos
  and K. Kutulakos)
  Total amount: $507,590
  Annual amount: $169,196
  Annual amount/PI: $56,399

- **On-Chip Networks to Enable Exascale Computing** 2011-2012
  Source of support: Connaught New Researcher Award (sole PI)
  Total amount: $50,000
  Annual amount: $25,000
  Annual amount/PI: $25,000

- **Next Generation FPGA Platforms** 2011-2013
  Source of support: Fujitsu Labs (co-PI w/ A. Sheikholeslami and J. Anderson)
  Total amount: $297,000
  Annual amount: $148,500
  Annual amount/PI: $49,500

- **Early-Stage Coherence Modeling for On-Chip Network Performance and Power Analysis** 2011-2014
  Source of support: Intel University Research Office (sole PI)
  Total amount: $171,000
  Annual amount: $57,000
  Annual amount/PI: $57,000

- **Applications Exploiting Heterogeneous Processor Architectures for Improved Throughput and Energy-Efficiency** 2011
  Source of support: Natural Sciences and Engineering Research Councile, Engage Grant (PI w/
  J. Anderson)
  Total amount: $24,940
  Annual amount: $24,940
  Annual amount/PI: $12470

- **Multi-core applications, architectures and algorithms for complex systems** 2011-2016
  Source of support: Canadian Foundation for Innovations (co-PI w/ Z. Tate and J. Anderson)
  Total amount: $291,789
  Annual amount: $58,357
  Annual amount/PI: $19,452

- **Multi-core applications, architectures and algorithms for complex systems** 2011-2016
  Source of support: Ministry of Research and Innovation, Ontario Research Fund (co-PI, w/ Z.
  Tate and J. Anderson)
  Total amount: $291,785
  Annual amount: $58,356
  Annual amount/PI: $19,452

- **Heterogeneous Multi-Core Architectures** 2010
  Source of support: AMD (PI w/ J. Anderson)
  Total amount: $20,000 + Donation of 2 ATI Graphics Cards

Annual amount: $20,000
Annual amount/PI: $10,000

- **Exploiting Efficient Communication in the SCC**   2010
  Source of support: Intel Corporation (PI w/ G. Steffan)
  In-Kind Contribution: Access to the Intel Single-Chip Cloud Computer (consists of 48 IA-32
  cores on a single die with 4 memory controllers and a 4×6 mesh on-chip network)

- **Hybrid NoC/Crossbar Designs for SoC Fabrics**   2010
  Source of support: Natural Sciences and Engineering Research Council, Engage Grant (sole PI)
  Total amount: $23,580
  Annual amount: $23,580
  Annual amount/PI: $23,580

- **Integrated Photonics for Energy-Efficient Multi-Core Processors**   2010-2013
  Source of support: Natural Science and Engineering Research Council, Strategic Project Grant
  (co-PI w/ J. Poon, A. Moshovos, A. Leon-Garcia)
  Total amount: $533,100
  Annual amount: $177,700
  Annual amount/PI: $44,425

- **Semantically Rich Networks for Many-Core Architectures**   2009-2014
  Source of support: Natural Sciences and Engineering Research Council, Discovery Grant (sole
  PI)
  Total amount: $135,000
  Annual amount: $27,000
  Annual amount/PI: $27,000

- **Communication-centric Many-Core Computing Architectures**   2009
  Source of support: Connaught Fund (sole PI)
  Total amount: $10,000
  Annual amount: $10,000
  Annual amount/PI: $10,000

- **Start-Up Funds**   2009
  Source of support: University of Toronto (sole PI)
  Total amount: $100,000

TEACHING

Instructor ratings below refer to the "Overall Rating as an Instructor" question on the anonymous
course evaluations filled out by students at the end of the semester.

- **ECE552 – Computer Architecture**   2009-Present

  - Course covers traditional and advanced topics on computer architecture: pipelining, caches,
    dynamic scheduling, multiprocessors and multi-threading.
  - Fall 2012 enrollment: 85; Instructor rating: 6.33/7 (Dept. average: 5.72/7).
  - Fall 2011 enrollment: 69; Instructor rating: 6.07/7 (Dept. average: 5.86/7).
  - Fall 2010 (as ECE452/1718) enrollment: 82; Instructor rating: 5.62/7 (Dept. average:
    5.79/7).
  - Fall 2009 (as ECE452) enrollment: 34; Instructor rating: 4.61/7 (Dept. average: 5.74/7).

- **ECE243 – Computer Organization**   2011-Present

  - A second year course on assembly language and computer organization.
  - Winter 2013 enrollment: 114; Instructor rating: 6.00/7 (Dept. average: 5.61/7).
  - Winter 2012 enrollment: 110; Instructor rating: 5.62/7 (Dept. average: 5.61/7).
  - Winter 2011 enrollment: 91; Instructor rating: 5.44/7 (Dept. average: 5.71/7).

- **ECE1749 – Interconnection Networks for Parallel Computer Architectures**

  2010-Present

  - Course covers fundamental concepts related to interconnection networks: topology, routing algorithms, flow control and router microarchitecture. The course also exposes students to cutting-edge research in this field.
  - Fall 2012 enrollment: 24; Instructor rating: 5.92/7 (Dept. average: 6.14/7).
  - Fall 2011 enrollment: 21; Instructor rating: 6.52/7 (Dept. average: 6.09/7).
  - Winter 2011 enrollment: 10; Instructor rating: 6.60/7 (Dept. average: 6.23/7).
  - Winter 2010 enrollment: 8; Instructor rating: 6.75/7 (Dept. average: 6.07/7).

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STUDENT
SUPERVISION

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Graduated M.A.Sc. Students

Tahir Diop   9/2011 – 9/2013
Co-supervised ∼50% by Prof. J. Anderson
Thesis: Regression Modelling of Power Consumption for Heterogeneous Processors
First Employment: Software engineer, TXIO

Kai Feng   9/2010 – 9/2012
Thesis: Quality-of-Service for NoC-based Smartphone/Tablet Systems-on-Chip
First Employment: China Electronics Corporation

Matthew Misler   1/2009 – 6/2010
Thesis: An Exploration of On-Chip Network Based Thread Migration
First Employment: IT Analyst, TD Bank Financial Group

Danyao Wang   1/2009 – 9/2010
Co-supervised ∼50% by Prof. J. G. Steffan
Thesis: DART: An FPGA-based Accelerator Platform for Network-on-Chip Simulation
First Employment: Software Engineer, Google

Haofan Yang   9/2011 – 9/2013
Thesis: Dodec: A Random-Link Approach for Low-Radix On-Chip Networks
First Employment: Engineer, NVIDIA

Post-Doctoral Researchers

Jorge Albericio Latorre   7/2013 – Present
Co-supervised ∼50% by Prof. A. Moshovos
Topic: Memory Optimizations for Smartphone Platforms

Current Ph.D. Students

Neha Agarwal (University of Michigan)   8/2012 – Present
Co-supervised ∼50% by Prof. T. Wenisch, University of Michigan
Topic: Switch Allocation Optimizations for Networks-on-Chip

Wenbo Dai   9/2011 – Present
Topic: Simulation Acceleration Techniques for Networks-on-Chip

Shehab Elsayed   9/2012 – Present
Topic: Quality of Service for Smartphone Networks-on-Chip

Robert Hesse   8/2009 – Present
Topic: Reconfigurable Communication Architectures

Parisa Khadem Hamedani   1/2012 – Present
Co-supervised ∼25% by Prof. S. Hessabi, Sharif University
Topic: Novel Optical On-Chip Network Topologies

Current M.A.Sc. Students

Mario Badr   5/2011 – Present
    Topic: Synthetic Traffic Models for Cache Coherent Systems

Latch Dimitrov   6/2011 – Present
    Topic: Interconnect Architectures for Multi-FPGA Systems

Steven Gurfinkel   5/2011 – Present
    Co-supervised ∼50% by Prof. J. Anderson
    Topic: Workload Scheduling for Heterogeneous Architectures

Zimo Li   9/2013 – Present
    Co-supervised ∼50% by Prof. J. G. Steffan
    Topic: Heterogeneous Silicon Interposer System-on-Chip Architectures

Ajaykumar Kannan   9/2013 – Present
    Topic: Silicon Interposer-Based Architectures

Joshua San Miguel   5/2012 – Present
    Topic: Optimizations for Multi-Plane NoCs

Visiting International Ph.D. Students

Sheng Ma   9/2010 – 9/2012
    Current Position: Assistant Professor
    National University of Defense Technology, China

M.Eng. Students Supervised

Remi Dufour   1/2013 – 9/2013
    Topic: Multi-core Prefetching Algorithms
    Current Position: Apple

Xiaoyin Liu   1/2012 – 6/2012
    Topic: Simulation Visualization for Networks-on-Chip

John Matienzo   1/2012 – 10/2012
    Topic: Optimized Broadcast Algorithms for the Intel SCC
    Current Position: Apple

MENTORING AND OUTREACH

Co-Organizer: Women in Computer Architecture Group (WICArch), 2011-Present
International membership consisting of professors, industry researchers and students in the field of computer architecture.

Organize annual networking events at major computer architecture conferences (ISCA and MICRO)

ECE Representative: Girls Leadership in Engineering Experience (GLEE) Dinner for prospective undergraduate students, 2013.

Panelist: "Being an Engineering Professor" hosted by the University of Toronto Prospective Professor in Training Program, April 2013

Speaker: CRA-W Graduate Cohort, April 2013

Co-Organizer: CRA-W/CDC Computer Architecture Discipline Specific Mentoring Workshop, August 2012
    Co-Organizers: Hillery Hunter (IBM), Russ Joseph, (Northwestern), Li-Shiuan Peh (MIT), Kelly Shaw (University of Richmond)

Received funding support from CRA-W/CDC and ACM SIGARCH, ACM SIGMICRO, AMD, IBM, Intel, Microsoft, Google, Oracle Labs, and VMware

Panelist: "What if... You Thrived on the Tenure Track?"
Grace Hopper Celebration of Women in Computing, 2011
Organizer: Ioana Burcea, University of Toronto

High School Outreach
Lester B. Pearson Collegiate Institute: Presentation on ECE to Grade 10 Computer Science class, April 2012
Bishop Strachan School: Presentation on ECE to Grade 11 Physics class, March 2012.
Bishop Strachan School: Presentation on ECE to Grade 11 Physics class, January 2011.

CRA-W/CDC Distinguished Lecture Series Organizer for University of Toronto, 2010
Speakers: Margaret Martonosi (Princeton) and Jaime Moreno (IBM)

Panelist: "Campus visit, interview and more"
Positioning Yourself for a Career in Academia. Hosted by the Status of Women Office at the University of Toronto, April 2010.

PROFESSIONAL SERVICE

Program Chair
20th International Symposium on High Performance Computer Architecture (HPCA), 2014

Program Co-Chair
7th ACM/IEEE International Symposium on Networks-on-Chip, 2013

Steering Committee Member, 2013–Present
International Symposium on Networks-on-Chip

Associate Editor, ACM Transactions on Architecture and Code Optimization, 2013-Present

Track Co-Chair
International Conference on Computer Design, Computer Systems and Applications Track, 2013
Canadian Conference on Electrical and Computer Engineering, Computer, Software and Applications Track, 2011

Workshop/Tutorials Chair
International Conference on Parallel Architecture and Compilation Techniques, 2013
International Symposium on Performance Analysis of Systems and Software, 2013

Publicity Chair
International Symposium on Computer Architecture (ISCA), 2014
International Symposium on Code Generation and Optimization (CGO), 2010

Instructor, 8th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, 2012
4-day course: Networks-on-Chip: Communication challenges for many-core architectures

Guest Co-Editor (with Mikko Lipasti, University of Wisconsin-Madison)
IEEE MICRO Special Issue on Systems for Very Large Scale Computing, May/June 2011

Workshop Co-Organizer
10th Annual Workshop on Duplicating, Deconstructing and Debunking (held with ISCA-39)

9th Annual Workshop on Duplicating, Deconstructing and Debunking (held with ISCA-38)

8th Annual Workshop on Duplicating, Deconstructing and Debunking (held with ISCA-36)

Session Chair

International Symposium on Computer Architecture (ISCA), June 2013

International Symposium on High Performance Computer Architecture (HPCA), February 2012

External Reviewer

NSERC Discovery Grants, Electrical and Computer Engineering Committee: 2011, 2012, 2013

Panelist

National Science Foundation (US), Computing and Communication Foundations (CCF) Grant Review Panel, 2012

National Science Foundation (US), Joint Computing and Communication Foundations (CCF)/ Computer and Network Systems (CNS) Grant Review Panel, 2011

Program Committee (Conferences)

Intl. Conference for High Performance Computing, Networking, Storage and Analysis (SC)	2014
Intl. Conference on Parallel Architectures and Compilation Techniques (PACT)	2010, 2014
Intl. Conference on Supercomputing (ICS)	2011, 2014
Intl. Symposium on Computer Architecture (ISCA)	2013
Intl. Symposium on High Performance Computer Architecture (HPCA)	2012, 2013
IEEE Micro Top Picks	2013
Intl. Conference on Parallel Processing (ICPP)	2010, 2013
Intl. Parallel and Distributed Processing Symposium (IPDPS)	2011, 2012, 2013
Intl. Conference on Computer Design (ICCD)	2009, 2010, 2011, 2012
Intl. Symposium on Performance Analysis of Software and Systems (ISPASS)	2011, 2012
Intl. Symposium on Microarchitecture (MICRO)	2011
Intl. Conference on Computer Aided Design (ICCAD)	2009, 2010
Intl. Conference on Design Automation and Test in Europe (DATE)	2010

Program Committee (Workshops)

General Purpose Processing Using GPUs (at ASPLOS)	2013
Interconnection Network Architectures: On-Chip, Multi-Chip (at HiPEAC)	2011, 2012, 2013
Communication Architecture for Scalable Systems (CASS) (at IPDPS)	2011, 2012, 2013
Network on Chip Architectures (at MICRO)	2009, 2010, 2011, 2012, 2013
Chip Multiprocessor Memory Systems and Interconnects (at HPCA)	2010
Chip Multiprocessor Memory Systems and Interconnects (at ISCA)	2009

External Review Committee

Intl. Conf. on High-Performance and Embedded Architectures and Compilers (HiPEAC), 2013

International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2013

Intl. Conf. on High-Performance and Embedded Architectures and Compilers (HiPEAC), 2012

International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2010

Reviewer for Conference and Journals

Journals: IEEE Micro, ACM Transactions on Computers, IEEE Transactions on Computers, IEEE Transactions in VLSI, IEEE Computer Architecture Letters, ACM Transactions on Embed-

ded Computing Systems, ACM Transactions on Architecture and Code Optimization, Journal of Parallel and Distributed Computing, IEEE Journal of Emerging and Selected Topics in Circuits and Systems, Transactions on Computer Aided Design, ACM Computing Surveys, ACM Transactions on Design Automation of Electronic Systems, IEEE Systems Journal, Canadian Journal of Electrical and Computer Engineering, Journal of Optical Communications and Networking, IEEE Transactions on Parallel and Distributed Computing

Conferences: International Symposium on Microarchitecture, International Symposium on Computer Architecture, International Conference on Architectural Support for Programming Languages and Operating Systems, International Conference on Parallel Architectures and Compilation Techniques, International Conference on Supercomputing, International Symposium on Parallel Algorithms and Architectures, International Conference on Parallel Processing, International Conference on Computer Design, International Conference on Computer Aided Design, International Symposium on High Performance Computer Architecture, International Symposium on Performance Analysis of Systems and Software, International Symposium on Circuits and Systems, Grace Hopper Celebration

Professional Memberships
IEEE, IEEE Computer Society
Senior Member
ACM, SIGARCH, SIGMICRO
Licensed Professional Engineer (P.Eng.) in Ontario

UNIVERSITY SERVICE

Member
Advisory Committee on the Appointment of ECE Chair, 2013

Vice-Chair
Community Affairs and Gender Issues Committee, Faculty of Applied Science and Engineering, 2010-2011, 2012-2013, 2013-2014 (acting chair)

Member
Community Affairs and Gender Issues Committee, Faculty of Applied Science and Engineering, 2010-2014