The Transmogrifier-4: An FPGA-Based Hardware Development System with Multi-Gigabyte Memory Capacity And High Host and Memory Bandwidth

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Abstract

This paper presents the design and implementation of a new FPGA-based development system that was created with the goal of providing as much inter-FPGA bandwidth, host-to-FPGA bandwidth, memory capacity and memory bandwidth as feasible. The system meets these goals by providing 4 Altera Stratix FPGAs, 8GB of external memory, and a 64bit/66MHz PCI bus host-to-FPGA link.

1. Introduction

An FPGA-based rapid development system is a set of hardware and software components that enable hardware engineers to design and implement high speed digital systems both quickly and cheaply.

This paper presents the Transmogrifier-4 development system (TM-4 for short).

The set of design requirements was selected based on knowledge gained from previous development platforms [1] [2] [3] as well as application case studies. A more detailed version of this topic can be found at [4] and [5].

The following two sections describe the design of the TM-4, and present system performance results.

2. The TM-4 Design

This section presents a brief overview of the design of the TM-4.

The TM-4 consists of two major subsystems: the FPGA development subsystem, and the interface subsystem. The development subsystem contains the portion of the TM-4 that is directly usable by designers in implementing their designs, including the development FPGAs, external memories, and video peripherals. The interface subsystem provides support functionality, including control of the TM-4 and a communication channel from the host computer to the development subsystem. These components are shown in Figure 1.

The development subsystem is composed of four Altera Stratix S80 chips that provide a total usable development area of 316,160 logic elements, 29.6Mb of on-chip SRAM, and 704 embedded 9x9 multipliers. The four FPGAs are interconnected using a fully interconnected point-to-point interconnection topology. The interconnections between each pair of FPGAs consist of both differential and singled ended signals. These signals provide between 56Gb/s and 66.5Gb/s of bandwidth between each pair of FPGAs.

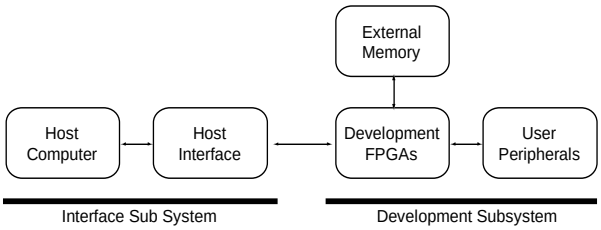

Figure 1: Top Level System Diagram

Each of the four FPGAs is connected to two independent DDR SDRAM modules. Each of these RAM slots can be populated with between 512MB and 2GB of RAM running at up to 166MHz. The standard configuration contains 8 1GB modules and provides a total peak bandwidth of 17.8GB/s.

Two of the FPGAs are connected to video peripherals. There are two NTSC analog video-in channels, one VGA video-out channel and two independent IEEE-1394 buses.

The interface subsystem provides a communication channel between the host computer and the development FPGAs. A custom designed FPGA core is used as a bridge between the host computer's 64bit 66MHz PCI bus and a custom-designed bus that connects to the development FPGAs. Communication across this link is provided through the use of a software API, on the host computer, and a hardware bus interface soft IP core, for the development FPGAs.

The TM-4 PCB, shown in Figure 2, is designed to have a high-performance single board computer plug into it. In the prototype system the host computer is a Pentium III Xeon computer running Linux. Both the single board computer and the TM-4 PCB fit into a standard PC case. This allows the TM-4 to be a completely self-contained development platform.

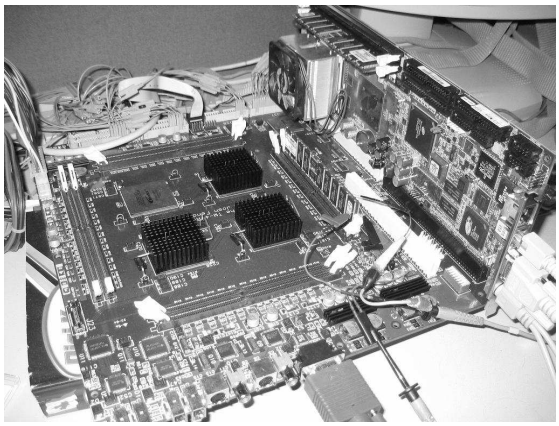

Figure 2: The Transmogrifier-4 PCB

Figure 3: A Video Delay Circuit

3. Performance Results

A prototype of the TM-4 was built and its performance was measured. The memory performance of the TM-4, under burst access conditions, was found to provide a sustained memory bandwidth of 17.6GB/s, while using all 8 memory modules.

The inter-FPGA bandwidth was measured by experimentally finding the maximum data rate that the inter-FPGA signal wires can support. The total measured aggregate bandwidth between FPGAs is either 577 or 1155MB/s, depending on which pair of FPGAs is considered. There are two numbers because not all pairs of FPGAs have the same number of interconnection wires.

The final goal of the TM-4 was to provide as much host-to-FPGA bandwidth as feasible. The measured write performance of the TM-4 was found to be 266MB/s, and the measured read performance was found to be 154MB/s. These performance numbers corresponds to a PCI bus utilization of 50% and 29% respectively.

4. Current Status

Although the TM-4 is a new system it does have a variety of functional applications, including both simple test applications, such as video in and out, and DDR SDRAM tests, and more complicated applications that have been ported from the TM-3, such as a real time edge detector and a procedural texture mapper. Figure 3 shows a test circuit that captures video data from an attached camera, stores it in DRAM, and allows it to be played back at various speeds on the VGA out.

Currently four additional TM-4s are being built for use by researchers at both the University of Toronto and McGill University. These researchers intend to implement new applications in both the areas of computational vision and bioinformatics, as well as other application domains.

5. Conclusions

This paper presented the design of an FPGA-based rapid prototyping system. The objective of this work was to provide a development platform with as much memory capacity, memory bandwidth, inter-FPGA bandwidth, and host-to-FPGA bandwidth as feasible. The resulting tests, on a prototype system, showed that the TM-4 was able to deliver large amounts of bandwidth in all of the categories.

It is the hope of the authors that the creation of this system will enable future researchers to implement designs not possible with previous technologies.

6. Acknowledgements

The authors would like to thank Altera, NSERC and Micronet, for providing funding and FPGAs to the TM-4 project, and Marcus van Ierssel for providing valuable technical support, as well as all those who participated in the specification and design reviews.

7. References

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