# 5 A Stochastic Model to Predict the Routability of Field-Programmable Gate Array Routing Architectures

## 5.1 Introduction

In this chapter, a study of FPGA routing architectures using a stochastic modelling approach is presented. The purpose of the model is twofold: to confirm the experimental results that were presented in Chapter 4, and to develop the foundations of a theory that facilitates further study of FPGA routing architectures, without the time-consuming demands of experimental work. In the stochastic model, circuits are represented by parameters that specify the total number of connections to be routed and the length of each connection. The model probabilistically 'routes' a circuit in an FPGA that has a certain size and a given routing architecture. Using probability theory, the model predicts the effect of a routing architecture's flexibility on its routability. Flexibility and routability were defined in Section 4.1. It is shown that the theoretical results are comparable to the corresponding experimental results from Chapter 4.

FPGAs are characterized in the stochastic model using the same basic assumptions that appear in Chapters 3 and 4. For ease of reference, some information discussed in those chapters is repeated here. An example FPGA is illustrated in Figure 5.1, which shows a square array of logic cells, with $N$ cells per side. Note that the grid coordinates in Figure 5.1 number only the logic cells, which differs from figures shown in earlier chapters. This change has been made because this labelling scheme is more convenient for the stochastic model. No assumptions are necessary about the internal details of the logic cells, except that each cell has some number of pins that are connected to the routing channels by routing switches. Routing switches are contained within C blocks and S blocks. It is assumed that tracks are hard-wired straight through the C blocks, without passing through routing switches, but that a routing switch is always involved to pass through an S block. This means that all tracks are composed of wiring segments that span the length of one logic cell. The switches in the C blocks are used to connect the logic cell pins to the wiring segments, and the S block switches provide connections from one wiring segment to another. The flexibility of a C block is defined by $F_c$, which specifies the number of tracks that each logic cell pin can connect to. The flexibility of an S block is given by $F_s$, which defines the number of other wiring segments that a wiring segment entering an S block can be connected to.

The routing of FPGAs is modelled assuming that a two-stage routing approach of global routing followed by detailed routing is used (see Section 2.2.2). The global routing stage is represented in the model by making assumptions, which are described in the next section, concerning the solution that a global router would produce. Assuming that a connection is assigned a single global route, the stochastic model uses probability

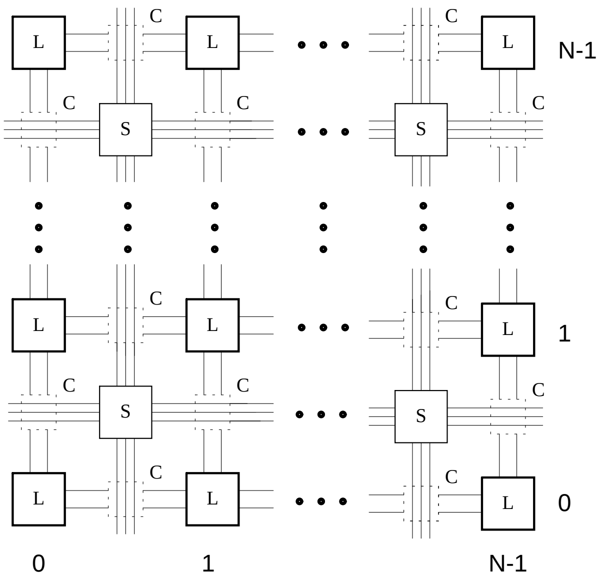


**Figure 5.1 -** *An $N \times N$ FPGA*

theory to represent the detailed routing of an FPGA as a random process. The probability of successfully performing the detailed routing of each connection is calculated and used to predict the routability of the FPGA.

This chapter is organized as follows. Section 5.2 provides an overview of the stochastic model, Section 5.3 describes previous research that is used to predict channel densities, Section 5.4 derives analytic expressions for calculating the probability that a connection can be successfully routed, the theoretical predictions of routability are given in Section 5.5, and Section 5.6 provides concluding remarks.

## 5.2 Overview of the Stochastic Model

In the stochastic model, it is assumed that a circuit with a total of $C_T$ two-point connections is to be routed in an FPGA with $N \times N$ logic cells. The length of each connection is drawn from a probability distribution, $P_L$. It will later be necessary to choose a specific distribution for $P_L$. In Section 5.4.4, it is assumed that $P_L$ is geometric, with mean length $\bar{R}$. This assumption is taken from earlier work on the stochastic modelling of two-dimensional arrays of connected cells [Heller84] [ElGa81], and has the following physical interpretation in an FPGA: at each C block along the path of a connection, the connection will terminate (at a logic cell) with probability $\frac{1}{\bar{R}}$ and will continue (to the next C block) with probability $1 - \frac{1}{\bar{R}}$.

The $C_T$ connections are individually referred to as $C_1, C_2, ..., C_{C_T}$ and the statistical event that each connection is successfully routed is called $R_{C_1}, R_{C_2}, ..., R_{C_{C_T}}$. The key to the stochastic model is the calculation of the probabilities of $R_{C_1}, R_{C_2}, ..., R_{C_{C_T}}$. Recall that routability is defined as the percentage of the connections in a circuit that can be successfully routed. In terms of $R_{C_1}, R_{C_2}, \ldots, R_{C_{C_T}}$ this corresponds to the ratio of the expected number of successfully routed connections to the total number of connections, $C_T$. Thus, routability is the average probability of completing a connection and can be calculated in the stochastic model according to

$$Routability = \frac{1}{C_T} \sum_{i=1}^{C_T} P(R_{C_i}),$$

where $P(R_{C_i})$ is the probability of successfully routing $C_i$.

### 5.2.1 Model of Global Routing and Detailed Routing

In order to use a key research result by El Gamal [ElGa81] to predict the densities of the routing channels in an FPGA, the following assumption is made concerning the way in which a global routing algorithm would assign the connections in a circuit to the routing channels. It is assumed that each connection is assigned a single path through the routing channels in such a way that the number of connections per routing channel is Poisson distributed. Section 5.3 justifies this assumption and illustrates its use.

In the stochastic model, the detailed routing of an FPGA is represented as a random process. Based on the assumption that a connection is assigned a single path through the routing channels, the probability of successfully performing the detailed routing of the connection is calculated using combinatorial analysis. The probability expressions account for the number of tracks per routing channel, the flexibilities of the C and S blocks, and the side-effects that the routing of one connection has on others.

Recall, from earlier discussions in this dissertation, that a key issue in the detailed routing of FPGAs is how the routing of one connection may affect other connections. To compute the value of each $P(R_{C_i})$, it is necessary for the stochastic model to account for these effects. To accomplish this, the model 'routes' the connections in a serial manner and predicts the effect that each successfully routed connection has on the densities of the routing channels. By this mechanism, the probability of routing each subsequent connection is influenced because there are more connections in a channel to compete with. The next section shows how El Gamal's results can be used to calculate channel densities and following this, the probability formulas for $P(R_{C_i})$ are derived.

## 5.3 Previous Research for Predicting Channel Densities

In [ElGa81], a stochastic model is developed to predict the wiring requirements of Master Slice Integrated Circuits that have a two-dimensional array of identical cells, with horizontal and vertical routing channels between the rows and columns of cells. The model divides the channels into segments that span the length or width of one cell and it is assumed that all interconnections start at one cell and travel a minimum distance through the channel segments to another cell. It is further assumed that the number of connections per cell can be drawn independently from a Poisson distribution, with parameter $\lambda$, where $\lambda$ is defined as the ratio of the total number of connections in a circuit to the total number of cells in the array. The average connection length, in number of cells traversed, is called $\bar{R}$. The paper also makes assumptions about the trajectories of connections, but these assumptions are not necessary for the results that are quoted here.

[ElGa81] shows that under the above assumptions, in an array that has $N \times N$ routing channels, the densities of the channel segments will be Poisson distributed, with the average density given by $\frac{\lambda \bar{R}}{2}$. This result holds as long as $\bar{R} < \infty$, independent of $N$, and provides a convenient method of predicting channel densities.

### 5.3.1 Predicting Channel Densities in FPGAs

Although the results in [ElGa81] were developed for Master Slice circuits, they can also be applied to the FPGAs considered here, since both types of devices are based on a two-dimensional array of identical cells. The definitions of the routing channels differ, but these differences can be ignored since the tracks consist of short segments that span only one logic cell in both cases.

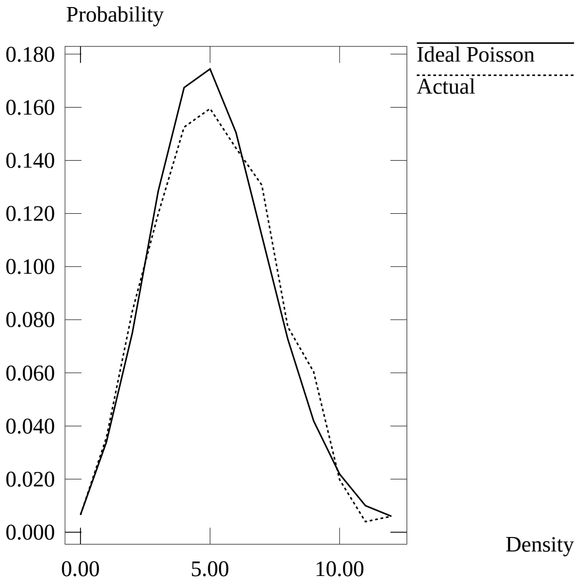


**Figure 5.2 -** *Predicted versus Actual Channel Densities*

Having made these assumptions, it is convenient to predict channel densities in FPGAs using El Gamal's result. The accuracy of the predictions can be checked by comparing the ideal Poisson distribution with mean $\frac{\lambda \bar{R}}{2}$ to the distribution of channel densities in real FPGA circuits. Such comparisons were conducted for the example circuits from Chapter 4. A typical result is shown in Figure 5.2, which gives one curve for the ideal Poisson distribution and another curve for the measured distribution of channel densities. As the figure shows, the actual channel densities are surprisingly close to the Poisson predictions.

It is interesting to discuss a physical interpretation of the Poisson distribution in this context. Assume that an FPGA has $W$ tracks in each routing channel and consider a specific channel segment. For each of the $W$ tracks, define $p_i$ as the probability of the statistical event that the track would be occupied if a circuit were routed in the FPGA. If $W = 1$, there will be a probability, $p_1$, that the track will be occupied by some connection. If $W = 2$, then there will be a probability, $p_2$, that each of the two tracks will be occupied by some connection and $p_2 < p_1$. Extending this to the general case, if $W = n$, then each track will be occupied with probability $p_n$, and $p_n < p_{n-1} < \cdots < p_2 < p_1$. Furthermore, as $n \rightarrow \infty$, $p_n \rightarrow 0$. Since $p_n$ is small in the limiting case, the event that a track is used is a rare event and the number of these events (density) can be approximated by the Poisson distribution.

In FPGAs in which the tracks consist of segments that span multiple logic cells, El Gamal's result is probably not an accurate approximation of channel densities. In such cases, a different method of calculating densities would be needed. For this reason, the probability expressions that are developed in the following section are derived in a general way that does not hinge upon any particular distribution for the channel densities. However, assuming a Poisson distribution for the channels does allow some expressions to be simplified, an example of which is given in Section 5.4.1.

## 5.4 Calculating the Probability of Successfully Routing a Connection

This section derives analytic expressions for calculating the probability of successfully performing the detailed routing of a single connection in an FPGA. As an example of a connection, consider Figure 5.3. The figure shows a connection, $C_i$, that starts at logic cell $(x_1, y_1)$ and travels through routing channels to logic cell $(x_2, y_2)$. The length of $C_i$ is defined in terms of logic cell hops (to be consistent with [ElGa81]), as

$LC_i = |x_1 - x_2| + |y_1 - y_2|$. Also, the number of S blocks that $C_i$ passes through is given by $LC_i - 1$. To define the probability, $P(R_{C_i})$, of successfully routing $C_i$, assume that $LC_i = n+1$. The statistical event that corresponds to this assumption is written $L_{n+1}$. Also define the following events:

- $X_1$ - the event that the logic cell pin associated with $C_i$ at $(x_1, y_1)$ can connect to at least one track at the first C block. Note that there are, by definition, $F_c$ tracks that can connect to the logic cell pin, but any number of them may already be used by other connections that have been previously 'routed'.
- $S_1, S_2, \cdots, S_n$ - the events that $C_i$ can successfully reach at least one track on the outgoing side of the first, second, up to the $n^{th}$ S block. There are $LC_i - 1$ such events for $C_i$.
- $X_2$ - the event that at least one of the tracks that are available to $C_i$ at the last C block can be connected to the appropriate logic cell pin at $(x_2, y_2)$.
- $R_{C_i}$ - the event that $C_i$ can be successfully routed.

Since $C_i$ is successfully routed only if all of the events $X_1, S_1, S_2, ..., S_n, X_2$ occur, then

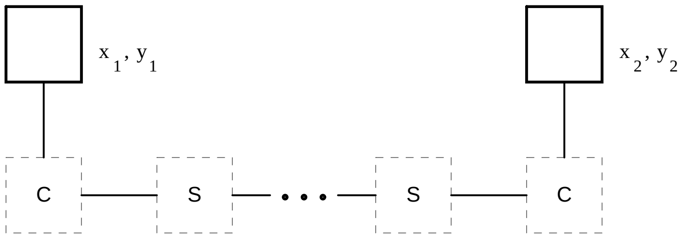


**Figure 5.3 -** *A Typical Connection*

$$R_{C_i} \mid L_{n+1} = X_1 \cap S_1 \cap S_2 \cdots \cap S_n \cap X_2$$

and the probability of successfully routing $C_i$ is given by

$$\begin{aligned} P(R_{C_i} \mid L_{n+1}) &= P(X_1 \cap S_1 \cap S_2 \cdots \cap S_n \cap X_2) \\ &= P(X_1)P(S_1 \mid X_1)P(S_2 \mid S_1 \cap X_1) \cdots P(S_n \mid S_{n-1} \cap \cdots \cap S_1 \cap X_1) \\ &\quad \cdot P(X_2 \mid S_n \cap \cdots S_1 \cap X_1)\,. \end{aligned} \qquad 5.1$$

Since the events $X_1, S_1, S_2, ..., S_n,$ and $X_2$ are not independent, it is necessary to find formulas for each of the terms in Equation 5.1. This is accomplished in the following sections by using combinatorial analysis that accounts for the flexibilities of the C and S blocks ($F_c$ and $F_s$), the number of tracks per routing channel ($W$), and the densities of the routing channels. As discussed in Section 5.3, channel density is approximated by the Poisson distribution with parameter $\lambda_g = \frac{\lambda \bar{R}}{2}$, where $\lambda$ is the number of connections per logic cell and $\bar{R}$ is the average connection length. Appropriate values for $\lambda$ and $\bar{R}$ are discussed in Section 5.5.

### 5.4.1 The Logic Cell to C Block Event

The event $X_1$ can be depicted pictorially as shown in Figure 5.4. The figure shows a routing channel with $W$ tracks and a logic cell pin that can connect to $F_c$ of the tracks, via routing switches (shown by an X). The figure also shows a set of $D$ tracks, drawn as dashed lines, that are already occupied by previously routed connections. In the figure, $W = 10$, $F_c = 5$, and $D = 5$. The event $X_1$ can then be viewed as a random process in which a logic cell pin can connect to any of the unused tracks where there are switches. To derive a formula for $P(X_1)$, it is convenient to define the event NONE as the oppo-

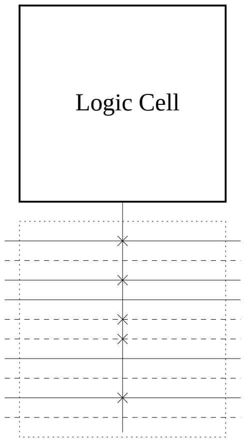


**Figure 5.4 -** *The Event* $X_1$

site of $X_1$ - i.e. $P(X_1) = 1 - P(NONE)$. The event *NONE* occurs when all $F_c$ tracks are within the set of *D* used tracks. As a first step to evaluating $P(NONE)$, assume that $D = d$ and define the corresponding event $D_d$. Assuming that the $F_c$ switches can appear on any of the *W* tracks, the probability of NONE conditional on $D_d$ is given by the ratio of the number of ways in which all of the $F_c$ switches can lie within the *d* occupied tracks to the number of ways in which the $F_c$ switches can appear on any of the *W* tracks. Using combinatorial analysis, this can be expressed as

$$P(NONE \mid D_d) = \frac{{}_dC_{F_c}}{{}_WC_{F_c}} , \qquad 5.2$$

where ${}_dC_{F_c}$ means the combinations of *d* things taken $F_c$ at a time. As a check, note that $P(NONE \mid D_d)$ is 0 if $d < F_c$ and 1 if $d = W$. Next, consider the events $D_0, D_1, ..., D_W$ corresponding to the possible values of *D*. Since the occurrence of NONE implies exactly one of $D_0, D_1, ..., D_W$, then

$$NONE = (NONE \cap D_0) \cup (NONE \cap D_1) \cup \cdots \cup (NONE \cap D_W)$$

and since $D_0, D_1, ..., D_W$ are mutually exclusive

$$P(NONE) = P(NONE \cap D_0) + P(NONE \cap D_1) + \cdots + P(NONE \cap D_W) .$$

Using the relation $P(X \cap Y) = P(X)P(Y \mid X)$,

$$P(NONE) = P(D_0)P(NONE \mid D_0) + P(D_1)P(NONE \mid D_1) + \cdots$$
$$+ P(D_W)P(NONE \mid D_W) .$$

The terms $P(D_d)$ are given by the Poisson distribution with parameter $\lambda_g$, written $p(\lambda_g, d)$, so that

$$P(NONE) = \sum_{d=0}^{W} p(\lambda_g, d) \cdot P(NONE \mid D_d)$$

and, substituting equation 5.2,

$$P(NONE) = \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{F_c}}{{}_WC_{F_c}} .$$

Finally,

$$P(X_1) = 1 - P(NONE) = 1 - \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{F_c}}{{}_WC_{F_c}} \qquad 5.3$$

Note that Equation 5.3 is an approximation because the Poisson distribution has an infinite tail, whereas the summation has an upper limit of $W$. This means that there is a non-zero probability of channel densities above $W$, but for practical values of $W$ this error is very small and can be ignored. This same statement also applies to other equations that appear later in this chapter.

Equation 5.3 has been developed in a way that does not depend upon the channel densities being Poisson distributed. This approach is taken because the channel densities in some FPGAs, such as those having tracks with segments that span multiple logic cells, may have distributions that are not Poisson. The stochastic model can still be used for such FPGAs, simply by replacing $p(\lambda_g, d)$ with an appropriate distribution. It is interesting to note, however, that the properties of the Poisson distribution allow expressions like Equation 5.3 to be simplified, as described below.

Equation 5.3 can be simplified by noting that a Poisson distribution is infinitely divisible. In the case of event $X_1$, this means that rather than considering a Poisson process over $W$ tracks, with mean $\lambda_g$, it is sufficient to deal with a smaller Poisson process over $F_c$ tracks, with mean $\lambda_g \frac{F_c}{W}$. $P(NONE)$ is then given by $p(\lambda_g \frac{F_c}{W}, F_c)$, and Equation 5.3 can be expressed as

$$P(X_1) = 1 - P(NONE) = 1 - p(\lambda_g \frac{F_c}{W}, F_c) .$$

Similar simplifications can be made for other expressions shown later in this section, but they are easily developed and so are not shown.

Equation 5.3 calculates $P(X_1)$ based on the relationship between the event $X_1$ and the event *NONE*. An alternative is to calculate $P(X_1)$ directly by defining $A_1^{X_1}, A_2^{X_1}, ..., A_{F_c}^{X_1}$ as the events that $X_1$ occurs with exactly 1, 2, ..., $F_c$ available tracks. Using this approach,

$$X_1 = A_1^{X_1} \cup A_2^{X_1} \cup \cdots \cup A_{F_c}^{X_1}$$

and since $A_1^{X_1}, A_2^{X_1}, ..., A_{F_c}^{X_1}$ are mutually exclusive,

$$P(X_1) = P(A_1^{X_1}) + P(A_2^{X_1}) + \cdots + P(A_{F_c}^{X_1}) .$$

Although $P(X_1)$ can be calculated using Equation 5.3, each of $P(A_a^{X_1})$ will be required in the next section, so they are derived here. Consider the general case of $X_1$ occurring with exactly $(a)$ available tracks, and the corresponding event $A_a^{X_1}$. Assuming a specific number of occupied tracks, $D = d$, the conditional probability $P(A_a^{X_1} \mid D_d)$ can be expressed using combinatorial analysis as

$$P(A_a^{X_1} \mid D_d) = \frac{{}_dC_{(F_c - a)} \cdot {}_{(W-d)}C_a}{{}_WC_{(F_c - a)} \cdot {}_{(W-(F_c - a))}C_a} \cdot {}_{F_c}C_a \,.$$

In words, this is the number of ways that a set of $(F_c - a)$ tracks can be within $(d)$ used tracks times the number of ways of choosing a set of $(a)$ tracks from $(F_c)$ tracks, all divided by the number of ways that two distinguishable sets of $(a)$ and $(F_c - a)$ tracks can be within $W$ tracks. Since the occurrence of $A_a^{X_1}$ implies exactly one of $D_0, D_1, ..., D_W$, following the steps shown for equation 5.3,

$$\begin{aligned} P(A_a^{X_1}) &= \sum_{d=0}^{W} p(\lambda_g, d) \cdot P(A_a^{X_1} \mid D_d) \\ &= \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(F_c - a)} \cdot {}_{(W-d)}C_a}{{}_WC_{(F_c - a)} \cdot {}_{(W-(F_c - a))}C_a} \cdot {}_{F_c}C_a \end{aligned} \qquad 5.4$$

As a check, it is easily verified that $P(NONE)$ can be obtained using equation 5.4 by setting $a = 0$, which must be true since $P(NONE) \equiv P(A_0^{X_1})$. Finally,

$$\begin{aligned} P(X_1) &= \sum_{a=1}^{F_c} P(A_a^{X_1}) \\ &= \sum_{a=1}^{F_c} \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(F_c - a)} \cdot {}_{(W-d)}C_a}{{}_WC_{(F_c - a)} \cdot {}_{(W-(F_c - a))}C_a} \cdot {}_{F_c}C_a \,. \end{aligned}$$

### 5.4.2 The S Block Events

All of the events that are associated with S blocks can be treated in a uniform way. This section first derives probability formulas for $S_1 \mid X_1$ and then shows how the resulting expressions can be applied to subsequent S blocks.

#### 5.4.2.1 The First S Block Event, for $\mathbf{F_s = 3}$

Since $P(S_1 \mid X_1)$ will be affected by the flexibility of the S block, it is convenient to assume a specific value of $F_s$. In the following derivation, the case $F_s = 3$ is assumed.

This is the easiest case to handle because it means that each wiring segment that enters an S block can connect to exactly one wiring segment on each other side. Also, the derivation need not be concerned with whether a connection turns or passes straight through an S block since the effect is the same in both cases.

The event $S_1 \mid X_1$ is depicted in Figure 5.5, which shows an S block and a routing channel that has $W$ tracks. The figure shows a set of $A^{X_1}$ tracks, drawn as bold lines, that are available at the incoming side of the S block and a set of $D$ tracks, drawn as dashed lines on the outgoing side of the S block, that are already used by other connections. In the figure, $D = 4$, $W = 10$, and $A^{X_1} = 3$. Note that setting $A^{X_1}$ to three corresponds to the event $A_3^{X_1}$, from Section 5.4.1. Figure 5.5 uses dotted lines to indicate S block switches and shows that each track on the incoming side of the S block can be connected to one other track on the outgoing side. The event can then be considered to be a random process in which each of the $A^{X_1}$ incoming tracks can connect to one track on the outgoing side of the S block, as long as that outgoing track is not among the $D$ used tracks. In other words, given that there are $A^{X_1}$ tracks that are available on the incoming side of the S block, it is necessary to find the probability that one or more of these tracks are also available on the outgoing side.

The event $S_1 \mid X_1$ can occur with one or more available outgoing tracks. To calculate $P(S_1 \mid X_1)$, define $A_1^{S_1}, ..., A_{F_c}^{S_1}$ as the events that $S_1 \mid X_1$ occurs with exactly 1, 2, ..., $F_c$ available tracks on the outgoing side. Since

$$S_1 \mid X_1 = A_1^{S_1} \cup \cdots \cup A_{F_c}^{S_1}$$

and $A_1^{S_1}, ..., A_{F_c}^{S_1}$ are mutually exclusive

$$P(S_1 \mid X_1) = P(A_1^{S_1}) + \cdots + P(A_{F_c}^{S_1}) \,. \qquad 5.5$$

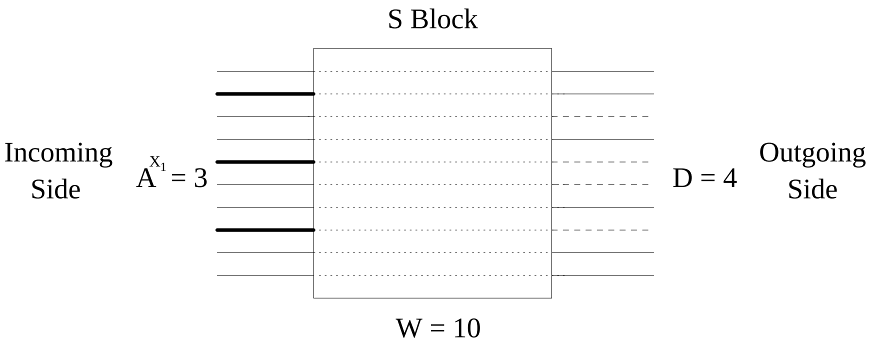


**Figure 5.5 -** *The Event* $S_1$

Solving for each term in this summation requires several steps. Consider the general case where $S_1 \mid X_1$ occurs with exactly $k$ available outgoing tracks. The corresponding event is written $A_k^{S_1}$. The probability of $A_k^{S_1}$ will depend on the number of tracks available on the incoming side, given by $A^{X_1}$, and on the value of $D$. Assume a specific value of $A^{X_1} = a$. Since $X_1$ is known to have occurred, this corresponds to assuming that $X_1$ occurred with exactly $(a)$ available tracks. The appropriate statistical event for this assumption is then written as $A_a^{X_1} \mid X_1$. Also, assume that $D = d$ and define the event $D_d$. A conditional probability for $A_k^{S_1}$ can then be expressed using combinatorial analysis as

$$P((A_k^{S_1} \mid (A_a^{X_1} \mid X_1)) \mid D_d) = \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{W-(a-k)}C_k} \cdot {}_aC_k \,. \qquad 5.6$$

Equation 5.6 expresses the ratio of the number of ways in which exactly $(k)$ of the $(a)$ available incoming tracks can end up on unoccupied tracks on the outgoing side to the number of ways in which $(k)$ and $(a-k)$ tracks can appear on any of the $W$ tracks. To expand Equation 5.6, following the steps outlined in the previous section, consider the events $D_0, D_1, ..., D_W$ corresponding to the possible values of $D$. Since the occurrence of $(A_k^{S_1} \mid (A_a^{X_1} \mid X_1))$ implies exactly one of $D_0, D_1, ..., D_W$, then

$$P(A_k^{S_1} \mid (A_a^{X_1} \mid X_1)) = \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{W-(a-k)}C_k} \cdot {}_aC_k .$$

Next, consider the events $(A_1^{X_1} \mid X_1), ..., (A_{F_c}^{X_1} \mid X_1)$ corresponding to the possible values of $A^{X_1}$. The occurrence of $A_k^{S_1}$ implies exactly one of $(A_1^{X_1} \mid X_1), ..., (A_{F_c}^{X_1} \mid X_1)$, so that

$$P(A_k^{S_1}) = \sum_{a=1}^{F_c} P(A_a^{X_1} \mid X_1) \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{W-(a-k)}C_k} \cdot {}_aC_k . \qquad 5.7$$

As stated above, the terms $P(A_a^{X_1} \mid X_1)$ express the probability that, given the occurrence of event $X_1$, $X_1$ occurred with exactly $(a)$ available tracks. Each of $P(A_a^{X_1} \mid X_1)$ is defined by Bayes' rule [Fell52], according to

$$P(A_a^{X_1} \mid X_1) = \frac{P(A_a^{X_1})}{\sum_{j=1}^{F_c} P(A_j^{X_1})}, \qquad 5.8$$

where $P(A_1^{X_1}), ..., P(A_{F_c}^{X_1})$ are given by Equation 5.4. Substituting 5.7 and 5.8 into 5.5,

$$\begin{aligned} P(S_1 \mid X_1) &= \sum_{k=1}^{F_c} P(A_k^{S_1}) \\ &= \sum_{k=1}^{F_c} \sum_{a=1}^{F_c} \frac{P(A_a^{X_1})}{\left( \sum_{j=1}^{F_c} P(A_j^{X_1}) \right)} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{W-(a-k)}C_k} \cdot {}_aC_k . \end{aligned} \qquad 5.9$$

### 5.4.2.2 The First S Block Event, for Any Value of $F_s$

Equation 5.9 assumes a specific value of S block flexibility, $F_s = 3$. This section shows how Equation 5.9 can be generalized for other values of $F_s$. In Equation 5.6, a one-to-one correspondence was assumed between the subscript $(a)$ in $A_a^{X_1} \mid X_1$, on the left hand side of the equation, and the variable $(a)$, on the right hand side. This relation holds for $F_s = 3$ but does not necessarily apply for other values of $F_s$. For example, if

$F_s = 6$, a more appropriate variable for the right hand side of the equation is $2a$. In general, the subscript $(a)$ should be scaled by some factor, $\alpha$, and Equation 5.6 becomes

$$P((A_k^{S_1} \mid (A_a^{X_1} \mid X_1)) \mid D_d) = \frac{{}_dC_{(\alpha a - k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha a - k)} \cdot {}_{W-(\alpha a - k)}C_k} \cdot {}_{\alpha a}C_k \,. \qquad 5.10$$

Clearly, $\alpha$ depends on the value of $F_s$, but $\alpha$ may also depend on whether a connection passes straight through a particular S block, or turns. Define $Z_1$ as the event that a connection passes straight through an S block, and $Z_2$ as the event that it turns. Also, define $\alpha_1$ and $\alpha_2$ as the values of $\alpha$ corresponding to $Z_1$ and $Z_2$. Since $S_1 \mid X_1$ implies one of $Z_1$ and $Z_2$, then

$$P(S_1 \mid X_1) = P(Z_1) \cdot P((S_1 \mid X_1) \mid Z_1) + P(Z_2) \cdot P((S_1 \mid X_1) \mid Z_2)$$

and using Equation 5.9 and 5.10,

$$P(S_1 \mid X_1) =$$

$$P(Z_1) \cdot \sum_{k=1}^{W} \sum_{a=1}^{F_c} \frac{P(A_a^{X_1})}{\left( \sum_{j=1}^{F_c} P(A_j^{X_1}) \right)} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_1 a - k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_1 a - k)} \cdot {}_{W-(\alpha_1 a - k)}C_k} \cdot {}_{\alpha_1 a}C_k +$$

$$P(Z_2) \cdot \sum_{k=1}^{W} \sum_{a=1}^{F_c} \frac{P(A_a^{X_1})}{\left( \sum_{j=1}^{F_c} P(A_j^{X_1}) \right)} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_2 a - k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_2 a - k)} \cdot {}_{W-(\alpha_2 a - k)}C_k} \cdot {}_{\alpha_2 a}C_k \qquad 5.11$$

Appropriate values for $P(Z_1)$ (note that $P(Z_2) = 1 - P(Z_1)$), $\alpha_1$, and $\alpha_2$ are discussed in Section 5.5. Note that the $(k)$ summation in Equation 5.11 has an upper limit of $W$, whereas the corresponding upper limit in Equation 5.9 is $F_c$. This change is required since it may be possible to connect to all $W$ tracks in a channel for values of $F_s$ that are greater than three.

#### 5.4.2.3 The Remaining S Block Events

Thus far, this section has dealt specifically with the event $S_1 \mid X_1$, but the derived expressions are applicable to any of the other S block events, with two changes. First, for the $m^{th}$ S block event, $(S_m \mid S_{m-1} \cap \cdots \cap S_1 \cap X_1)$, all summations must reach an upper limit of *W*. Second, the probabilities $P(A_1^{X_1})$, ..., $P(A_{F_c}^{X_1})$ in Equation 5.11 are replaced by $P(A_1^{S_{m-1}})$, ..., $P(A_W^{S_{m-1}})$, which are defined by Equation 5.12, with $m = m-1$. Applying these changes, Equation 5.7 becomes

$$P(A_k^{S_m}) = \sum_{a=1}^{W} P(A_a^{S_{m-1}} \mid S_{m-1} \cap \cdots \cap S_1 \cap X_1) \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{W-(a-k)}C_k} \cdot {}_aC_k \qquad 5.12$$

and Equation 5.11 becomes

$$P(S_m \mid S_{m-1} \cap \cdots \cap S_1 \cap X_1) =$$

$$P(Z_1) \cdot \sum_{k=1}^{W} \sum_{a=1}^{W} \frac{P(A_a^{S_{m-1}})}{\left(\sum_{j=1}^{W} P(A_j^{S_{m-1}})\right)} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_1 a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_1 a-k)} \cdot {}_{W-(\alpha_1 a-k)}C_k} \cdot {}_{\alpha_1 a}C_k +$$

$$P(Z_2) \cdot \sum_{k=1}^{W} \sum_{a=1}^{W} \frac{P(A_a^{S_{m-1}})}{\left(\sum_{j=1}^{W} P(A_j^{S_{m-1}})\right)} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_2 a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_2 a-k)} \cdot {}_{W-(\alpha_2 a-k)}C_k} \cdot {}_{\alpha_2 a}C_k \qquad 5.13$$

### 5.4.3 The C Block to Logic Cell Event

The event $X_2$ is depicted by Figure 5.6, which shows a set of $A^{S_n} = 4$ tracks, drawn as bold lines, that are available at a C block (this corresponds to the event $A_4^{S_n}$ in Section 5.4.2) and a set of $F_c = 5$ tracks that connect to the appropriate logic cell pin for the connection. The event $X_2$ can then be viewed as a random process in which the logic cell pin can be connected to any of the set of $(A^{S_n})$ tracks where there are switches. Stated differently, given that one or more tracks were available at the outgoing side of the last S block, it is necessary to determine the probability that one or more of these tracks con-

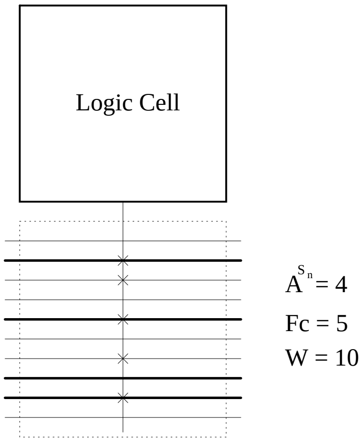


**Figure 5.6 -** *The Event* $X_2$

nects to the appropriate logic cell pin. To simplify the notation, the expression $S_n \cap \cdots S_1 \cap X_1$ will be substituted for by *SX*. To calculate the probability of $X_2 \mid SX$, define the opposite event $NONE \mid SX$, where $P(X_2 \mid SX) = 1 - P(NONE \mid SX)$. To find $P(NONE \mid SX)$, assume a specific value of $A^{S_n} = a$ and define the corresponding event $A_a^{S_n}$. A conditional probability for $NONE \mid SX$ can then be defined by

$$P((NONE \mid SX) \mid A_a^{S_n}) = \frac{{}_{(W-F_c)}C_a}{{}_W C_a} . \qquad 5.14$$

Equation 5.14 assumes that each of the $F_c$ switches for the the logic cell pin associated with event $X_2$ is equally likely to be on any of the *W* tracks. This may not be realistic since a good C block topology would ensure that the tracks that are connectable to one pin would overlap the tracks connectable to others, as was discussed in Section 4.2.2.1. This assumption will have the effect of producing low predictions of routability for low values of $F_c$, which is discussed further in Section 5.5.

Consider the events $A_1^{S_n}, A_2^{S_n}, \ldots, A_W^{S_n}$ corresponding to the possible values of $A^{S_n}$. Since the occurrence of $NONE \mid SX$ implies exactly one of $A_1^{S_n}, A_2^{S_n}, \ldots, A_W^{S_n}$, it follows that

$$P(NONE \mid SX) = \sum_{a=1}^{W} P(A_a^{S_n} \mid SX) \cdot P((NONE \mid SX) \mid A_a^{S_n}),$$

where each of $P(A_a^{S_n} \mid SX)$ is given by Bayes' rule, so that

$$P(X_2 \mid SX) = 1 - P(NONE \mid SX) = 1 - \sum_{a=1}^{W} \frac{P(A_a^{S_n})}{\left(\sum_{j=1}^{W} P(A_j^{S_n})\right)} \cdot \frac{{}_{(W-F_c)}C_a}{{}_{W}C_a} . \qquad 5.15$$

Each of $P(A_1^{S_n}), ..., P(A_W^{S_n})$ can be calculated using Equation 5.12, with $m = n$. Note that for the case of a connection that has length one, there are no S block events, so that $A_a^{S_n}$ in Equation 5.15 are replaced by $A_a^{X_1}$. Each of $P(A_1^{X_1}), ..., P(A_{F_c}^{X_1})$ can be calculated using Equation 5.4.

### 5.4.4 The Probability of $R_{C_i}$

Equation 5.1 can now be solved using the formulas developed in this section to calculate $P(R_{C_i})$, for the given value of $LC_i = n+1$. Equation 5.1 is reproduced below, as Equation 5.16.

$$\begin{aligned} P(R_{C_i} \mid L_{n+1}) &= P(X_1 \cap S_1 \cap S_2 \cdots \cap S_n \cap X_2) \\ &= P(X_1) P(S_1 \mid X_1) P(S_2 \mid S_1 \cap X_1) \cdots P(S_n \mid S_{n-1} \cap \cdots \cap S_1 \cap X_1) \\ &\quad \cdot P(X_2 \mid S_n \cap \cdots S_1 \cap X_1) . \end{aligned} \qquad 5.16$$

To make use of this result to calculate $P(R_{C_i})$, define $LC_i = l_{\max}$ as the maximum length of any connection and $L_{l_{\max}}$ as the corresponding event. Appropriate values for $l_{\max}$ are discussed in Section 5.5. Next, consider the events $L_1, ..., L_{l_{\max}}$ corresponding to the possible values of $LC_i$. Since the occurrence of $R_{C_i}$ implies exactly one of $L_1, ..., L_{l_{\max}}$, then

$$P(R_{C_i}) = \sum_{l=0}^{l_{\max}} P(L_l) \cdot P(R_{C_i} \mid L_l), \tag{5.17}$$

where $P(L_l)$ are given by the probability distribution of connection length, referred to in Section 5.2 as $P_L$, and each $P(R_{C_i} \mid L_l)$ is defined by Equation 5.16. As mentioned in Section 5.2, $P_L$ is assumed to be geometric, with mean $\bar{R}$. Thus, $P(L_l)$ is given by

$$P(L_l) = pq^{l-1},$$

where $p = \frac{1}{\bar{R}}$ and $q = 1 - p$. The following section shows how Equation 5.17 is evaluated to predict routability.

## 5.5 Using the Stochastic Model to Predict Routability

In order to make use of Equation 5.17, it is necessary to choose appropriate values for the various parameters that appear in the formulas developed in Section 5.4, as well as to evaluate the function $\lambda_g$, that is used to predict channel densities. This section first shows how $\lambda_g$ is calculated and then gives appropriate values for each of the parameters. Following this, the routability predictions that are produced by the stochastic model are presented, with comparisons to the experimental results that were shown in Chapter 4.

As stated in Section 5.3, the parameter $\lambda_g$ is defined by $\lambda_g = \frac{\lambda \bar{R}}{2}$, where $\bar{R}$ is the average connection length and $\lambda$ is the ratio of the expected number of routed connections to the total number of logic cells. Given this definition, $\lambda$ must be re-calculated after each connection is probabilistically ’routed’ by the stochastic process. Thus, after $i-1$ connections have been ’routed’, $\lambda$ can be calculated as

$$\lambda = \frac{1}{N^2} \sum_{c=1}^{i-1} P(R_{C_c}) . \tag{5.18}$$

It is necessary to assign values to the following parameters: $N$, $W$, $l_{max}$, $C_T$, $\bar{R}$, $P(Z_1)$, $\alpha_1$, $\alpha_2$, $F_s$, and $F_c$. The first three of these depend on the size of the FPGA array and the next three are determined by the characteristics of the circuit to be routed. Since the routability predictions that are generated in this chapter are to be compared with the results from Chapter 4, the parameters will be taken from the FPGA circuits that were used in that chapter. The corresponding values are given in Table 4.1.

| Circuit | $N$ | $W$ | $l_{max}$ | $C_T$ | $\bar{R}$ | $P(Z_1)$ |
|---|---|---|---|---|---|---|
| BUSC | 11 | 11 | 20 | 392 | 2.7 | .71 |
| DMA | 15 | 12 | 28 | 771 | 2.8 | .75 |
| BNRE | 20 | 14 | 38 | 1257 | 3.0 | .75 |
| DFSM | 21 | 13 | 40 | 1422 | 2.85 | .76 |
| Z03 | 25 | 13 | 48 | 2135 | 3.15 | .75 |

**Table 4.1 -** *Stochastic Model Parameters for Experimental Circuits*

| | $F_s$ | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | ... |
| $\alpha_1$ | 1.0 | 1.0 | 2.0 | 2.0 | 2.0 | 3.0 | 3.0 | 3.0 | 4.0 | ... |
| $\alpha_2$ | 0.5 | 1.0 | 1.0 | 1.5 | 2.0 | 2.0 | 2.5 | 3.0 | 3.0 | ... |

**Table 4.2 -** *Approximations to* $\alpha_1$ *and* $\alpha_2$

The parameters $\alpha_1$ and $\alpha_2$ can be approximated by making some assumptions concerning the topology of the S blocks. It is assumed here that the topology is similar to the one used in Chapter 4. This means that, as $F_s$ is increased from its minimum value of 2, switches are added to the wiring segments in the order straight across, right turn, left turn, straight across, right turn, etc.. It is further assumed that the topology spreads the switches among the tracks such that every track can be switched to exactly $F_s$ others.

Given these assumptions, appropriate values of $\alpha_1$ and $\alpha_2$ are shown in Table 4.2.

### 5.5.1 Routability Predictions

Recall, from Section 5.2, that routability is defined as

$$Routability = \frac{1}{C_T} \sum_{i=1}^{C_T} P(R_{C_i}), \qquad 5.19$$

This equation can now be evaluated using Equation 5.17, the formulas developed in Section 5.4, Equation 5.18, and Tables 4.1 and 4.2. A typical result is shown in Figure 5.7, which gives a plot of the expected percentage of successfully completed connections versus connection block flexibility, $F_c$, for parameters that correspond to the circuit BNRE.

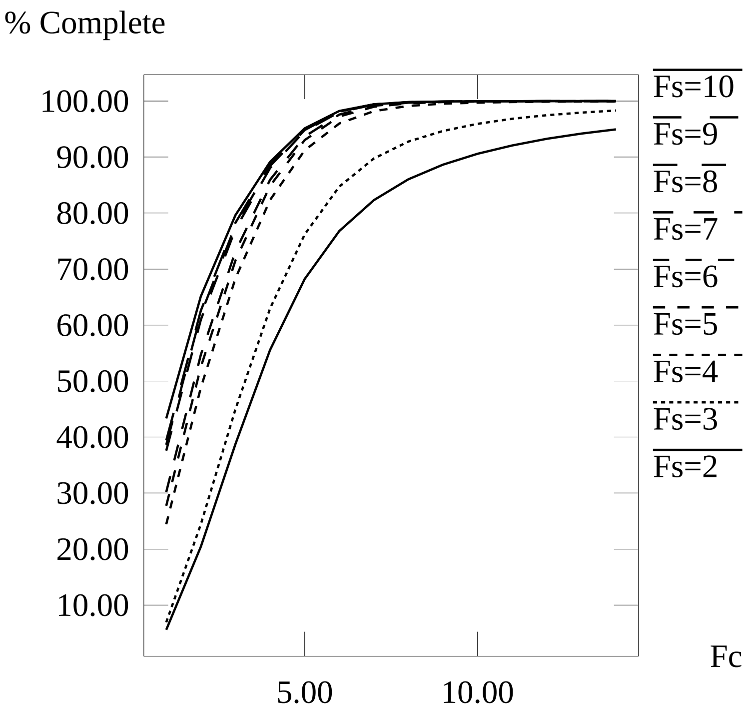


**Figure 5.7 -** *Routability Predictions vs. $F_s$, for Circuit BNRE*

Figure 5.7 is analogous to Figure 4.9. Each curve in the figure corresponds to a different value of S block flexibility, $F_s$. The lowest curve represents the case $F_s = 2$ and the highest curve corresponds to $F_s = 10$. The figure indicates that the routability is low for small values of $F_c$ and only approaches 100% when $F_c$ is at least one-half of W. The figure also shows that increasing the S block flexibility improves the completion rate at a given $F_c$, but to get near 100% the value of $F_c$ must always be high (above 7 for this circuit). The reader will note that these are the same conclusions that were reached experimentally in Chapter 4.

Figure 5.8 is a plot of the expected percentage of successfully completed connections versus S block flexibility, $F_s$, also for the circuit BNRE. This figure is analogous to Figure 4.12. Each curve in the figure corresponds to a different value of $F_c$, with the lowest curve representing $F_c = 1$ and the highest curve corresponding to $F_c = W$. The curves show an increase in slope at $F_s$ values of 4, 7, and 10. This occurs because switches are added straight across the S blocks for these values of $F_s$ and, as Table 4.1 shows, connections pass straight through the S blocks more than 70 percent of the time. Figure 5.8 shows that if $F_c$ is at least half of $W$, then very low values of $F_s$ approach 100% routability. Again, this is the same conclusion reached in Chapter 4.

While the theoretical and experimental results lead to the same general conclusions, they are not identical. Figure 5.9 compares the routability results produced by the stochastic model with the experimental results. The dashed curve corresponds to the model, whereas the solid curve is produced experimentally. Both curves correspond to circuit BNRE, with $F_s = 6$. As Figure 5.9 indicates, the two results are quite similar. The fact that the theoretical curve is lower than the experimental curve for low values of $F_c$ is due in part to Equation 5.14, which, as discussed in Section 5.4, does not accurately represent

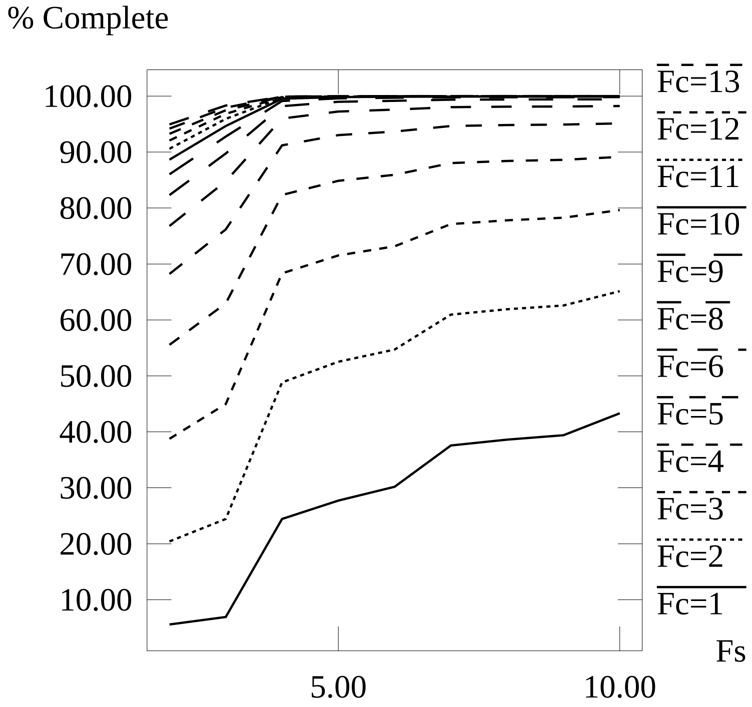


**Figure 5.8 -** *Routability Predictions vs. $F_c$, for Circuit BNRE*

good C block topologies. A summary of comparisons between theory and experiment for all of the circuits appears in Table 5.3. For each circuit, the table shows the difference between the theoretical and experimental routability results, for each value of $F_s$. Each entry gives the mean value (and standard deviation) of the difference between the experimental and theoretical routabilities, over the range of values of $F_c$ from 1 to $W$. The values in the table are in percentages since those are the units of routability. Absolute values are used in the table to avoid a misleading average that could be caused by combining negative and positive differences. However, this is not really necessary since, as Figure 5.9 indicates, the theoretical predictions are almost always pessimistic. As Table 5.3 shows, the experimental measurements and theoretical predictions of routability are surprisingly close, especially for values of $F_s$ greater than three.

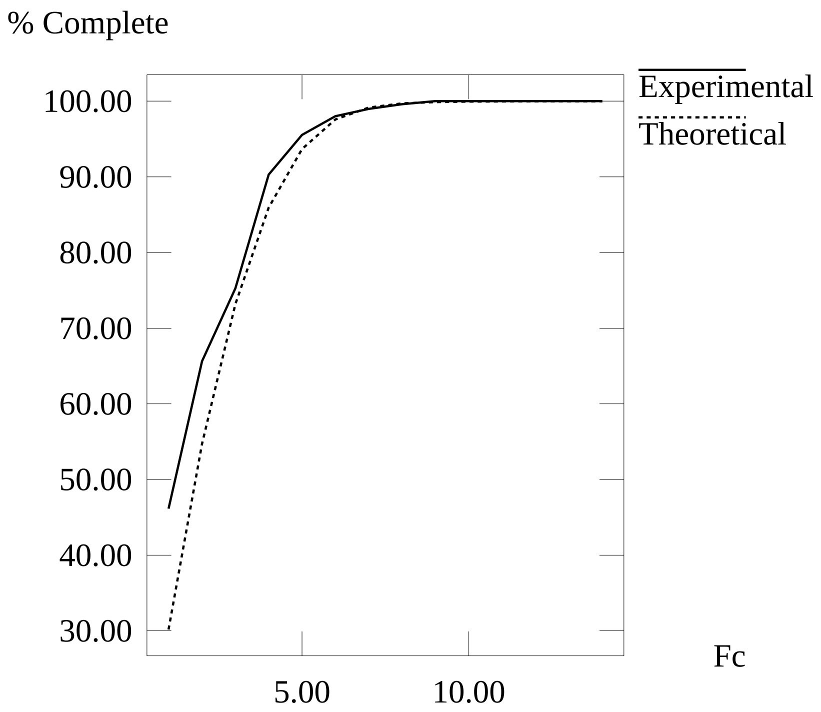


**Figure 5.9 -** *Comparison of Predictions and Experiments for* $F_s = 6$

| | BUSC | | DMA | | BNRE | | DFSM | | Z03 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $F_s$ | Mean | S.D. | Mean | S.D | Mean | S.D. | Mean | S.D. | Mean | S.D. |
| 2 | 7.7 | 4.9 | 10.2 | 7.5 | 7.3 | 6.3 | 8.9 | 8.3 | 7.2 | 5.9 |
| 3 | 9.7 | 5.6 | 12.5 | 8.1 | 8.7 | 6.7 | 10.8 | 9.4 | 10.2 | 5.6 |
| 4 | 2.9 | 2.9 | 4.1 | 4.5 | 1.5 | 3.1 | 2.7 | 5.3 | 1.9 | 2.1 |
| 5 | 3.7 | 4.3 | 4.9 | 5.8 | 2.4 | 4.3 | 3.7 | 6.1 | 1.8 | 2.7 |
| 6 | 3.2 | 3.5 | 5.0 | 6.2 | 2.6 | 4.7 | 4.0 | 6.7 | 2.1 | 3.3 |
| 7 | 4.8 | 4.3 | 5.1 | 6.6 | 2.8 | 4.3 | 3.9 | 6.1 | 1.8 | 2.8 |
| 8 | 4.3 | 4.6 | 5.1 | 6.5 | 3.1 | 4.3 | 4.1 | 6.2 | 2.2 | 2.6 |
| 9 | 4.3 | 4.9 | 5.0 | 6.3 | 3.2 | 4.4 | 4.2 | 6.2 | 2.5 | 3.0 |
| 10 | 4.3 | 4.8 | 5.2 | 6.7 | 3.2 | 4.3 | 4.2 | 5.9 | 2.9 | 3.4 |

**Table 5.3 -** *Summary of Comparisons Between Theory and Experiment*

## 5.6 Conclusions

This chapter has developed a stochastic model that can be used to study the effect of the flexibility of an FPGA’s routing architecture on its routability. It has been shown that the model can be used to reach the same conclusions that were generated in Chapter 4 using an experimental approach. In future work the model could be extended to handle the case where some of the routing switches in the S blocks are replaced by hard-wired connections. This would allow the modelling of routing architectures in which the tracks may be composed of segments of various lengths and would allow the stochastic model to be used to study such architectures.