# 6 Conclusions

## 6.1 Thesis Summary

The main focus of this thesis has been the study of FPGA routing architectures with regard to the tradeoff among routability, area and speed performance. The study's purpose has been to determine the level of flexibility of routing architectures that is high enough so that real circuits can be successfully routed, and yet low enough so that routing switches are not wasted. The research has been carried out using both experimental and theoretical approaches. In the experimental study, a new type of detailed routing algorithm, parameterized for different levels of flexibility, has been used to measure the effects of flexibility on the routability of circuits. Theoretical methods have also been applied to study this issue, using a stochastic modelling approach that predicts, based on combinatorial analysis, the effect of flexibility on routability. The results of the work in the thesis provide new insights into the design of FPGA routing algorithms and routing architectures.

## 6.2 Thesis Contributions

In Chapter 3, the Coarse Graph Expansion (CGE) detailed routing algorithm for FPGAs was described. It is the first published algorithm that approaches FPGA routing in a general way, and it can be used over a wide range of routing architectures. CGE employs a heuristic approach that bases routing decisions on a global cost function that accounts for contention for the routing resources that may exist among the connections in a circuit. The cost function also allows the optimization of routing delays for time-critical connections. CGE has been used to obtain excellent routing results for relatively large FPGA routing problems.

Chapter 4 gives the results of an experimental study of the effects on routability of the flexibility of FPGA routing architectures. This study is the first of its kind for FPGAs. The principal conclusions reached are that a high level of connectivity is desirable in the connection blocks that join the logic cell pins to the routing channels, but that a relatively low flexibility is sufficient in the switch blocks at the intersections of horizontal and vertical channels. Also, it is shown that, even with surprisingly low levels of flexibility, circuits can be routed with very close to the theoretical minimum number of tracks per channel. Finally, the results show the effect of the flexibility of the routing architecture on the total number of routing switches needed in an FPGA.

A theoretical foundation that can be used to study FPGA routing architectures is developed in Chapter 5. A stochastic model is presented that uses probability theory to predict the routability of circuits over a range of flexibility. The probability expressions are based on combinatorial analysis that accounts for both the flexibility of the routing architecture and the side-effects that the successful routing of one connection has on others. It is shown that the stochastic model can be used to reach the same conclusions that were found experimentally in Chapter 4.

## 6.3 Suggestions for Future Research

A future enhancement for the CGE detailed router could improve upon the usage of routing tracks comprising wiring segments that span multiple logic cells. Currently, special attention is paid to the segmentation-length of tracks only when routing time-critical connections. A better approach would be for the router to assign tracks to each connection such that the segmentation-length of the track matches, as closely as practical, the length of the connection. Both phases of the algorithm are affected by this issue. First, when paths are pruned from expanded graphs during graph expansion, those paths that correspond to tracks that have appropriate segment lengths should be given preference. Second, during path selection, segment lengths should be considered when specific tracks are chosen for each connection. These modifications to the algorithm's implementation should be integrated with the current cost function so that a high quality of routing can still be obtained, but with improved usage of segmented tracks.

A topic of future research that may yield significant results is the development of a near-optimal detailed router for FPGAs. The following discussion describes how such a router could be realized by building upon the results of this thesis. The CGE algorithm follows a heuristic approach; a pruning procedure controls the complexity of the routing problem, and an approximate cost function is used to resolve routing conflicts. The heuristic approach is necessary for two reasons:

(1) The number of possible detailed routes for a connection is an exponential function of the length of the connection.

(2) The number of connections to be routed is large.

Using the routing architecture flexibility results in this thesis, issue (1) can be removed by constraining the flexibility of the switch blocks ($F_S \leq 3$). While issue (2) still remains, it too can be eliminated by using the CGE router. An interesting scheme would be one that uses CGE to complete the detailed routes of all but the most difficult connections in a circuit. Then, for channel segments that still contain unrouted connections, a final routing stage could be invoked to try to complete the routing task. Having greatly reduced the scope of the problem, it should be practical to implement the final routing stage using some sort of optimal assignment algorithm. Note that the overall solution is still only "near-optimal" since there might be some influence on the final routing stage of decisions made by the heuristic.

The routing architecture results that are presented in Chapter 4 assume routing tracks that have a segmentation-length of one. Future research should expand this study to include other segment lengths. There are three issues to be addressed:

(1) How many tracks of each segmentation-length should be included?

(2) What connectivity should be available among the various tracks?

(3) How should the segmented tracks be populated? For segmented tracks, this issue refers to whether or not there should be routing switches, in the connection and switch blocks, that connect to the middle sections of segments.

The stochastic model described in Chapter 5 also assumes that tracks have a segmentation-length of one. The theory should be extended to include other segment lengths so that the model could be used to study such architectures. Appropriate modifications would also be necessary for the method that is used to approximate channel density, since it is also based on non-segmented channels.