References

[1] ACTEL, *Actel FPGA Data Book and Design Guide*, Actel Corp., 955 East Arques Avenue, Sunnyvale, CA 94086, 1996.

[2] C. ALPERT, *Private communication.* UCLA and IBM Austin.

[3] C. J. ALPERT AND A. B. KAHNG, *Recent Directions in Netlist Partitioning: A Survey*, Integration, the VLSI Journal, 12 (1995), pp. 1–81.

[4] ALTERA, *Altera Data Book*, Altera Corp., 2610 Orchard Parkway, San Jose, CA 95134-2020, 1996.

[5] G. BATTISTA, P. EADES, R. TAMASSIA, AND I. TOLLIS, *Algorithms for Automatic Graph Drawing: An Annotated Bibliography.* Tech. Report, Dept. of Computer Science, Brown University, Providence, RI. (Updated regularly.), 1989.

[6] A. BEKESSY, P. BEKESSY, AND J. KOMLÓS, *Asymptotic Enumeration of Regular Matrices*, Stud. Sci. Math. Hungar, 7 (1972), pp. 343–353.

[7] E. A. BENDER AND E. R. CANFIELD, *The asymtotic number of labelled graphs with given degree sequences*, J. Comb. Theory (A), 24 (1978), pp. 296–307.

[8] V. BETZ AND J. ROSE, *Directional Bias and Non-Uniformity in FPGA Global Routing Architectures*, in IEEE/ACM International Conference on Computer Aided Design (ICCAD), 1996, pp. 652–659.

[9] B. BOLLOBÁS, *A Probabilistic Proof of an Asymptotic Formula for the Number of Labelled Regular Graphs*, Europ. J. Combinatorics, 1 (1980), pp. 311–316.

[10] S. D. BROWN, *Routing algorithms and architectures for Field-Programmable Gate Arrays*, PhD thesis, University of Toronto, January, 1992.

[11] S. D. BROWN, R. J. FRANCIS, J. ROSE, AND Z. G. VRANESIC, *Field-Programmable Gate Arrays*, Kluwer, Norwell, Mass., 1992.

[12] P. K. CHAN, M. D. F. SCHLAG, AND J. Y. ZIEN, *On routability prediction for field-programmable gate arrays*, in Proc. 30th ACM/IEEE Design Automation Conference, 1993, pp. 326–330.

[13] J. CONG AND Y. DING, *FlowMap: An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs*, IEEE Trans. CAD, 13 (June, 1994), pp. 1–12.

[14] D. G. CORNEIL, H. LERCHS, AND L. A. STEWART-BURLINGHAM, *Complement reducible graphs*, Disc. Appl. Math, 3 (1981), pp. 163–174.

[15] J. DARNAUER AND W. DAI, *A Method for Generating Random Circuits and Its Application to Routability Measurement*, in 4th ACM/SIGDA Int'l Symp. on FPGAs (FPGA96), Feb., 1996, pp. 66–72.

[16] W. E. DONATH, *Statistical Properties of the Placement of a Graph*, SIAM J. Appl. Math, 16 (1968), pp. 439–457.

[17] ——, *Equivalence of Memory to Random Logic*, IBM J. Res. Dev., 18 (1974), pp. 401–407.

[18] ——, *Placement and average interconnection lengths of computer logic*, IEEE Trans. Comp., CAS-26 (1979), pp. 272–277.

[19] ——, *Wire length distribuition for placements of computer logic*, IBM J. Res. Dev., 25 (1981), pp. 152–155.

[20] ——, *Hierarchical structure of computers*, Tech. Rep. RC 2392, IBM T. J. Watson Research Centre, Yorktown Heights, N. Y. USA, March 1969.

[21] P. EADES, B. MCKAY, AND N. WORMALD, *On an edge-crossing problem*, in Proc. 9th Australian Computer Science Conference, 1986, pp. 327–334.

[22] P. EADES AND N. C. WORMALD, *Edge Crossings in Drawings of Bipartite Graphs*, Algorithmica, (1994), pp. 379–403.

[23] A. EL GAMAL, *Two-dimensional stochastic model for interconnections in master slice integrated circuits*, IEEE Trans. on Circuits and Systems, CAS-28 (1981), pp. 127–138.

[24] A. EL GAMAL AND Z. A. SYED, *A New Statistical Model for Gate Array Routing*, in Proc. 20th ACM/IEEE Design Automation Conference, 1983, pp. 671–674.

[25] M. FEUER, *Connectivity of Random Logic*, IEEE Trans. Comp., C-31 (1982), pp. 29–33.

[26] C. M. FIDUCCIA AND R. M. MATTHEYSES, *A linear time heuristic for improving network partitions*, in 19th ACM/SIGDA Design Automation Conference (DAC), 1982, pp. 175–181.

[27] R. J. FRANCIS, J. ROSE, AND K. CHUNG, *Chortle: A Technology Mapping Program for Lookup Table-Based Field Programmable Gate Arrays*, in Proc. 27th ACM/IEEE Design Automation Conference, 1990, pp. 613–619.

[28] A. M. FRIEZE, *On Random Regular Graphs with Non-Constant Degree*, tech. rep., Research Report #88-2, Dept. of Mathematics, Carnegie Mellon Univesity, 1988.

[29] M. R. GAREY AND D. S. JOHNSON, *Computers and Intractability: A Guide to the Theory of NP-Completeness*, W. H. Freeman and Company, New York, 1979.

[30] E. R. GASNER, E. KOUTSOFIOS, S. C. NORTH, AND K.-P. VO, *A Technique for Drawing Directed Graphs*, IEEE Trans. Software Eng., 19 (1993), pp. 214–230.

[31] A. GIBBONS, *Algorithmic Graph Theory*, Cambridge University Press, Great Britain, 1985.

[32] M. C. GOLUMBIC, *Combinatorial merging*, IEEE Trans. Comput., 25 (1976), pp. 1164–1167.

[33] J. GREENE, V. ROYCHOWDHURY, S. KAPTANOGLU, AND A. E. GAMAL, *Segmented Channel Routing*, in Proc. 27th ACM/IEEE Design Automation Conference, 1990, pp. 567–592.

[34] L. HAGEN AND A. B. KAHNG, *A New Approach to Effective Circuit Clustering*, in Proc. ACM/SIGDA Int'l Conference on Computer Aided Design (ICCAD), 1992, pp. 422–427.

[35] L. HAGEN, A. B. KAHNG, F. J. KURDAHI, AND C. RAMACHANDRAN, *On the Intrinsic Rent Parameter and Spectra-Based Partitioning Methodologies*, IEEE Trans. CAD, 13 (1994), pp. 27–37.

[36] N. HARADA, *A New Average Interconnection Length Prediction Method for Master-slice LSI*, in Proc. 19th ACM/IEEE Design Automation Conference (DAC), 1982, pp. 127–138.

[37] S. HAUK, G. BORRIELLO, AND C. EBLING, *Mesh Routing Topologies for FPGA Arrays*, in Proc. 2nd ACM/SIGDA Int'l Conference on FPGAs (FPGA94), 1994.

[38] H. J. HOOVER, M. M. KLAWE, AND N. J. PIPPENGER, *Bounding fan-out in logical networks*, J. ACM, 31 (1984), pp. 13–18.

[39] M. HUTTON, J. ROSE, AND D. CORNEIL, *Generation of Synthetic Sequential Benchmark Circuits*, in 5th ACM/SIGDA Int'l Symp. on FPGAs (FPGA97), 1997, pp. 149–155.

[40] M. D. HUTTON, *CIRC/GEN Web-site*.
http://www.eecg.toronto.edu/~mdhutton/gen/, 1997.

[41] M. D. HUTTON, J. P. GROSSMAN, J. S. ROSE, AND D. G. CORNEIL, *Characterization and Parameterized Random Generation of Digital Circuits*, in 33rd ACM/SIGDA Design Automation Conference (DAC), June., 1996, pp. 94–99.

[42] M. D. HUTTON, J. S. ROSE, J. P. GROSSMAN, AND D. G. CORNEIL, *Characterization and Parameterized Random Generation of Combinational Benchmark Circuits*. Submitted for journal publication.

[43] K. IWAMA AND K. HINO, *Random Generation of Test Instances for Logic Optimizers*, in Proc. 31st Design Automation Conference, 1994, pp. 430–434.

[44] K. IWAMA, K. HINO, H. KUROKAWA, AND S. SAWADA, *Random Benchmark Circuits with Controlled Attributes*, in To appear, Proc. 1997 European Design and Test Conference, 1997.

[45] D. S. JOHNSON, C. R. ARAGON, L. A. MCGEOCH, AND C. SCHEVON., *Optimization by simulated annealing: An experimental evaluation (Part I)*. Preprint, AT&T Bell Laboratories. Murray Hill, NJ, 1985.

[46] B. W. KERNIGHAN AND S. LIN, *An Efficient Heuristic Procedure for Partitioning Graphs*, Bell Systems Technical Journal, 49 (Feb., 1970), pp. 291–307.

[47] E. KOUTSOFIOS AND S. C. NORTH, *Drawing graphs with* DOT, tech. rep., AT&T Bell Laboratories, Murray Hill, New Jersey 07974, USA, 1993.

[48] B. KRISHNAMURTHY, *An improved min-cut algorithm for partitioning VLSI networks*, IEEE Transactions on Computers, C-33 (1984), pp. 438–446.

[49] B. S. LANDMAN AND R. L. RUSSO, *On a Pin Versus Block Relationship for Partitions of Logic Graphs*, IEEE Trans. Comp., C-20 (1971), pp. 1469–1479.

[50] T. LENGAUER, *Combinatorial Algorithms for Integrated Circuit Layout*, Wiley, West Sussex, England, 1990.

[51] B. D. MCKAY AND N. C. WORMALD, *Uniform Generation of Random Regular Graphs of Moderate Degree*, J. Algorithms, 11 (1990), pp. 52–57.

[52] R. M. MEADE AND H. GELLER, *Systems 360 Influence on the Design of Solid Logic Technology*, Solid State Design/Circuit Design Eng., (July 1965).

[53] M. MOLLOY, *Private communication*. University of Toronto.

[54] R. MURGAI, N. SHENOY, R. K. BRAYTON, AND A. SANGIOVANNI-VINCENTELLI, *Improved Logic Synthesis Algorithms for Table Look Up Architectures*, in Proc. Intl. Conf. on CAD, 1991.

[55] W. A. NOTZ, E. SCHISCHA, J. L. SMITH, AND M. G. SMITH, *Benefiting the System Designer*, Electronics, (Februrary 1967).

[56] PROGRAMMABLE ELECTRONICS PERFORMANCE CORPORATION, *PREP PLD Benchmark Suite#1, V1.2*. 504 Nino Ave. Los Gatos, CA 95032. http://www.prep.org, 1993.

[57] C. E. RADKE, *A justification of and an improvement on a useful rule for predicting circuit-to-pin ratios*, in Proc. 6th Annual SHARE/ACM/IEEE Design Automation Workshop, 1969, pp. 257–267.

[58] R. L. RUSSO, *On the Tradeoff Between Logic Performance and Circuit-to-Pin Ratio for LSI*, IEEE Trans. Comp., C-21 (1972), pp. 147–153.

[59] S. SASTRY AND A. C. PARKER, *Stochastic Models for Wireability Analysis of Gate Arrays*, IEEE Transactions on Computer-Aided Design, CAD-5 (1986), pp. 52–65.

[60] M. D. F. SCHLAG, J. KONG, AND P. K. CHAN, *Routability-Driven Technology Mapping for Lookup Table-Based FPGAs*, IEEE. Trans. CAD, 13 (Jan., 1994), pp. 13–26.

[61] C. SECHEN, *Average interconnection length estimation for random and optimal placements*, in Proc. IEEE International Conference on Computer Aided Design (ICCAD), 1988, pp. 190–193.

[62] E. M. SENTOVICH *et.al*, *SIS: A System for Sequential Circuit Analysis*. Tech. Report No. UCB/ERL M92/41. University of California, Berkeley, 1992.

[63] S. D. SHEW, *A Cograph Approach to Examination Scheduling*, Master's thesis, University of Toronto, 1986.

[64] J. SPENCER, *Ten Lectures on the Probabilistic Method*, Society for Industrial and Applied Mathematics, Philadelphia, PA, 1987.

[65] K. S. SUGIYAMA, S. TAGAWA, AND M. TODA, *Methods for visual understanding of hierarchical system structures*, IEEE Trans. Syst. Man, Cybern,, SMC-11 (1981), pp. 109–125.

[66] R. E. TARJAN, *Data Structures and Network Algorithms*, Society for Industrial and Applied Mathematics., Philadelphia, PA, 1983.

[67] L. TREVILLYAN, *An Experiment in Technology Mapping for FPGAs using a fixed Library.*, in International Logic Synthesis (IWLS) Workshop, 1993.

[68] J. VARGHESE, M. BUTTS, AND J. BATCHELLER, *An Efficient Logic Emulation System*, IEEE Trans. VLSI Systems, 1 (1993), pp. 171–174.

[69] S. J. E. WILTON, *Architectures and Algorithms for Field-Programmable Gate Arrays with Embedded Memory*, PhD thesis, University of Toronto, 1997.

[70] S. J. E. WILTON, J. ROSE, AND Z. G. VRANESIC, *Memory-to-Memory Connection Structures in FPGAs with Embedded Memory Arrays*, in 5th ACM/SIGDA Int'l Symp. on FPGAs (FPGA97), 1997, pp. 10–16.

[71] N. C. WORMALD, *The Asymptotic Connectivity of Labelled Regular Graphs*, J. Comb. Theory (B), 31 (1981), pp. 156–167.

[72] ——, *The Asymptotic Distribution of Short Cycles in Random Regular Graphs*, J. Comb. Theory (B), 31 (1981), pp. 156–167.

[73] XILINX, *The Programmable Gate Array Data Book*, Xilinx Inc., 2100 Logic Drive, San Jose, CA 95124, 1996.

[74] S. YANG, *Logic Synthesis and Optimization Benchmarks, Version 3.0*, tech. rep., Microelectronics Centre of North Carolina, P.O. Box 12889, Research Triangle Park, NC 27709 USA, 1991.